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# FCH043N60

## N-Channel SuperFET® II MOSFET

600 V, 75 A, 43 mΩ

### Features

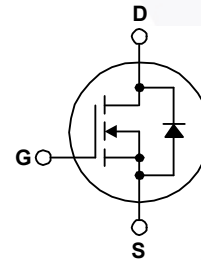
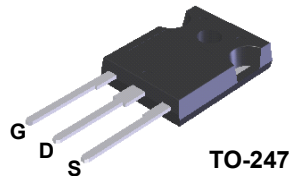
- 650 V @  $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(on)} = 37\text{ m}\Omega$
- Ultra Low Gate Charge (Typ.  $Q_g = 163\text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)} = 730\text{ pF}$ )
- 100% Avalanche Tested
- RoHS Compliant

### Applications

- Telecom / Server Power Supplies
- Industrial Power Supplies

### Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is suitable for various AC/DC power conversion for system miniaturization and higher efficiency.



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCH043N60	Unit
$V_{DSS}$	Drain to Source Voltage	600	V
$V_{GSS}$	Gate to Source Voltage	- DC	$\pm 20$
		- AC ( $f > 1\text{ Hz}$ )	$\pm 30$
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	75
		- Continuous ( $T_C = 100^\circ\text{C}$ )	47.5
$I_{DM}$	Drain Current	- Pulsed (Note 1)	225
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	2025
$I_{AR}$	Avalanche Current	(Note 1)	15
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	5.92
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	20	
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	592
		- Derate Above $25^\circ\text{C}$	4.74
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FCH043N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.21	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH043N60	FCH043N60	TO-247	Tube	N/A	N/A	30 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}, T_C = 25^\circ\text{C}$	600	-	-	V
		$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}, T_C = 150^\circ\text{C}$	650	-	-	
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$ , Referenced to $25^\circ\text{C}$	-	0.67	-	$V/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_C = 125^\circ\text{C}$	-	4.5	-	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	2.5	-	3.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 38\text{ A}$	-	37	43	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 38\text{ A}$	-	73	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	9194	12225	pF
$C_{oss}$	Output Capacitance		-	353	470	pF
$C_{rss}$	Reverse Transfer Capacitance		-	11	16	pF
$C_{oss\text{eff}}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$	-	730	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380\text{ V}, I_D = 38\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)	-	163	215	nC
$Q_{gs}$	Gate to Source Gate Charge		-	35	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	39	-	nC
ESR	Equivalent Series Resistance	$f = 1\text{ MHz}$	-	1.1	-	$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380\text{ V}, I_D = 38\text{ A}, V_{GS} = 10\text{ V}, R_G = 4.7\text{ }\Omega$ (Note 4)	-	46	102	ns
$t_r$	Turn-On Rise Time		-	36	82	ns
$t_{d(off)}$	Turn-Off Delay Time		-	162	334	ns
$t_f$	Turn-Off Fall Time		-	6	-	ns

### Drain-Source Diode Characteristics

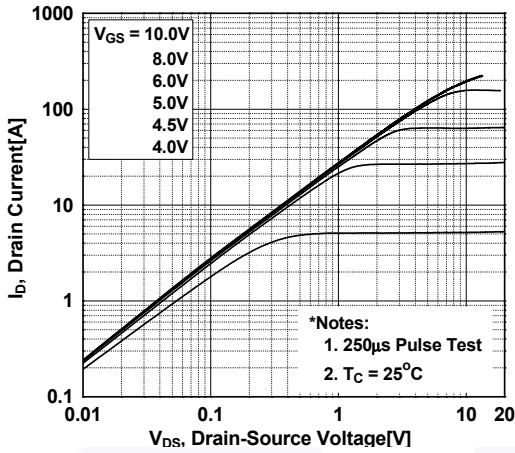
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	75	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	225	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 38\text{ A}$	-	-	1.2	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 38\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$	-	605	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	16	-	$\mu\text{C}$

#### Notes:

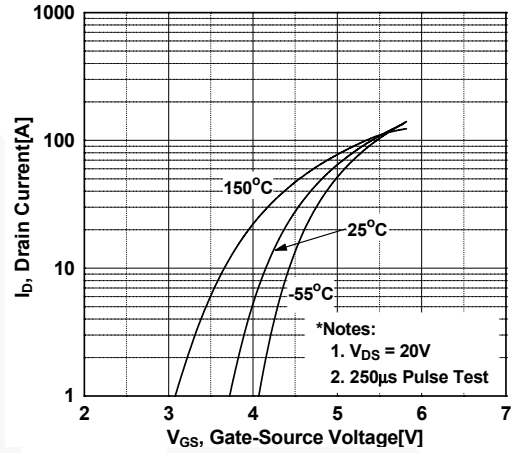
1. Repetitive rating; pulse-width limited by maximum junction temperature.
2.  $I_{AS} = 15\text{ A}, R_G = 25\text{ }\Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 38\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq 380\text{ V}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.

## Typical Performance Characteristics

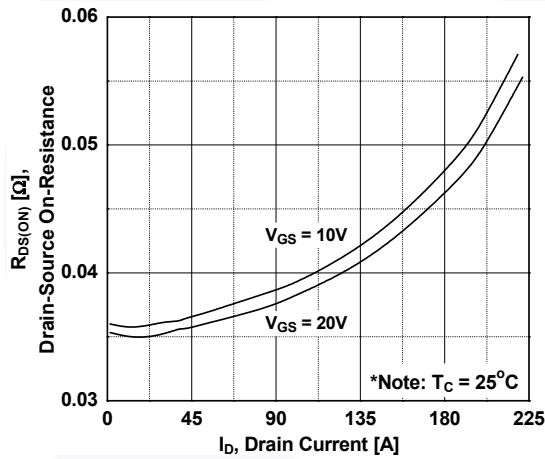
**Figure 1. On-Region Characteristics**



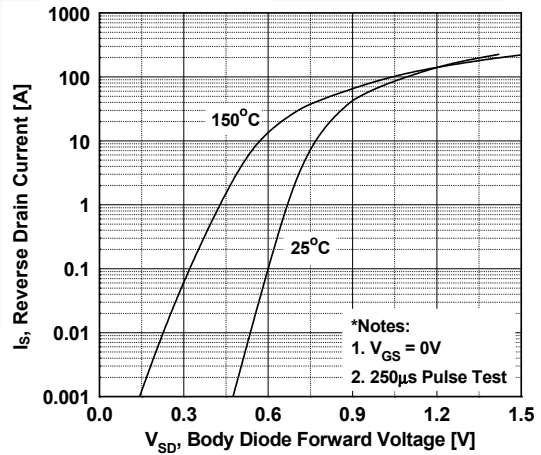
**Figure 2. Transfer Characteristics**



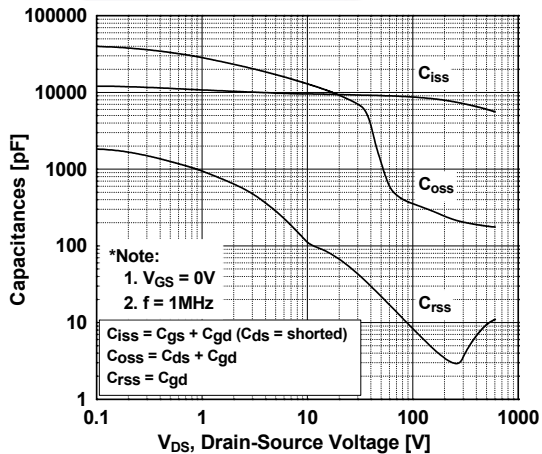
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



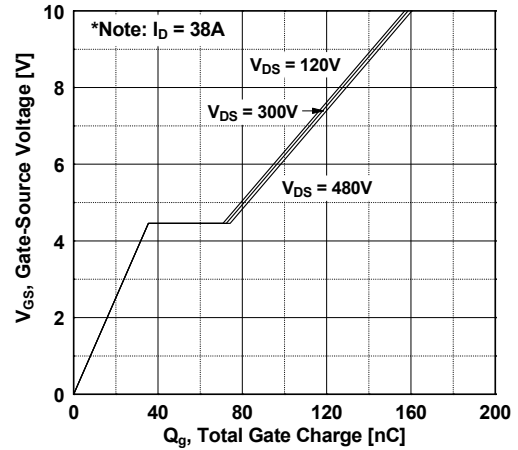
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

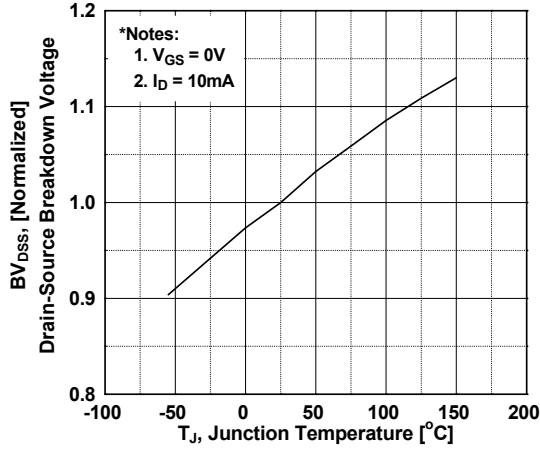


**Figure 6. Gate Charge Characteristics**

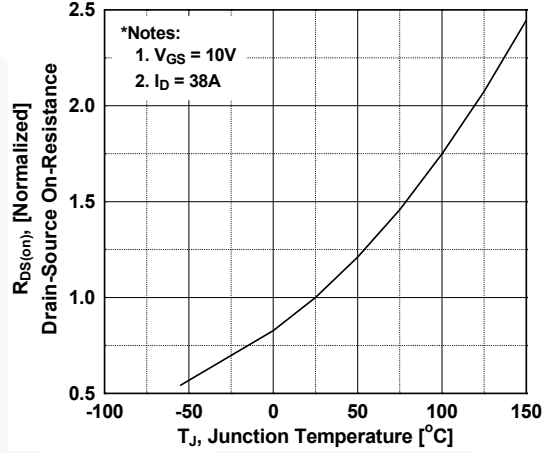


**Typical Performance Characteristics** (Continued)

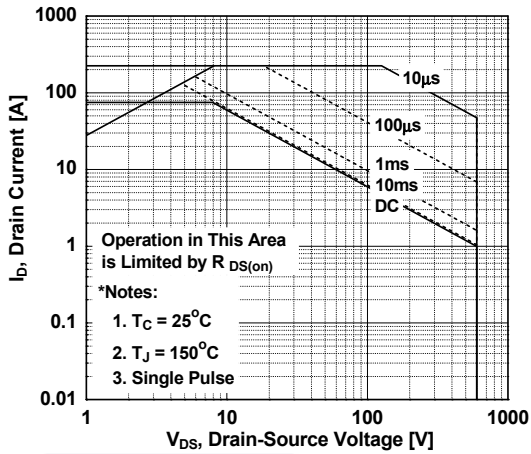
**Figure 7. Breakdown Voltage Variation vs. Temperature**



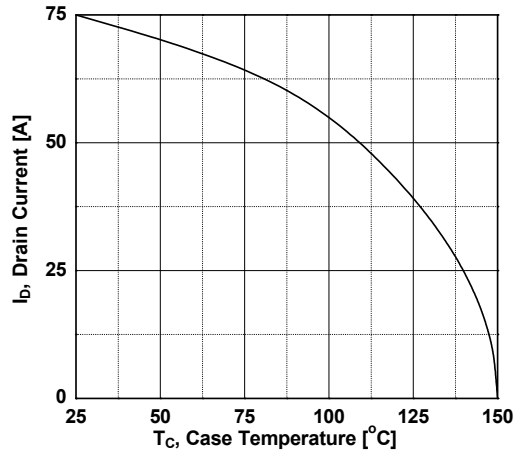
**Figure 8. On-Resistance Variation vs. Temperature**



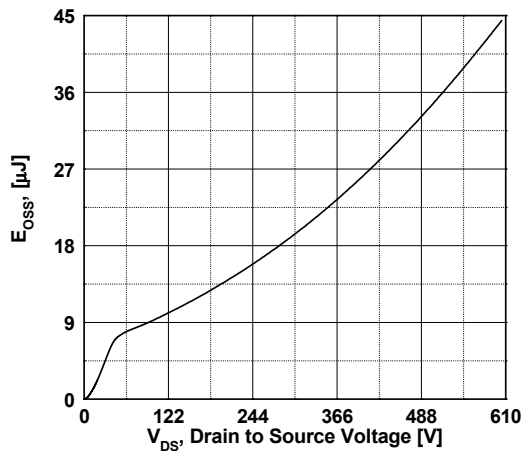
**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. E\_oss vs. Drain to Source Voltage Switching Capability**



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve

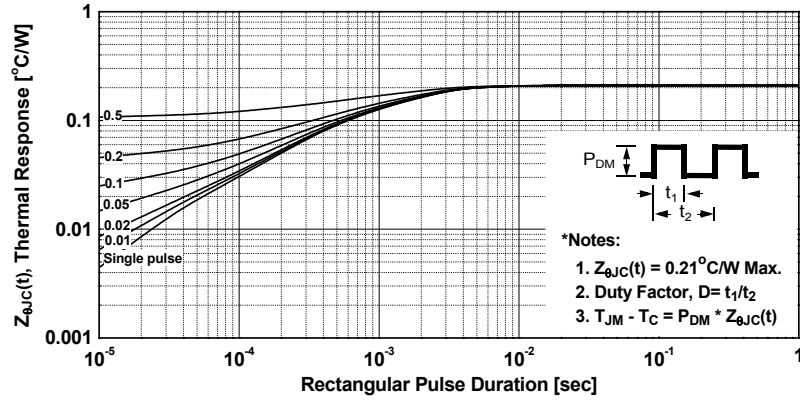


Figure 13. Gate Charge Test Circuit & Waveform

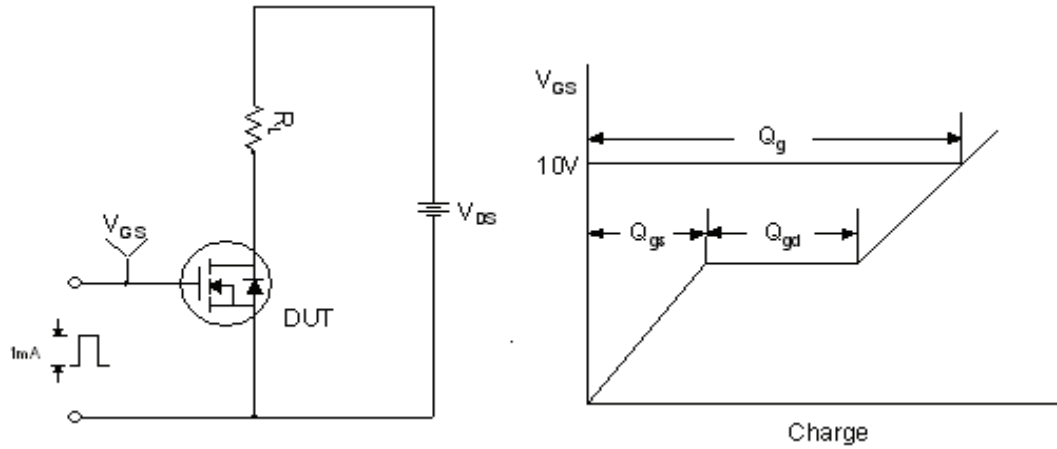


Figure 14. Resistive Switching Test Circuit & Waveforms

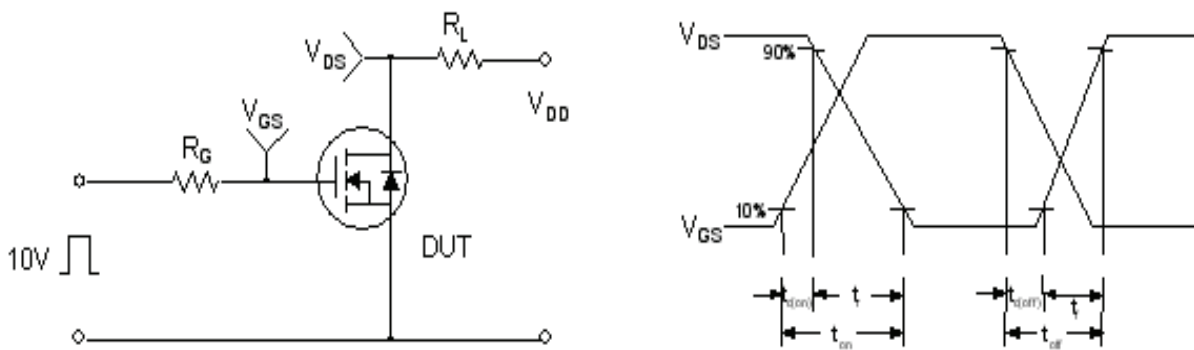


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

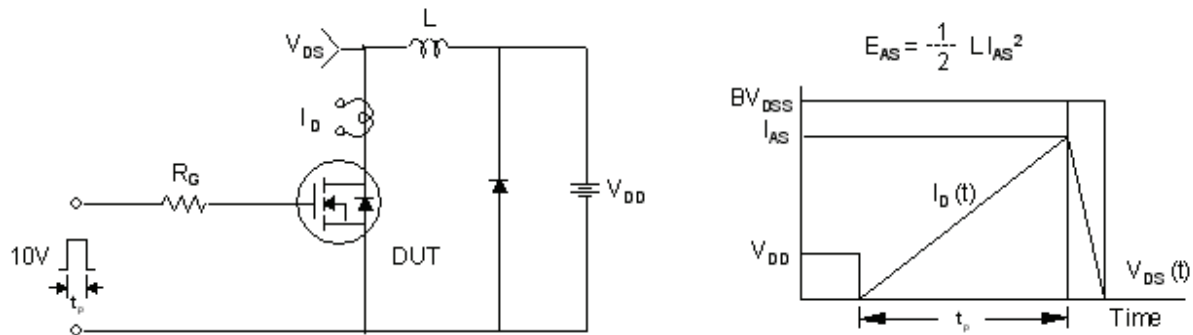
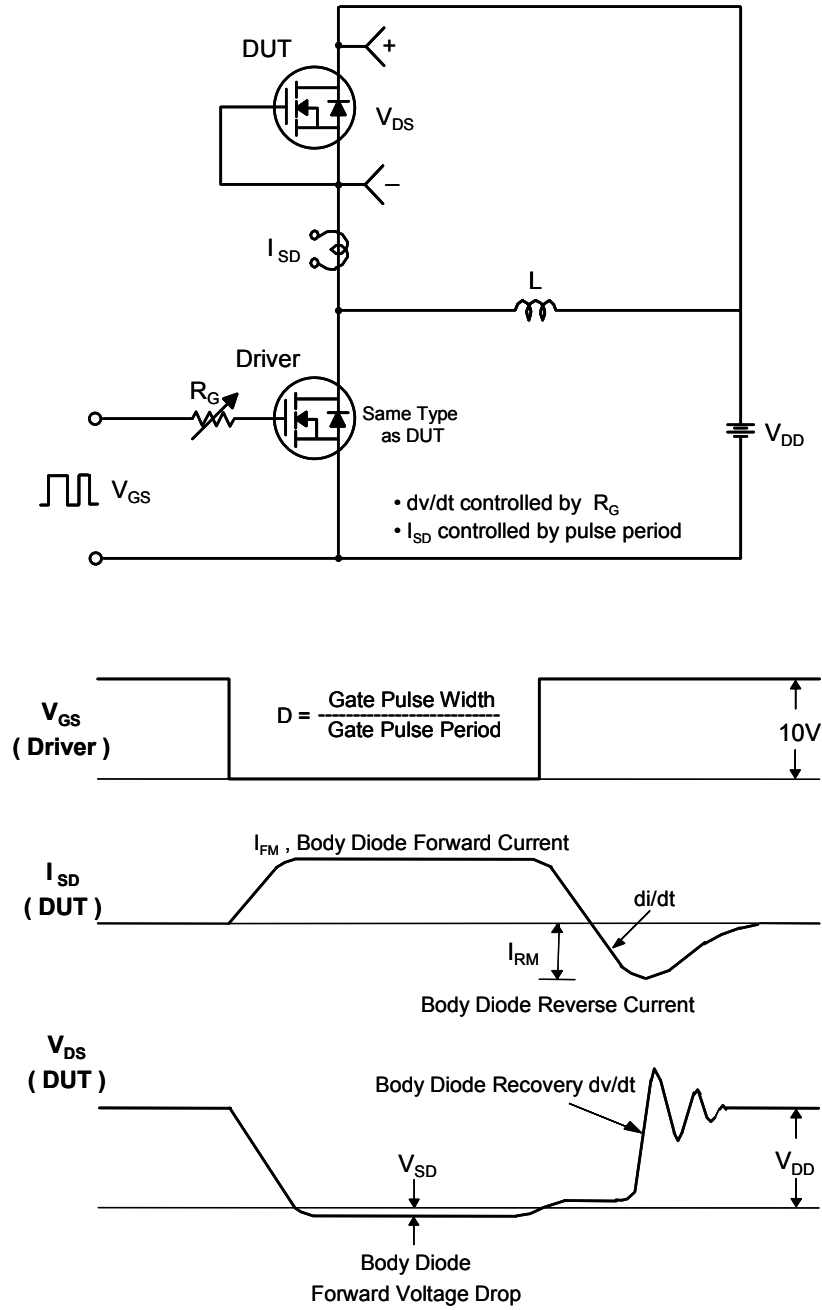


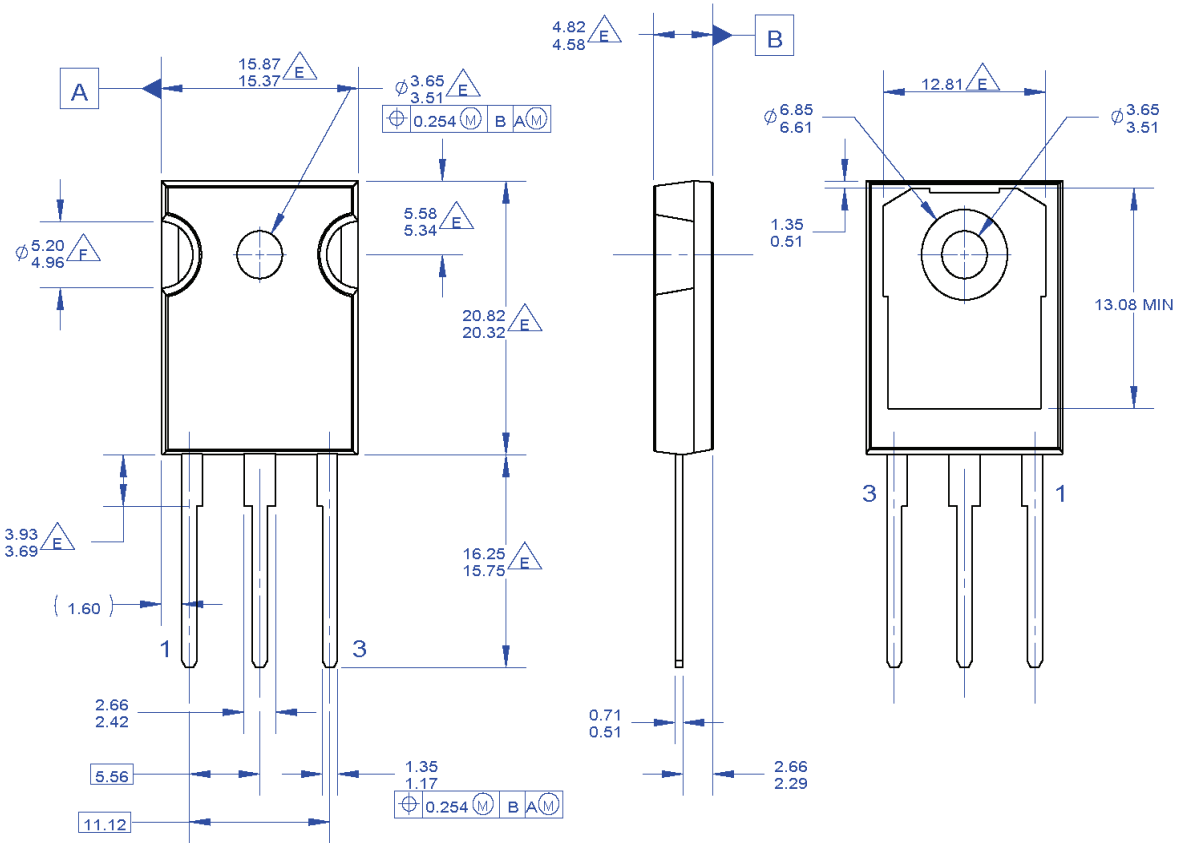
Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms





## Mechanical Dimensions

### TO-247 3L



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$\triangle E$  DOES NOT COMPLY JEDEC STANDARD VALUE

$\triangle F$  NOTCH MAY BE SQUARE

G. DRAWING FILENAME: MKT-TO247A03\_REV03

**Figure 17. TO-247, Molded, 3 Lead, Jeduc Variation AB**

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