



ON Semiconductor®

# FCH190N65F-F085

## N-Channel SuperFET II FRFET MOSFET

650 V, 20.6 A, 190 mΩ

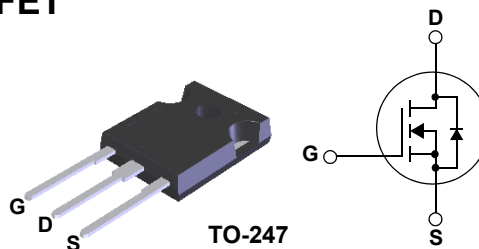
### Features

- Typical  $R_{DS(on)}$  = 148 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 10\text{ A}$
- Typical  $Q_{g(tot)}$  = 63 nC at  $V_{GS} = 10\text{ V}$ ,  $I_D = 10\text{ A}$
- UIS Capability
- Qualified to AEC Q101
- RoHS Compliant

### Description

SuperFET® II MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently SuperFETII is very well suited for the Soft switching and Hard Switching topologies like High Voltage Full Bridge and Half Bridge DC-DC, Interleaved Boost PFC, Boost PFC for HEV-EV automotive.

SuperFET II FRFET® MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.



### Application

- Automotive On Board Charger
- Automotive DC/DC converter for HEV



### Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain to Source Voltage	650	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current - Continuous ( $V_{GS}=10$ ) (Note 1)	20.6	A
	Pulsed Drain Current	See Fig 4	A
$E_{AS}$	Single Pulse Avalanche Rating (Note 2)	400	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	50	
$P_D$	Power Dissipation	208	W
	Derate Above $25^\circ\text{C}$	1.67	
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to + 150	$^\circ\text{C}$
$R_{\theta JC}$	Maximum Thermal Resistance Junction to Case	0.6	$^\circ\text{C/W}$
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient (Note 4)	40	$^\circ\text{C/W}$

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCH190N65F	FCH190N65F-F085	TO-247	-	-	30

#### Notes:

- 1: Current is limited by bondwire configuration.
- 2: Starting  $T_J = 25^\circ\text{C}$ ,  $L = 50\text{mH}$ ,  $I_{AS} = 4\text{A}$ ,  $V_{DD} = 100\text{V}$  during inductor charging and  $V_{DD} = 0\text{V}$  during time in avalanche.
- 3:  $I_{SD} \leq 10\text{A}$ ,  $di/dt \leq 200\text{ A/us}$ ,  $V_{DD} \leq 380\text{V}$ , starting  $T_J = 25^\circ\text{C}$ .
- 4:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> pad of 2oz copper.

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

**Off Characteristics**

$B_{V_{DS}}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	650	-	-	V
$I_{DSS}$	Drain to Source Leakage Current	$V_{DS} = 650\text{V}, T_J = 25^\circ\text{C}$	-	-	10	$\mu\text{A}$
		$V_{GS} = 0\text{V}, T_J = 150^\circ\text{C}(\text{Note } 5)$	-	-	1	$\text{mA}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	$\text{nA}$

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	3.0	-	5.0	V
$r_{DS(on)}$	Drain to Source On Resistance	$I_D = 27\text{A}, T_J = 25^\circ\text{C}$	-	148	190	$\text{m}\Omega$
		$V_{GS} = 10\text{V}, T_J = 150^\circ\text{C}(\text{Note } 5)$	-	346	401	$\text{m}\Omega$

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	2447	3181	$\text{pF}$
$C_{oss}$	Output Capacitance		-	2345	3048	$\text{pF}$
$C_{rss}$	Reverse Transfer Capacitance		-	131	-	$\text{pF}$
$R_g$	Gate Resistance	$f = 1\text{MHz}$	-	0.5	-	$\Omega$
$Q_{g(ToT)}$	Total Gate Charge	$V_{DD} = 380\text{V}, I_D = 10\text{A}, V_{GS} = 10\text{V}$	-	63	82	$\text{nC}$
$Q_{g(th)}$	Threshold Gate Charge		-	4.3	5.6	$\text{nC}$
$Q_{gs}$	Gate to Source Gate Charge		-	12.6	-	$\text{nC}$
$Q_{gd}$	Gate to Drain "Miller" Charge		-	28	-	$\text{nC}$

**Switching Characteristics**

$t_{on}$	Turn-On Time	$V_{DD} = 380\text{V}, I_D = 10\text{A}, V_{GS} = 10\text{V}, R_G = 4.7\Omega$	-	40	100	$\text{ns}$
$t_{d(on)}$	Turn-On Delay Time		-	25	-	$\text{ns}$
$t_r$	Rise Time		-	14.5	-	$\text{ns}$
$t_{d(off)}$	Turn-Off Delay Time		-	64	-	$\text{ns}$
$t_f$	Fall Time		-	5	-	$\text{ns}$
$t_{off}$	Turn-Off Time		-	69	158	$\text{ns}$

**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 10\text{A}, V_{GS} = 0\text{V}$	-	-	1.2	V
$T_{rr}$	Reverse Recovery Time	$I_F = 10\text{A}, di_{SD}/dt = 100\text{A}/\mu\text{s}$	-	141	-	$\text{ns}$
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 520\text{V}$	-	889	-	$\text{nC}$

**Notes:**

5: The maximum value is specified by design at  $T_J = 150^\circ\text{C}$ . Product is not tested to this condition in production.

### Typical Characteristics

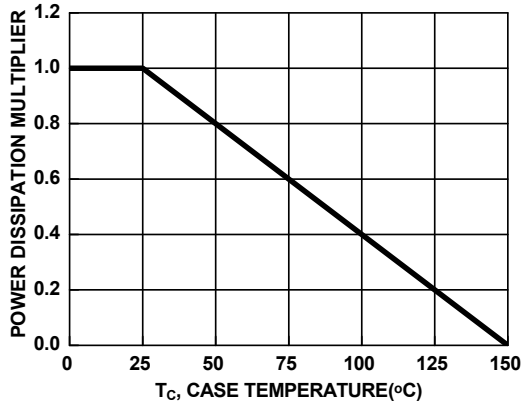


Figure 1. Normalized Power Dissipation vs. Case Temperature

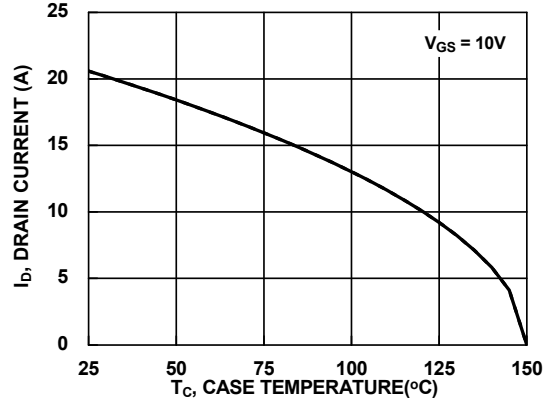


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

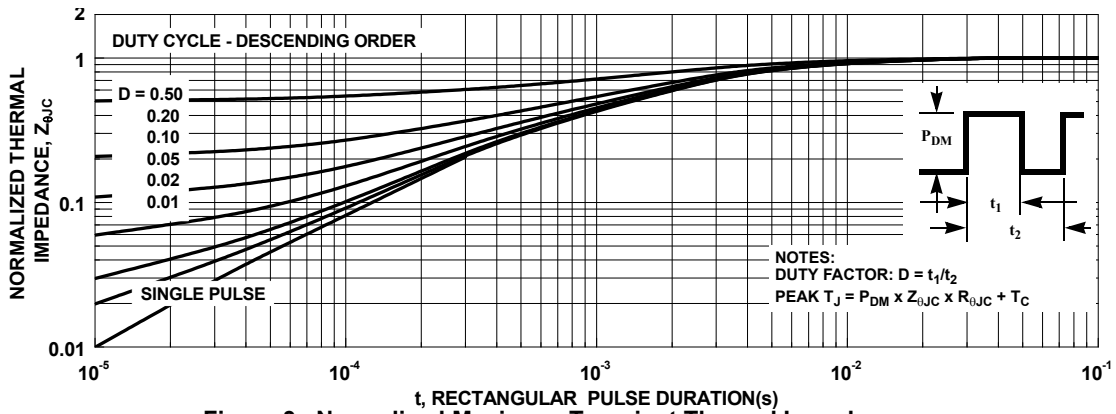


Figure 3. Normalized Maximum Transient Thermal Impedance

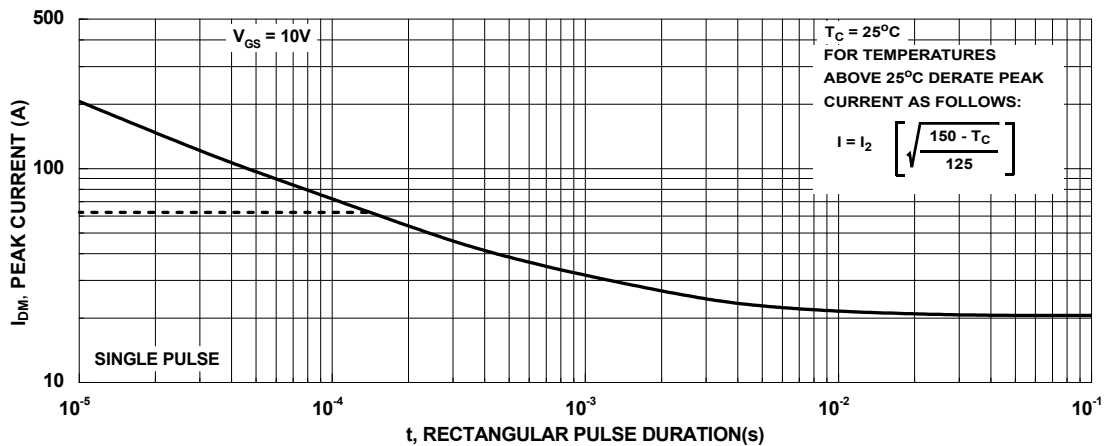


Figure 4. Peak Current Capability

## Typical Characteristics

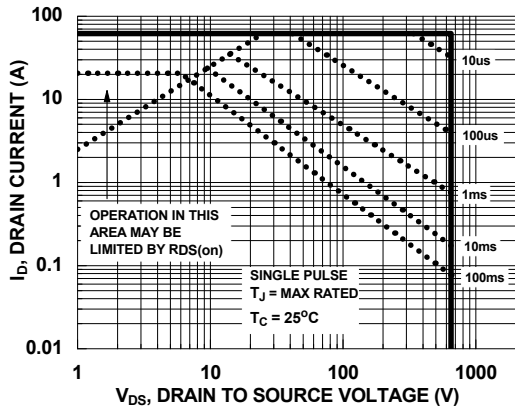


Figure 5. Forward Bias Safe Operating Area

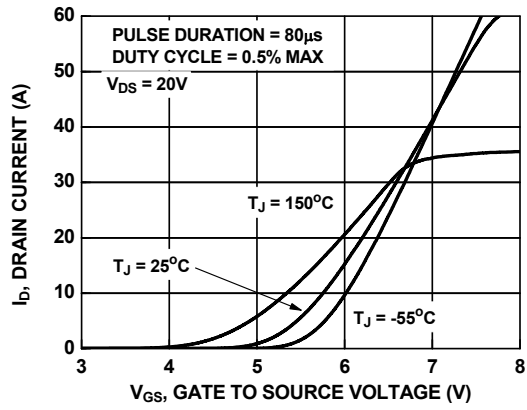


Figure 6. Transfer Characteristics

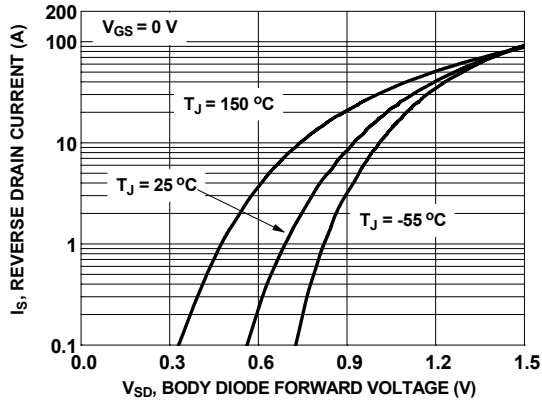


Figure 7. Forward Diode Characteristics

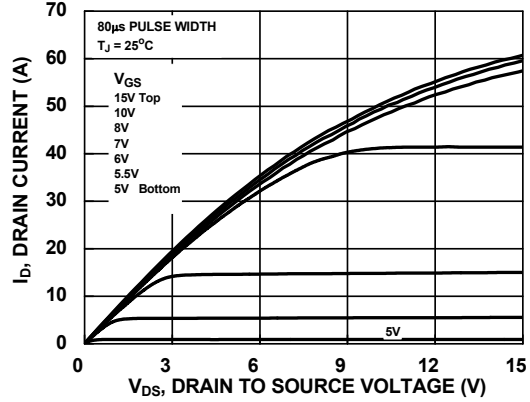


Figure 8. Saturation Characteristics

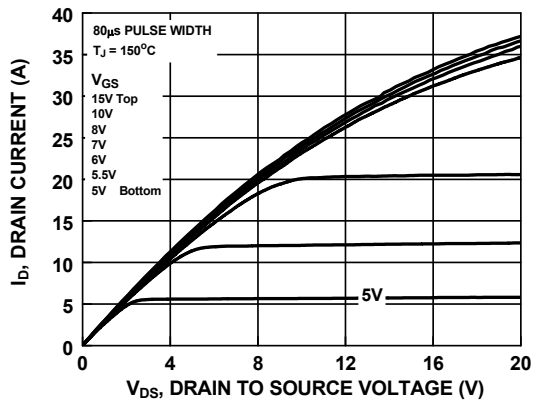


Figure 9. Saturation Characteristics

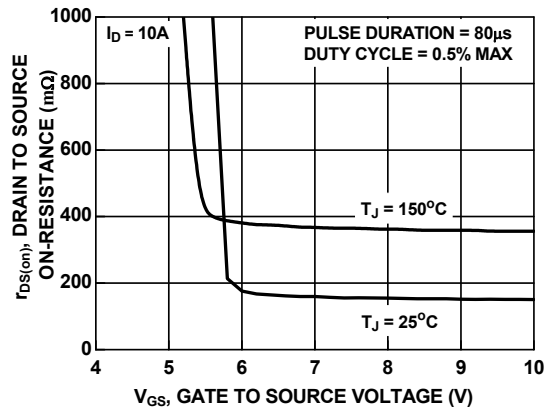


Figure 10.  $R_{DS(on)}$  vs. Gate Voltage

## Typical Characteristics

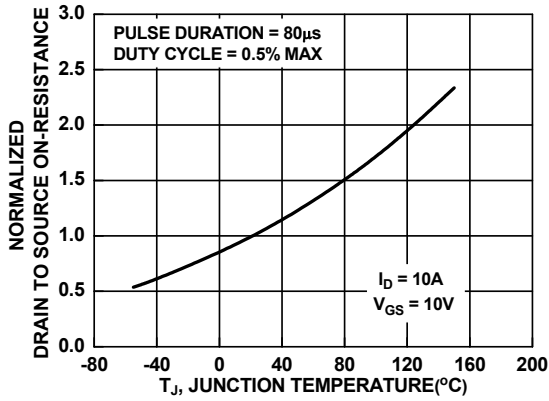


Figure 11. Normalized  $R_{DS(on)}$  vs. Junction Temperature

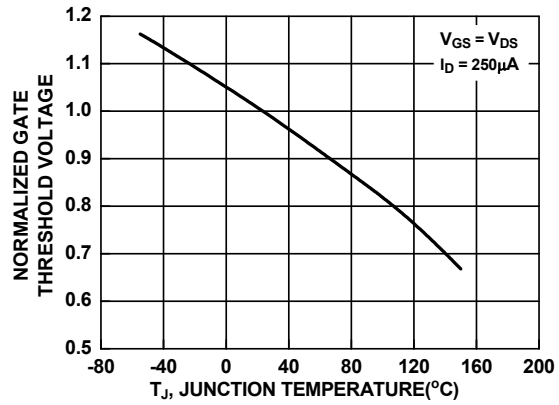


Figure 12. Normalized Gate Threshold Voltage vs. Temperature

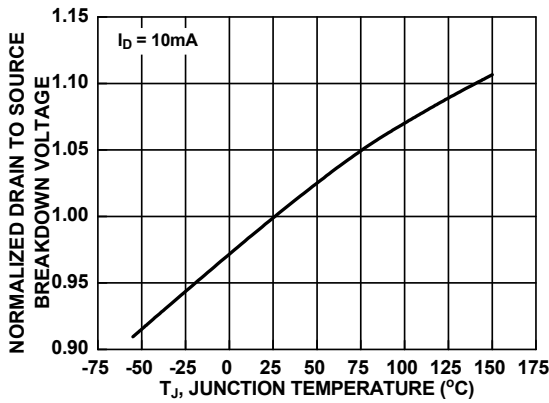


Figure 13. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

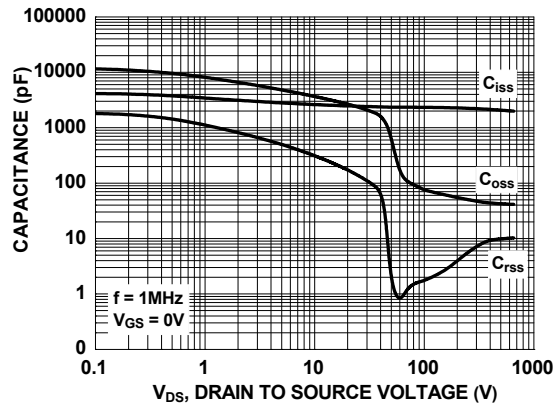


Figure 14. Capacitance vs. Drain to Source Voltage

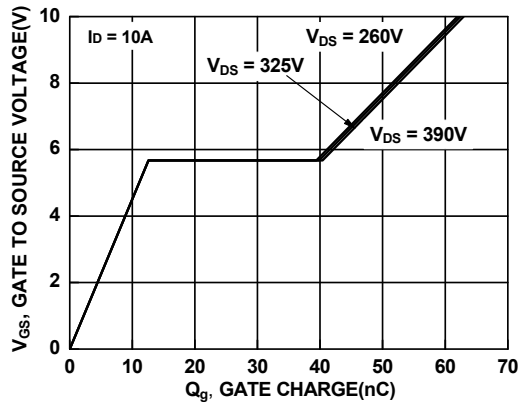


Figure 15. Gate Charge vs. Gate to Source Voltage

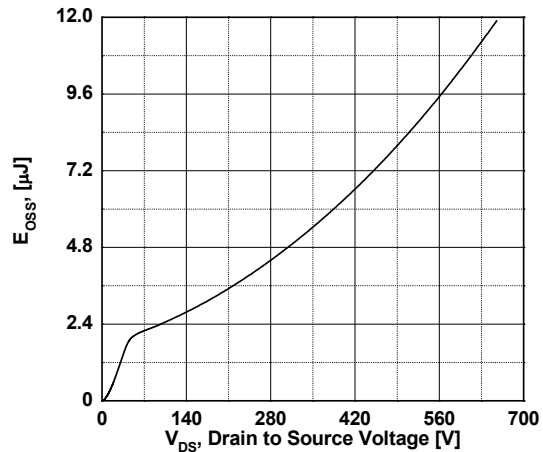


Figure 16.  $E_{oss}$  vs. Drain to Source Voltage

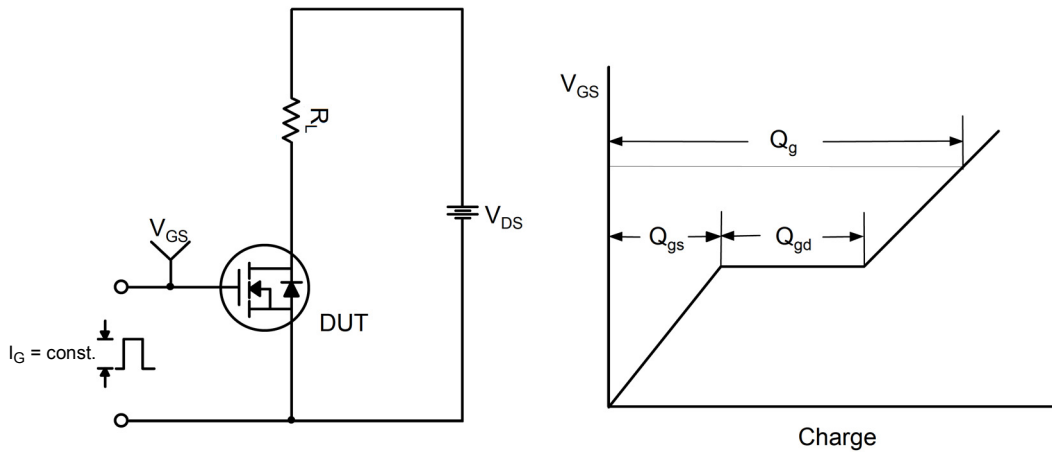


Figure 17. Gate Charge Test Circuit & Waveform

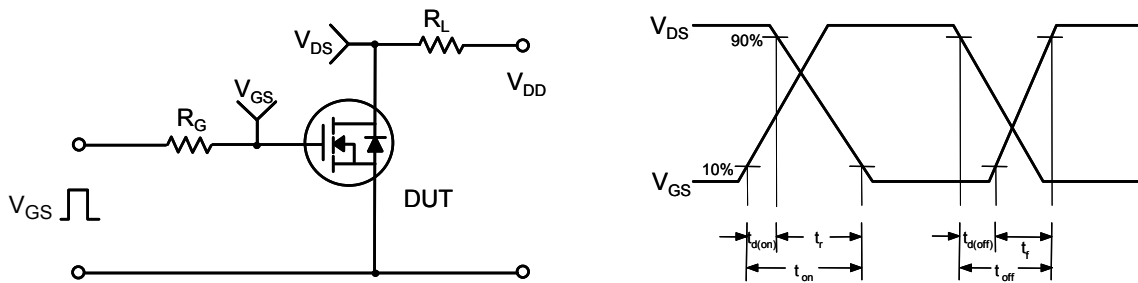


Figure 18. Resistive Switching Test Circuit & Waveforms

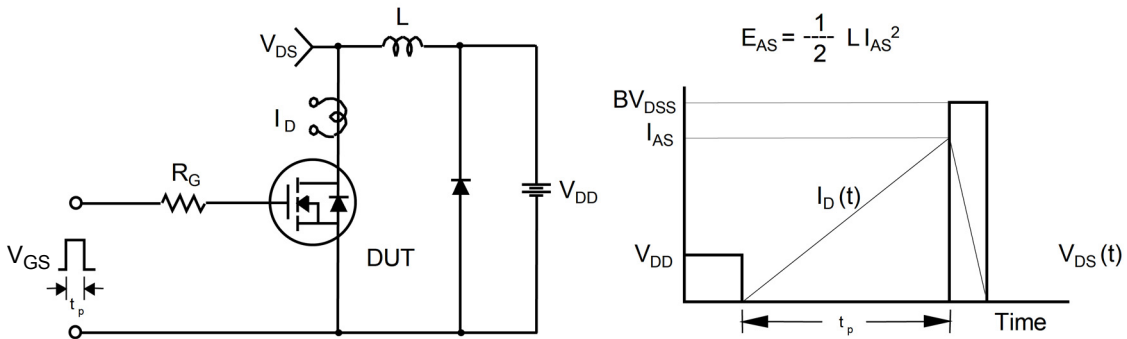


Figure 19. Unclamped Inductive Switching Test Circuit & Waveforms

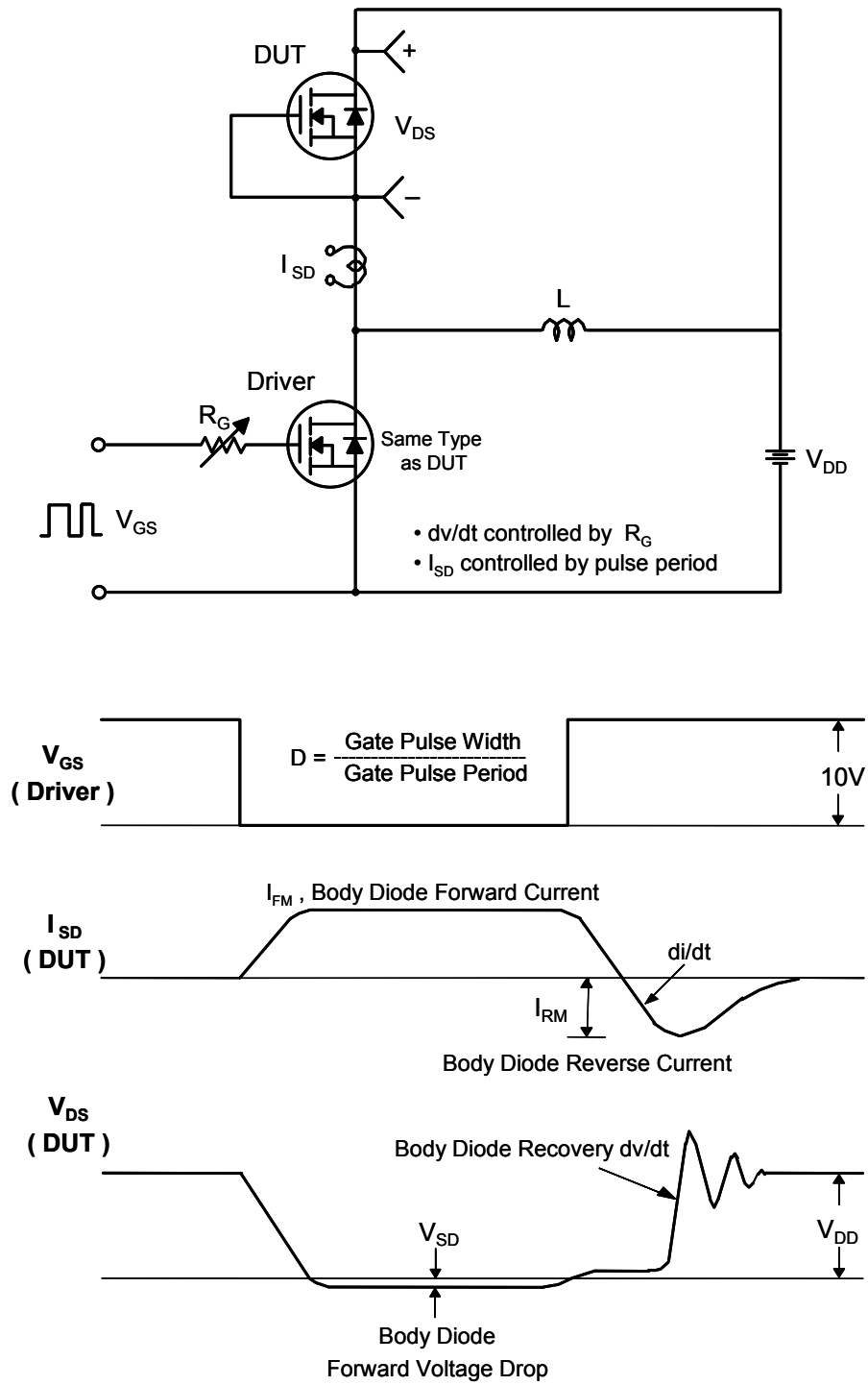
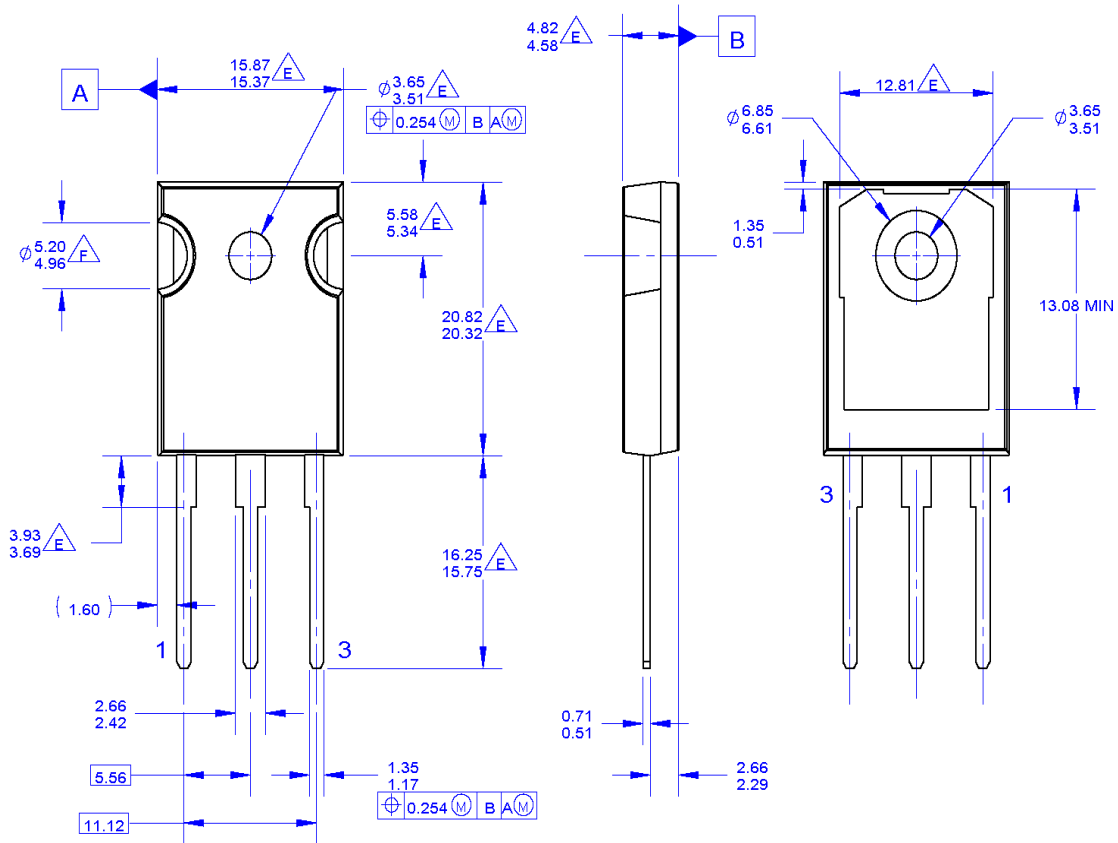


Figure 20. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. PACKAGE REFERENCE: JEDEC TO-247, ISSUE E, VARIATION AB, DATED JUNE, 2004.
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DRAWING CONFORMS TO ASME Y14.5 - 1994

$\triangle E$  DOES NOT COMPLY JEDEC STANDARD VALUE

$\triangle F$  NOTCH MAY BE SQUARE

G. DRAWING FILENAME: MKT-TO247A03\_REV03

**Figure 21. TO-247, Molded, 3-Lead, Jedec Variation AB**

Package drawings are provided as a service to customers considering ON Semiconductor components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a ON Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of ON Semiconductor's worldwide terms and conditions, specifically the warranty therein, which covers ON Semiconductor products.



ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local  
Sales Representative