

MOSFET - Power, N-Channel, SUPERFET[®] III, Easy-Drive

FCMT080N65S3 650 V, 80 mΩ, 38 A

General Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET Easy-drive series helps manage EMI issues and allows for easier design implementation.

The Power88 package is an ultra-slim surface-mount package (1 mm high) with a low profile and small footprint (8x8 mm²). SUPERFET III MOSFET in a Power88 package offers excellent switching performance due to lower parasitic source inductance and separated power and drive sources. Power88 offers Moisture Sensitivity Level 1 (MSL 1).

Features

- 700 V @ T_J = 150°C
- Typ R_{DS(on)} = 70 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 71 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 570 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

Applications

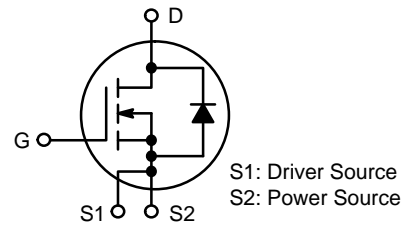
- Telecom / Server Power Supplies
- Industrial Power Supplies
- UPS / Solar



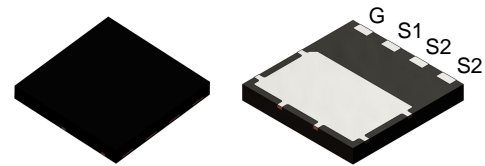
ON Semiconductor[®]

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V _{DSS}	R _{DS(ON)} MAX	I _D MAX
650 V	80 mΩ @ 10 V	38 A

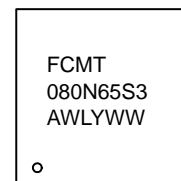


POWER MOSFET



Power88
TDFN4 8X8 2P
CASE 520AB

MARKING DIAGRAM



FCMT080N65S3 = Specific Device Code
 A = Assembly Location
 WL = Wafer Lot
 Y = Year
 WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FCMT080N65S3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, Unless otherwise specified)

Symbol	Parameter	FCMT080N65S3	Unit
V_{DSS}	Drain to Source Voltage	650	V
V_{GSS}	Gate to Source Voltage	DC	± 30
		AC ($f > 1\text{ Hz}$)	± 30
I_D	Drain Current	Continuous ($T_C = 25^\circ\text{C}$)	38
		Continuous ($T_C = 100^\circ\text{C}$)	24
I_{DM}	Drain Current	Pulsed (Note 1)	95
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	180	mJ
I_{AS}	Avalanche Current (Note 2)	4.6	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	2.6	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	20	
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	260
		Derate Above 25°C	2.08
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 s	300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $I_{AS} = 4.6\text{ A}$, $R_G = 25\ \Omega$ starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 19\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq 400\text{ V}$, starting $T_J = 25^\circ\text{C}$

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.48	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. (Note 4)	45	

4. Device on 1 in² pad 2 oz copper pad on 1.5 x 1.5 in. board of FR-4 material.

ORDERING INFORMATION

Device	Marking	Package	Reel Size	Tape Width	Quantity [†]
FCMT080N65S3	FCMT080N65S3	Power 88	13"	13.3 mm	3000 Units

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

FCMT080N65S3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	650	–	–	V
		$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 150^\circ\text{C}$	700	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 1\text{ mA}$, Referenced to 25°C	–	0.63	–	V/ $^\circ\text{C}$
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	–	–	10	μA
		$V_{DS} = 520\text{ V}, T_C = 125^\circ\text{C}$	–	3.0	–	
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	–	–	± 100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 0.88\text{ mA}$	2.5	–	4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 19\text{ A}$	–	70	80	m Ω
g _{FS}	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 19\text{ A}$	–	21	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	–	2765	–	pF
C _{oss}	Output Capacitance		–	65	–	pF
C _{oss(eff.)}	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	–	570	–	pF
C _{oss(er.)}	Energy Related Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	–	94	–	pF
Q _{g(tot)}	Total Gate Charge at 10V	$V_{DS} = 400\text{ V}, I_D = 19\text{ A}, V_{GS} = 10\text{ V}$ (Note 5)	–	71	–	nC
Q _{gs}	Gate to Source Gate Charge		–	16	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	29	–	nC
ESR	Equivalent Series Resistance	$f = 1\text{ MHz}$	–	0.55	–	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	$V_{DD} = 400\text{ V}, I_D = 19\text{ A},$ $V_{GS} = 10\text{ V}, R_g = 4.7\ \Omega$ (Note 5)	–	24	–	ns
t _r	Turn-On Rise Time		–	28	–	ns
t _{d(off)}	Turn-Off Delay Time		–	71	–	ns
t _f	Turn-Off Fall Time		–	5.4	–	ns

SOURCE-DRAIN DIODE CHARACTERISTICS

I _S	Maximum Continuous Source to Drain Diode Forward Current	–	–	38	A	
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current	–	–	95	A	
V _{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 19\text{ A}$	–	–	1.2	V
t _{rr}	Reverse Recovery Time	$V_{DD} = 400\text{ V}, I_{SD} = 19\text{ A},$ $di_F/dt = 100\text{ A}/\mu\text{s}$	–	405	–	ns
Q _{rr}	Reverse Recovery Charge		–	7.7	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

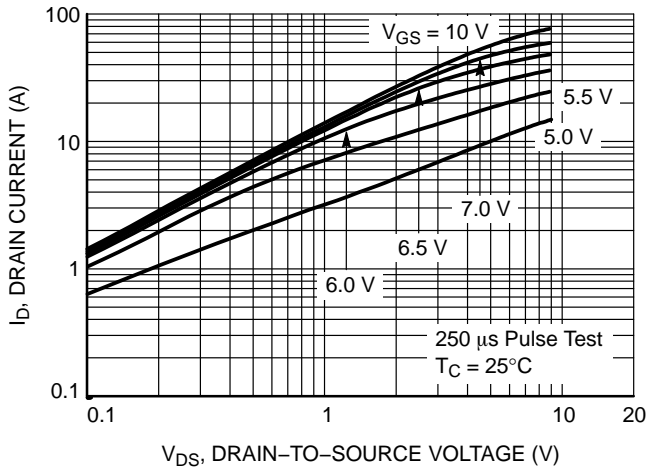


Figure 1. On-Region Characteristics

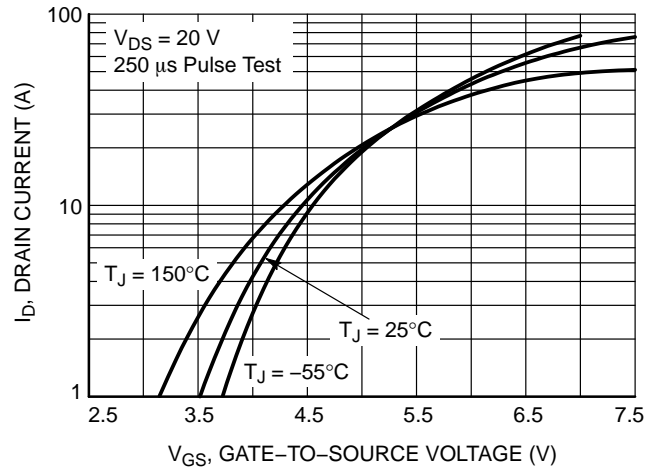


Figure 2. Transfer Characteristics

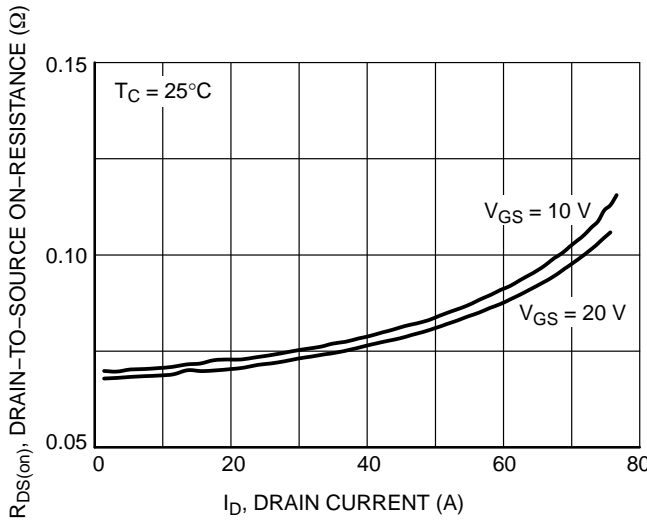


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

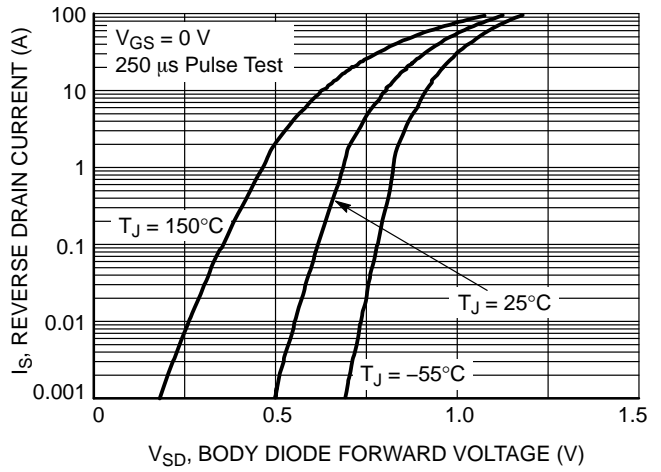


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

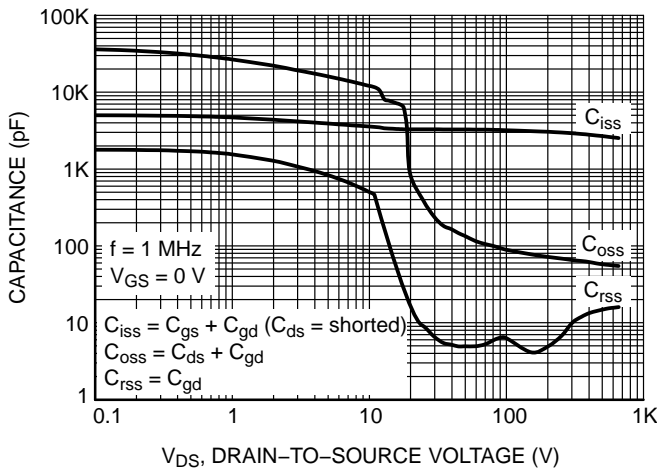


Figure 5. Capacitance Characteristics

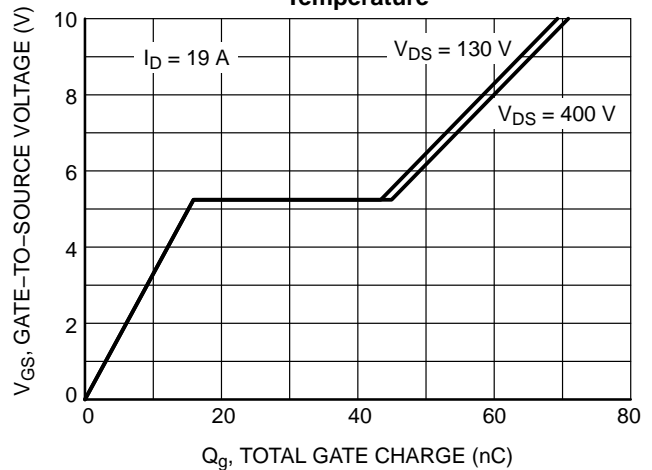


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

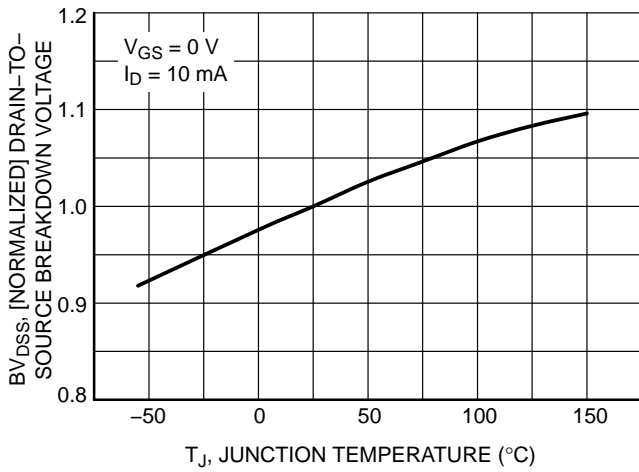


Figure 7. Breakdown Voltage Variation vs. Temperature

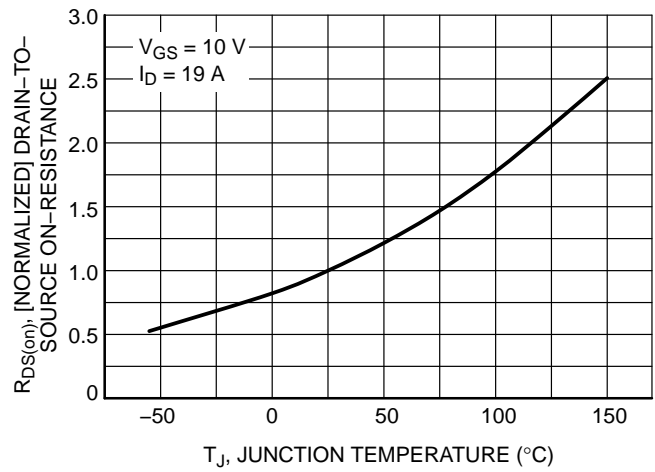


Figure 8. On-Resistance Variation vs. Temperature

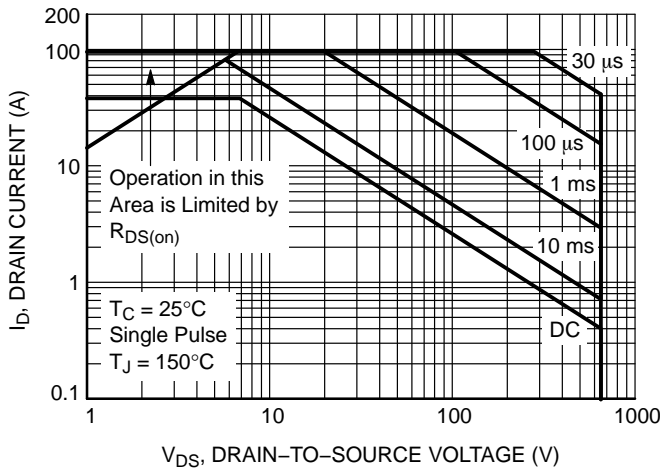


Figure 9. Maximum Safe Operating Area

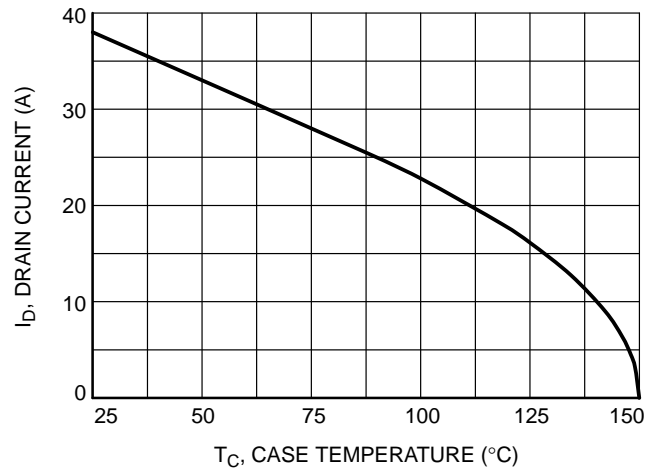


Figure 10. Maximum Drain Current vs. Case Temperature

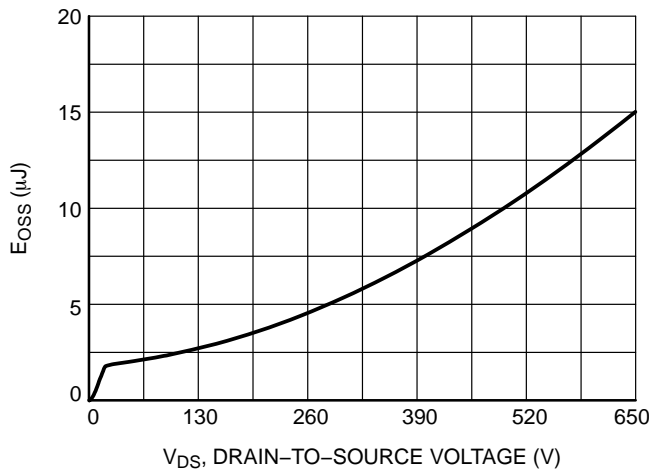


Figure 11. E_{OSS} vs. Drain-to-Source Voltage

FCMT080N65S3

TYPICAL CHARACTERISTICS

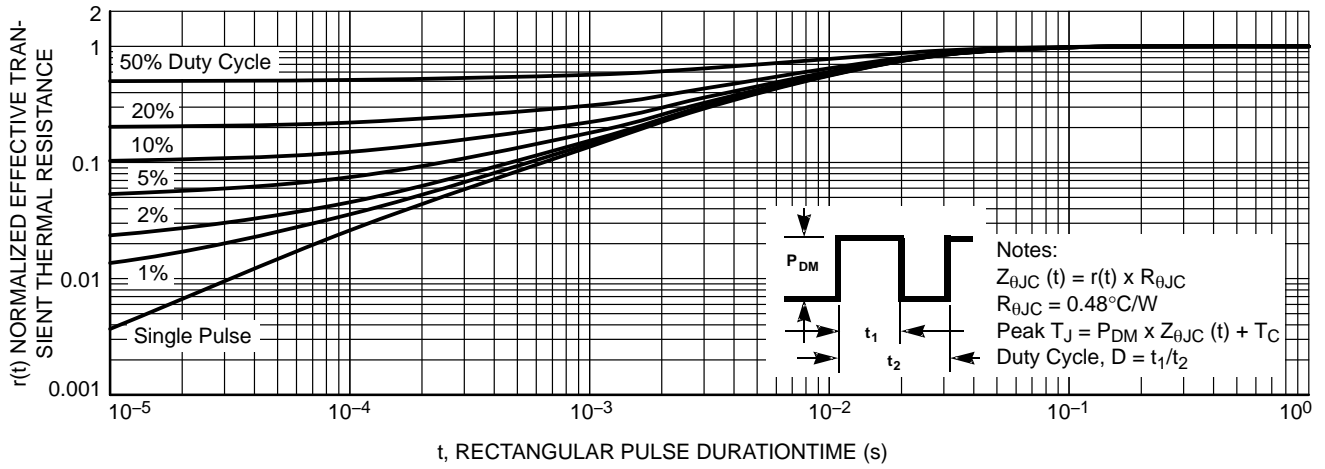


Figure 12. Transient Thermal Response Curve

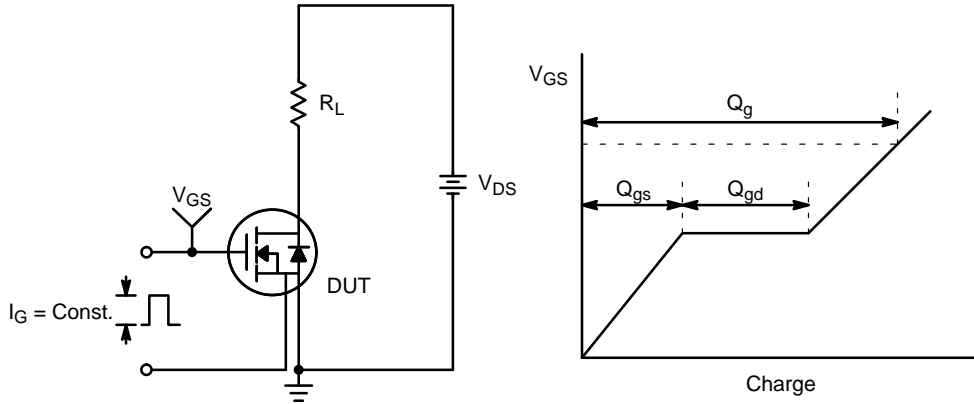


Figure 13. Gate Charge Test Circuit & Waveform

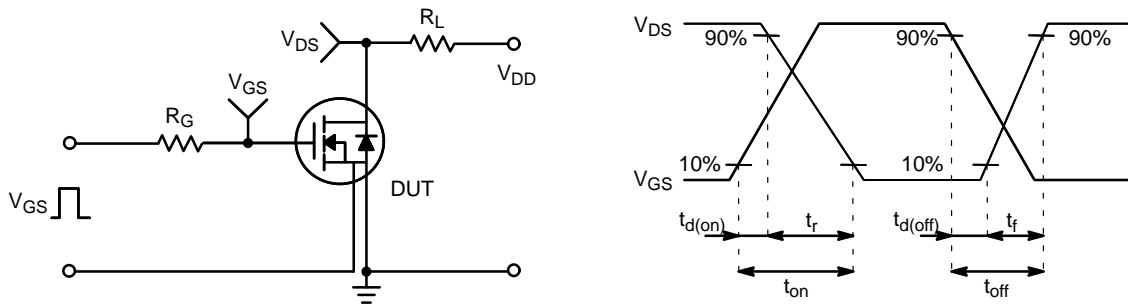


Figure 14. Resistive Switching Test Circuit & Waveforms

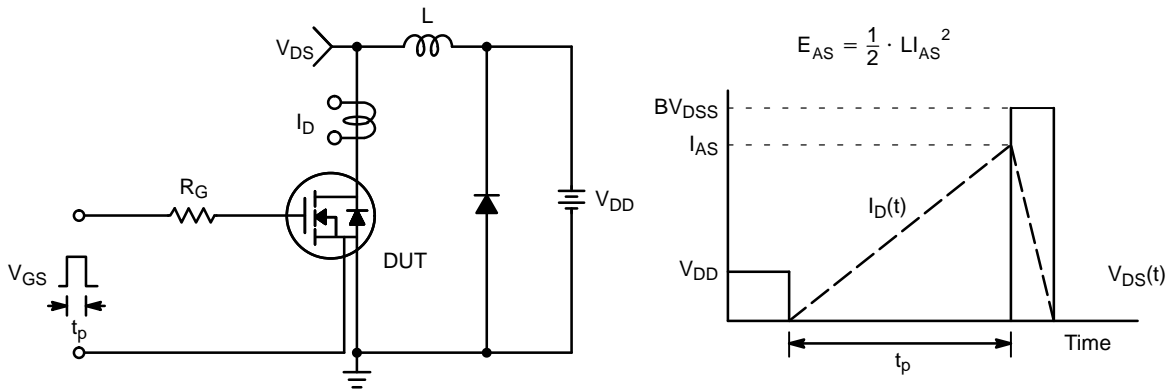


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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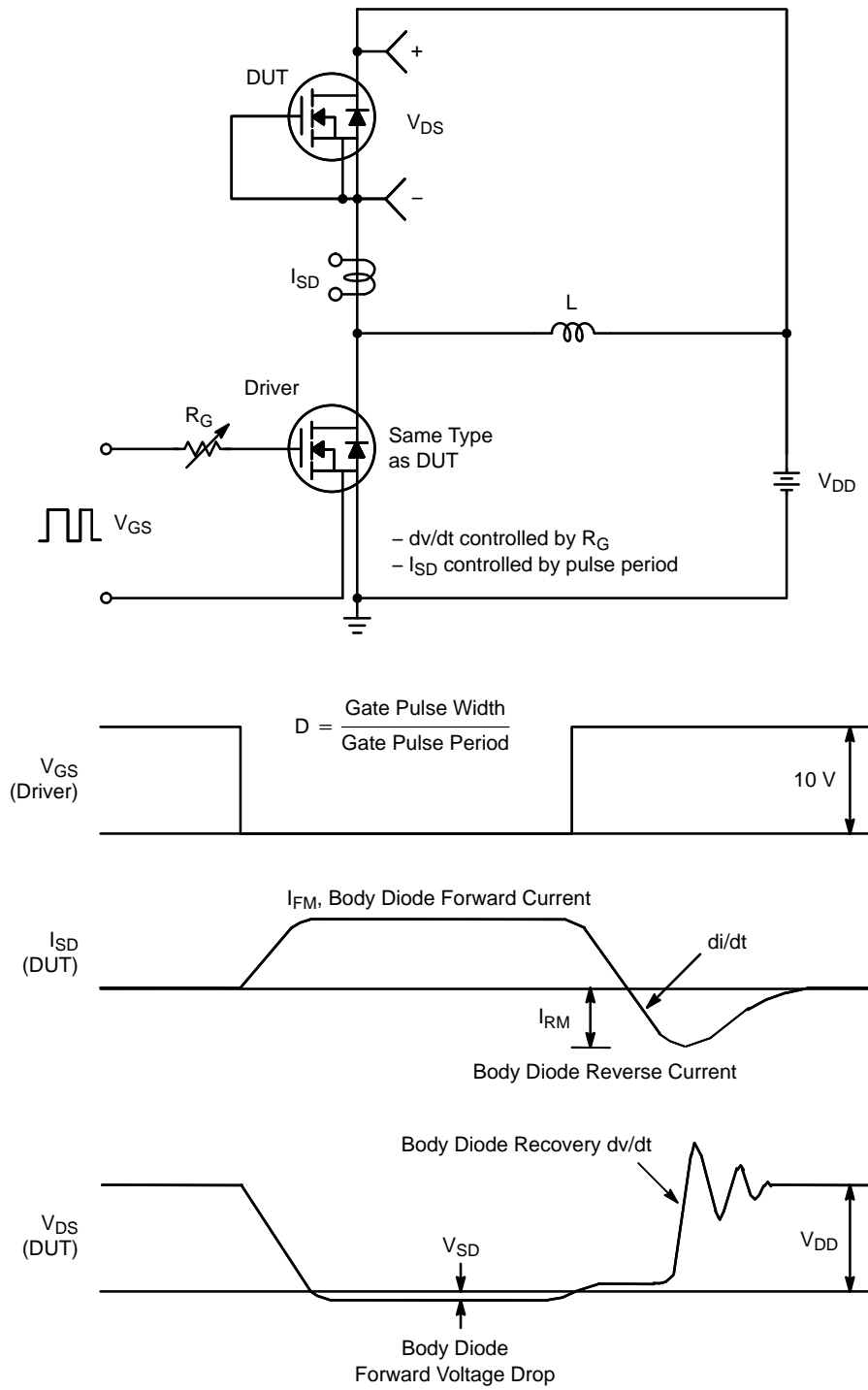
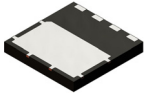


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE

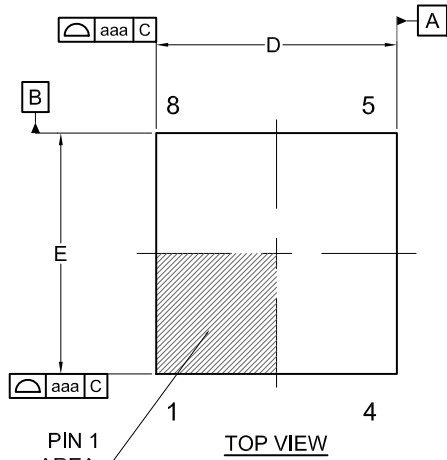
PACKAGE DIMENSIONS

ON Semiconductor®

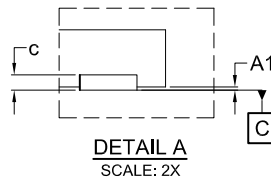


TDFN4 8x8, 2P
CASE 520AB
ISSUE O

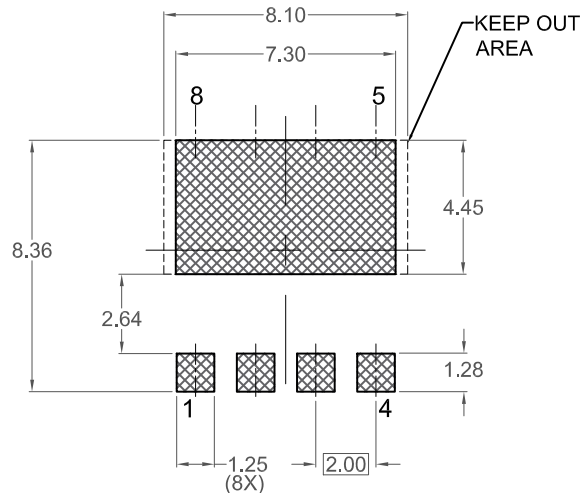
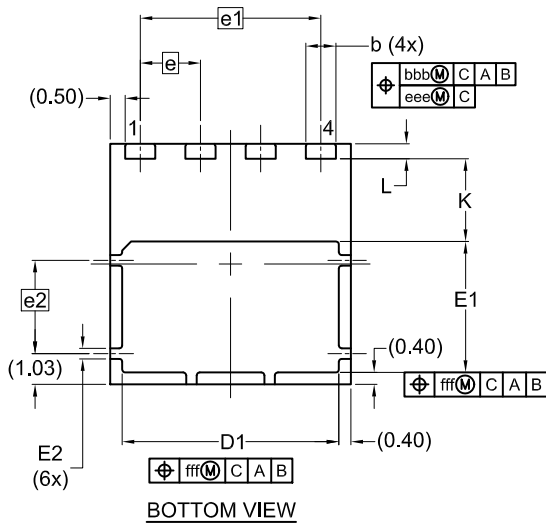
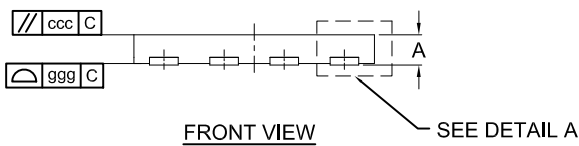
DATE 24 APR 2019



NOTES: UNLESS OTHERWISE SPECIFIED
 A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-220.
 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
 D) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



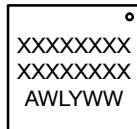
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.90	1.00	1.10
c	0.10	0.20	0.30
D	7.90	8.00	8.10
D1	7.10	7.20	7.30
E	7.90	8.00	8.10
E1	4.25	4.35	4.45
E2	0.15	0.25	0.35
e	2.00 BSC		
e1	6.00 BSC		
e2	3.10 BSC		
K	(2.75)		
L	0.40	0.50	0.60
aaa	0.10		
bbb	0.10		
ccc	0.05		
eee	0.05		
fff	0.10		
ggg	0.15		



RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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