

FCU900N65S3Z

Product Preview

Power MOSFET, N-Channel, SUPERFET[®] III, Easy-Drive

650 V, 4.5 A, 900 mΩ

Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provides superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET Easy-drive series helps manage EMI issues and allows for easier design implementation.

Features

- 700 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 647\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 7\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 105\text{ pF}$)
- ESD Improved Capability
- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

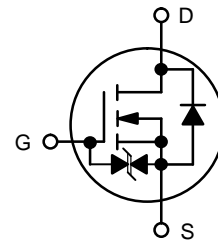
- Computing / Display Power Supplies
- Telecom / Server Power Supplies
- Industrial Power Supplies
- Lighting / Charger / Adapter



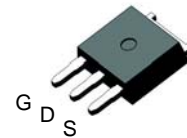
ON Semiconductor[®]

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V_{DSS}	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
650 V	900 mΩ @ 10 V	4.5 A

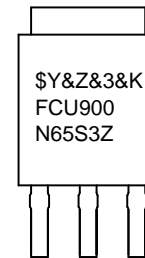


N-Channel MOSFET



IPAK
CASE 369AP

MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
FCU900N65S3Z	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

FCU900N65S3Z

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter	FCU900N65S3Z	Unit
V _{DSS}	Drain to Source Voltage	650	V
V _{GSS}	Gate to Source Voltage	- DC	±25
		- AC (f > 1 Hz)	±25
I _D	Drain Current:	- Continuous (T _C = 25°C)	4.5
		- Continuous (T _C = 100°C)	2.0
I _{DM}	Drain Current:	- Pulsed (Note 1)	11.3
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	TBD	mJ
I _{AS}	Avalanche Current (Note 2)	TBD	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	TBD	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	20	
P _D	Power Dissipation	(T _C = 25°C)	38
		Derate Above 25°C	0.30
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = TBD A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 1.75 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	FCU900N65S3Z	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	3.1	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max.	62.5	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
FCU900N65S3Z	FCU900N65S3Z	IPAK	Tube	N/A	N/A	75 Units

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	650	–	–	V
		V _{GS} = 0 V, I _D = 1 mA, T _J = 150°C	700	–	–	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25°C	–	0.64	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V	–	–	1	μA
		V _{DS} = 520 V, T _C = 125°C	–	0.2	–	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±25 V, V _{DS} = 0 V	–	–	±10	μA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 50 μA	2.5	–	4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 2.25 A	–	647	900	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 2.25 A	–	2.7	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 1 MHz	–	424	–	pF
C _{oss}	Output Capacitance		–	9.0	–	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	–	105	–	pF
C _{oss(er.)}	Energy Related Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	–	13.5	–	pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 400 V, I _D = 2.25 A, V _{GS} = 10 V (Note 4)	–	7.0	–	nC
Q _{gs}	Gate to Source Gate Charge		–	2.0	–	nC
Q _{gd}	Gate to Drain “Miller” Charge		–	4.0	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	TBD	–	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 400 V, I _D = 2.25 A, V _{GS} = 10 V, R _g = 4.7 Ω (Note 4)	–	5.0	–	ns
t _r	Turn-On Rise Time		–	6.0	–	ns
t _{d(off)}	Turn-Off Delay Time		–	21	–	ns
t _f	Turn-Off Fall Time		–	2.0	–	ns

SOURCE-DRAIN DIODE CHARACTERISTICS

I _S	Maximum Continuous Source to Drain Diode Forward Current	–	–	4.5	A	
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current	–	–	11.3	A	
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 2.25 A	–	–	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 2.25 A, dI _F /dt = 100 A/μs	–	204	–	ns
Q _{rr}	Reverse Recovery Charge		–	1.2	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

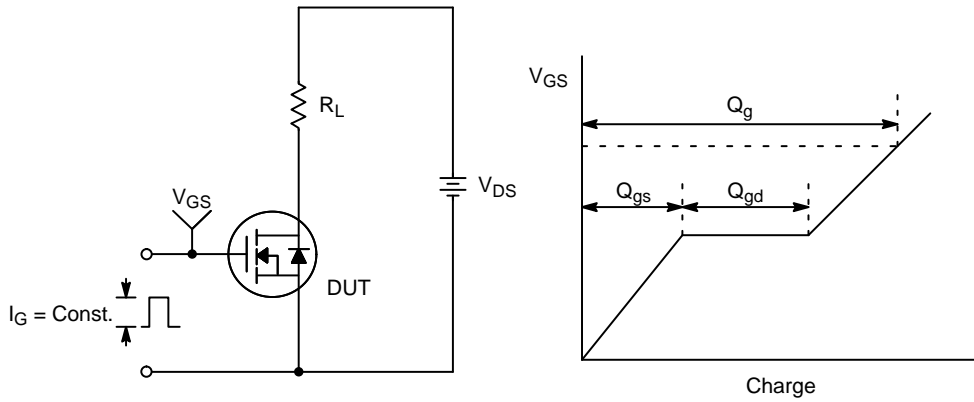


Figure 1. Gate Charge Test Circuit & Waveform

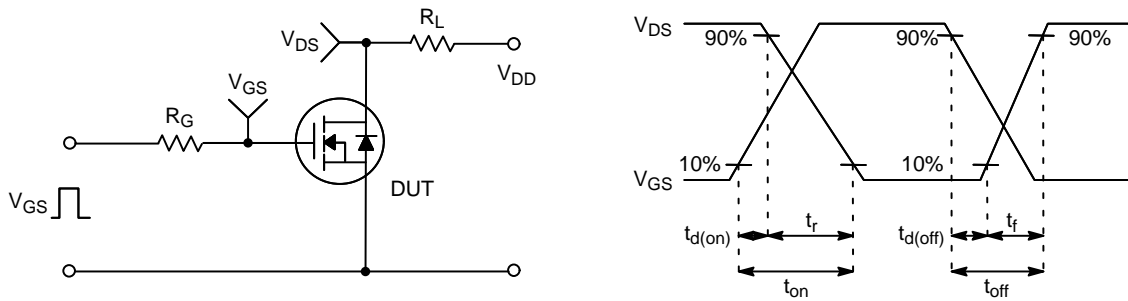


Figure 2. Resistive Switching Test Circuit & Waveforms

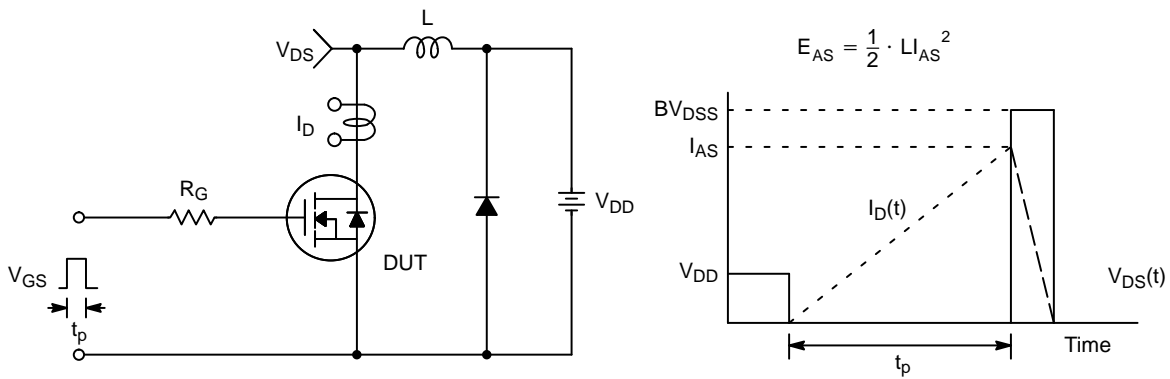


Figure 3. Unclamped Inductive Switching Test Circuit & Waveforms

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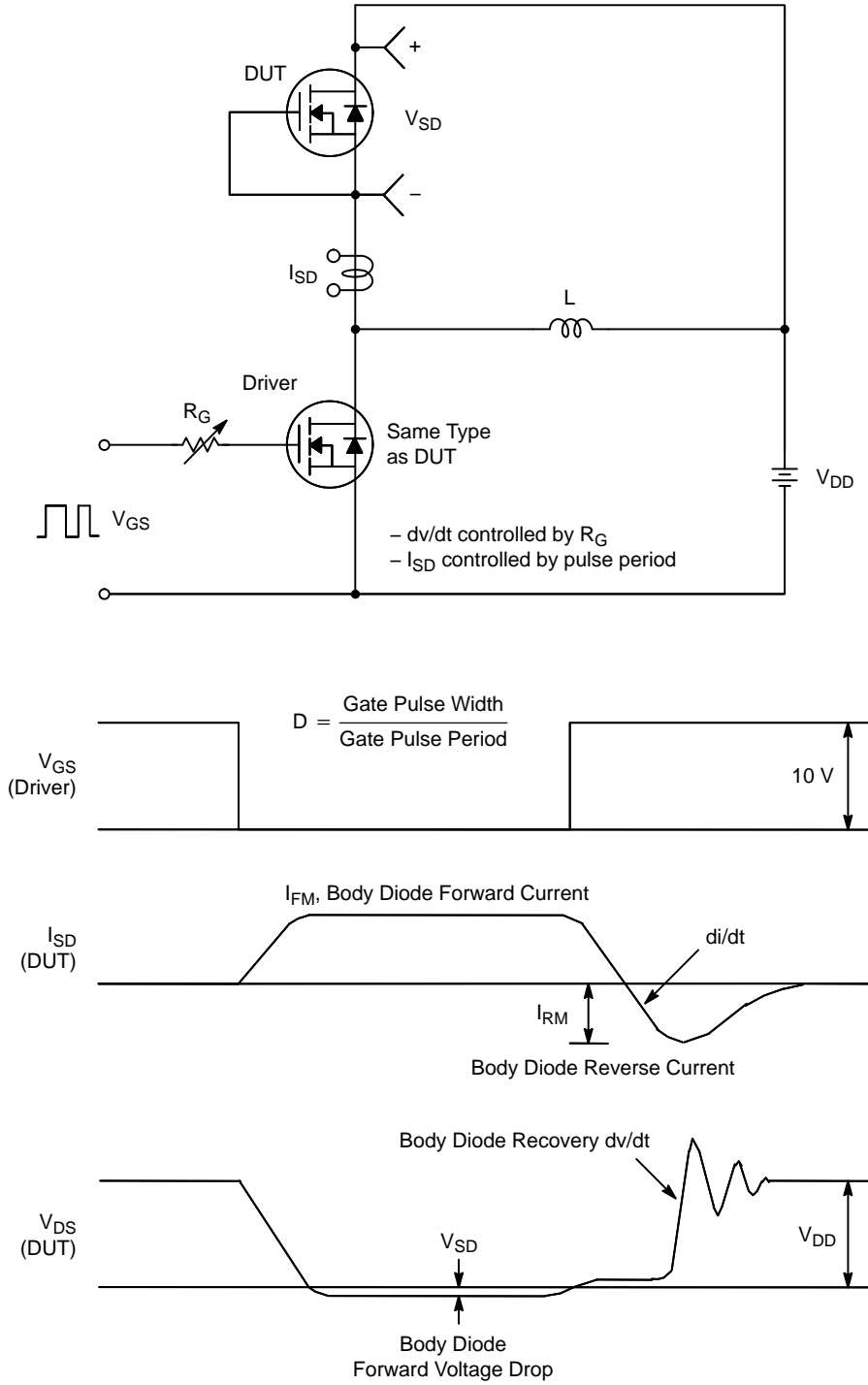


Figure 4. Peak Diode Recovery dv/dt Test Circuit & Waveforms

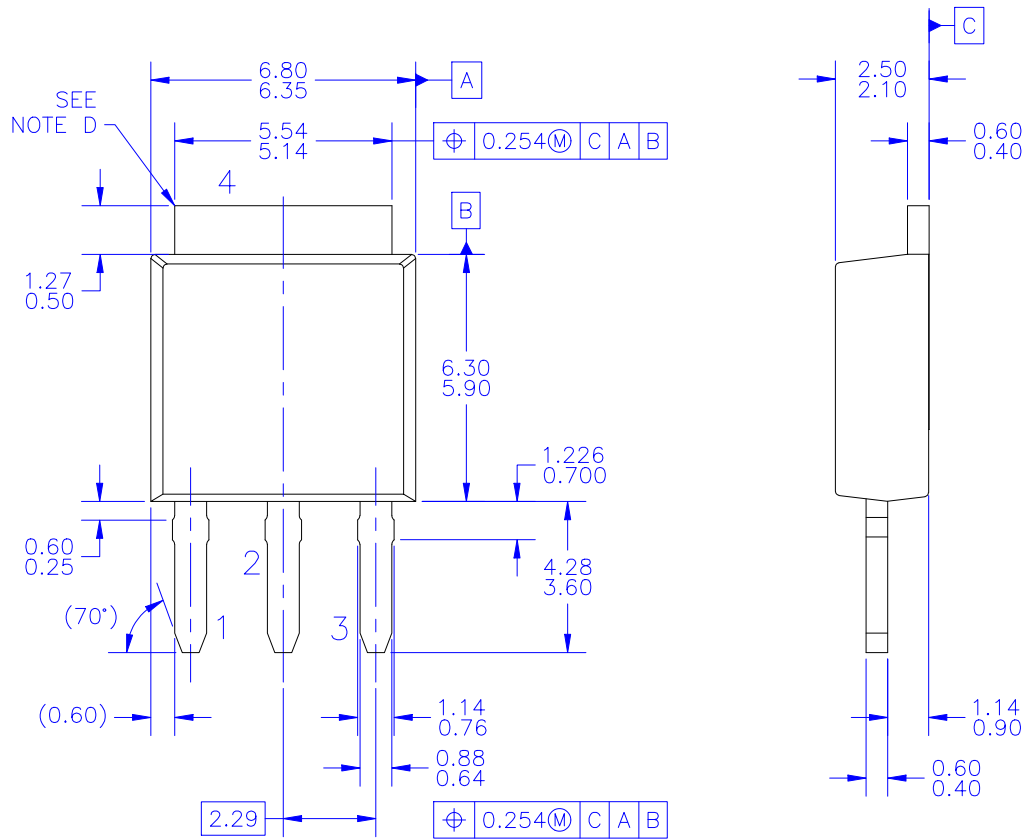
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PACKAGE DIMENSIONS

DPAK3 (STRAIGHT LEADS)

CASE 369AP


ISSUE O



NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) PACKAGE BODY REFERENCE: JEDEC, TO-251, ISSUE D, VARIATION AA, DATED JUNE 2002.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.

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