Power MOSFET, Single P-Channel

–40 V, –83 A, 8.0 m Ω

Features

- Low R_{DS(on)} to Minimize Conduction Losses
- Low QG and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			VDSS	-40	٧
Gate-to-Source Voltage			Vgs	±16	٧
Continuous Drain	Steady State	T _C = 25°C	I _D	-83	А
Current R _{0JC} (Notes 1, 3)		T _C = 100°C		-59	
Power Dissipation		T _C = 25°C		93.8	w
R _{θJC} (Note 1)		$T_C = 100^{\circ}C$	P_{D}	46.9	
Continuous Drain Current R _{θJA} (Notes 1, 2, 3)	Steady State	T _C = 25°C	I _D	-16.1	А
		T _C = 100°C		-11.4	
Power Dissipation		T _C = 25°C	P _D	3.5	w
R _{θJA} (Notes 1 & 2)		$T_C = 100^{\circ}C$		1.7	
Pulsed Drain Current $T_C = 25^{\circ}C$, $t_p = 10 \mu s$			Ірм	-669	Α
Operating Junction and Storage Temperature			TJ, Tstg	–55 to +175	°C
Source Current (Body Diode)			I _S	-80	Α
Single Pulse Drain-to-Source Avalanche Energy (IL(pk) = -64)			Eas	82	mJ
Lead Temperature for Soldering Purposes (1/83 from case for 10 s)			TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{ heta JC}$	1.6	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	43	°C/W

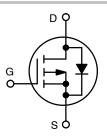
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
- 3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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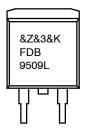
V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX	
-40 V	8.0 mΩ @ –10 V	-83 A	
	12.5 mΩ @ -4.5 V	007.	





D²PAK-3 (TO-163AB) CASE 418AJ

MARKING DIAGRAM



&Z = Assembly Plant Code &3 = Numeric Date Code

&K = Lot Code

FDB9509L= Specific Device Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 6 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
Off Characteristics							
Drain to Source Breakdown Voltage	V(BR)DSS	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$		-40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V(BR)DSS/ T _J				20		mV/°C
Zero Gate Voltage Drain Current	IDSS		T _J = 25°C			-1	μА
		$V_{GS} = 0 \text{ V}, V_{DS} = -40 \text{ V}$	T _J = 175°C			-1	mA
Zero Gate Voltage Drain Current	Igss	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 16 \text{ V}$				±100	nA
On Characteristics (Note 4)	•				•	•	•
Gate Threshold Voltage	VGS(TH)	V _{GS} = V _{DS} , I _D = -250 μA		-1	-1.7	-3	V
Threshold Temperature Coefficient	Vgs(TH)/TJ				-5		mV/°C
Drain-to-Source On Resistance	RDS(on)	V _{GS} = -10 V	I _D = -80 A		6.4	8.0	mΩ
		V _{GS} = -4.5 V	I _D = -40 A		9.6	12.5	1
Charges, Capacitances & Gate Resis	stance					1	
Input Capacitance	Ciss	V _{GS} = 0 V, f = 1 MHz, V	/ _{DS} = -20 V		3400		pF
Output Capacitance	Coss				1250		pF
Reverse Transfer Capacitance	Crss				39		pF
Gate Resistance	R_{g}	V _{GS} = 0.5 V, f = 100 kHz			21		Ω
Total Gate Charge	QG(TOT)	$V_{GS} = -10 \text{ V}, V_{DS} = -32 \text{ V}; I_D = -80 \text{ A}$ $V_{GS} = -4.5 \text{ V}, V_{DS} = -32 \text{ V}; I_D = -80 \text{ A}$			48		nC
					22		
Threshold Gate Charge	Qg(th)	V _{GS} = 0 to -1 V			6		
Gate to Source Gate Charge	Qgs	V _{DD} = -32 V _, I _D = -80 A			12		
Gate to Drain "Miller" Charge	Qgd				5		
Plateau Voltage	VGP				-3.5		V
Switching Characteristics						•	
Turn-On Delay Time	td(ON)	$V_{DD} = -20 \text{ V}, I_D = -80 \text{ A}, V_{GS} = -10 \text{ V}, R_{GEN} = 6 \Omega$			9		ns
Turn-On Rise Time	t _r	GG 1-1, FGE	V		4		ns
Turn-Off Delay Time	td(OFF)				200		ns
Turn-Off Fall Time	t _f	1			57		ns
Drain-Source Diode Characteristics		I.			I	1	
Source to Drain Diode Voltage	VsD	I _{SD} = -80 A, V _{GS}	= 0 V		-0.98	-1.25	V
		I _{SD} = -40 A, V _{GS}			-0.9	-1.2	V
Reverse Recovery Time	TRR	$V_{GS} = 0 \text{ V}, dI_{SD}/dt = 100 \text{ A/us}, I_{S} = -80 \text{ A}$			78		ns
Charge Time	t _a	1			33		=
Discharge Time	t _b	1			46		1
Reverse Recovery Charge	QRR	1			95		nC
	1						1

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300~\mu s$, duty cycle $\leq 2\%$ 5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

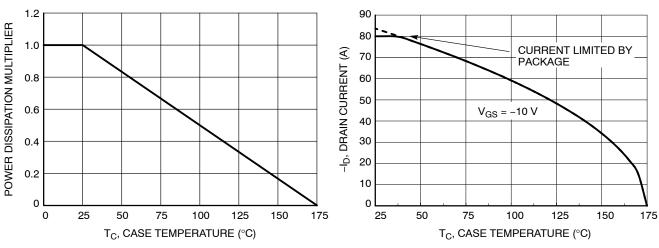


Figure 1. Normalized Power Dissipation vs.

Case Temperature

Figure 2. Maximum Continuous Drain Current vs. Case Temperature

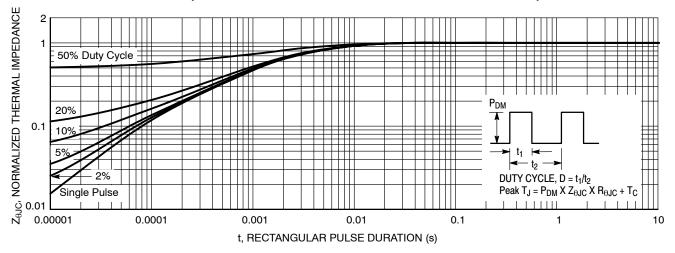


Figure 3. Normalized Maximum Transient Thermal Impedance

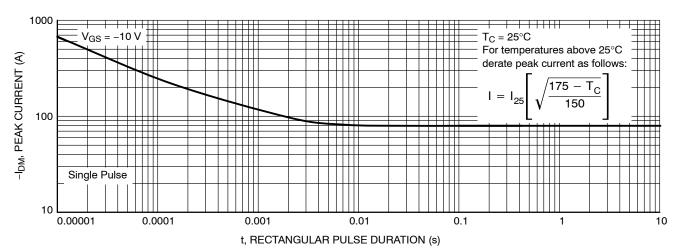


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

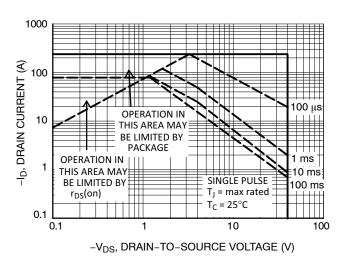
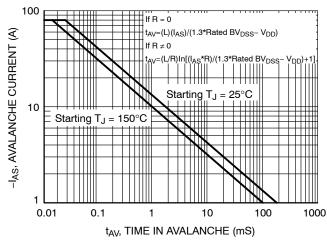


Figure 5. Forward Bias Safe Operating Area



Note: Refer to ON Semiconductor Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

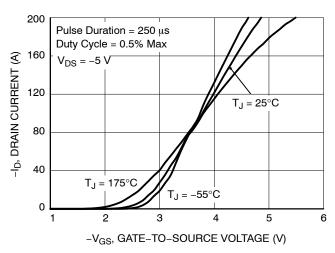


Figure 7. Transfer Characteristics

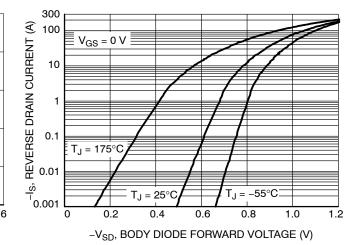


Figure 8. Forward Diode Characteristics

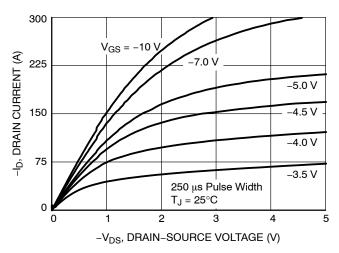


Figure 9. Saturation Characteristics

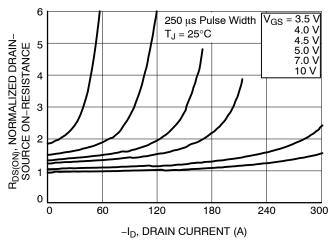


Figure 10. Normalized R_{DS(ON)} vs. Drain Current

TYPICAL CHARACTERISTICS

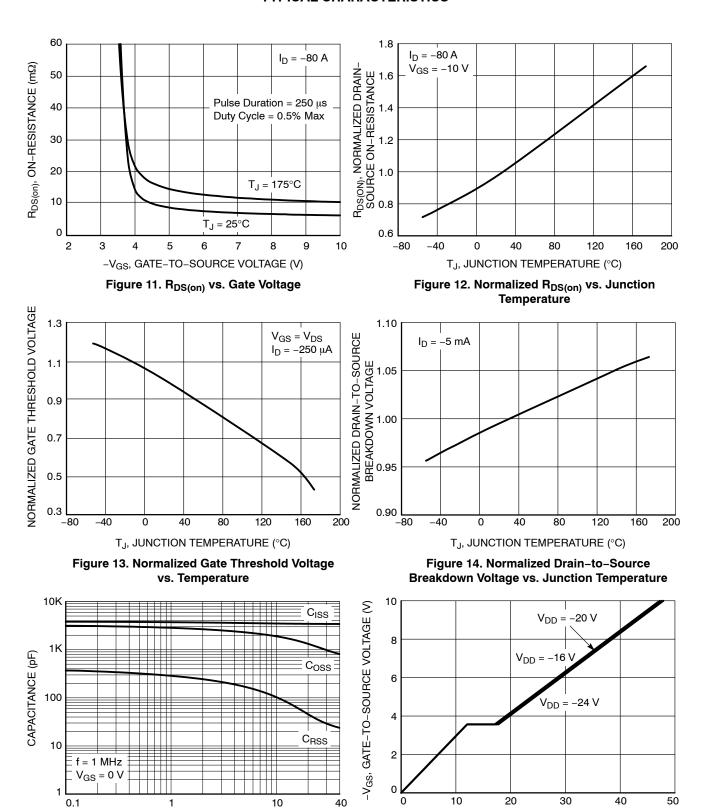


Figure 15. Capacitance vs. Drain-to-Source Voltage

-V_{DS}, DRAIN-TO-SOURCE VOLTAGE (V)

Q_g, GATE CHARGE (nC)

Figure 16. Gate Charge vs. Gate-to-Source

Voltage

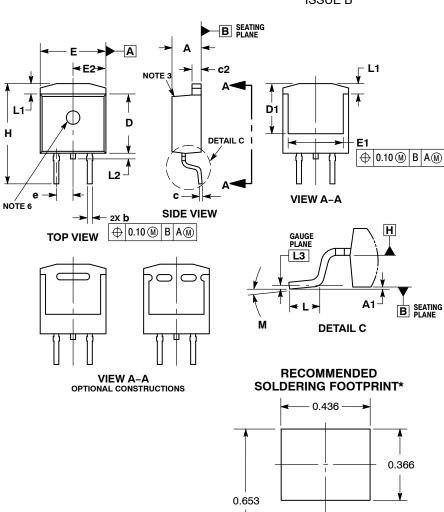
ORDERING INFORMATION

Device	Device Marking	Package	Shipping [†]
FDB9509L-F085	FDB9509L	D ² PAK-3 (Pb-Free, Halogen Free)	3,000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

PACKAGE DIMENSIONS

D²PAK-3 (TO-263, 3-LEAD) CASE 418AJ **ISSUE B**



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: INCHES.

- 2. CONTROLLING DIMENSION: INCHES.
 3. CHAMFER OPTIONAL
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
 5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1 AND E1.
 6. OPTIONAL MOLD FEATURE

	INC	HES	MILLIMETERS			
DIM	MIN	MAX	MIN	MAX		
Α	0.160	0.190	4.06	4.83		
A 1	0.000	0.010	0.00	0.25		
q	0.020	0.039	0.51	0.99		
C	0.012	0.029	0.30	0.74		
c2	0.045	0.065	1.14	1.65		
D	0.330	0.380	8.38	9.65		
D1	0.260		6.60			
Е	0.380	0.420	9.65	10.67		
E1	0.245		6.22			
е	0.100 BSC		2.54	BSC		
Н	0.575	0.625	14.60	15.88		
L	0.070	0.110	1.78	2.79		
L1		0.066		1.68		
L2		0.070		1.78		
L3	0.010 BSC		0.25	BSC		
М	0°	8°	0°	8°		

0.063

0.169

0.100 PITCH DIMENSIONS: INCHES

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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