

FDBL86361-F085

POWERTRENCH[®] MOSFET, N-Channel

80 V, 300 A, 1.4 mΩ



ON Semiconductor[®]

www.onsemi.com

Features

- Typical $R_{DS(on)}$ = 1.1 mΩ at $V_{GS} = 10$ V, $I_D = 80$ A
- Typical $Q_{g(tot)}$ = 172 nC at $V_{GS} = 10$ V, $I_D = 80$ A
- UIS Capability
- AEC-Q101 Qualified and PPAP Capable
- RoHS Compliant

Applications

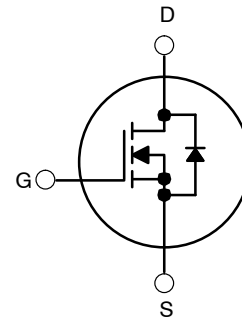
- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12 V Systems

MOSFET MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

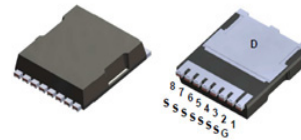
Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	80	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Drain Current – Continuous ($V_{GS} = 10$), $T_C = 25^\circ\text{C}$ (Note 1)	300	A
	Pulsed Drain Current, $T_C = 25^\circ\text{C}$	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	820	mJ
P_D	Power Dissipation	429	W
	Derate Above 25°C	2.86	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to $+175$	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.35	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	43	$^\circ\text{C}/\text{W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by bondwire configuration.
2. Starting $T_J = 25^\circ\text{C}$, $L = 0.4$ mH, $I_{AS} = 64$ A, $V_{DD} = 40$ V during inductor charging and $V_{DD} = 0$ V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

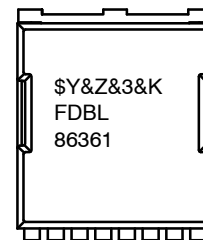


N-Channel



H-PSOF8L
CASE 100CU

MARKING DIAGRAM



- | | |
|-----------|-------------------------|
| \$Y | = ON Semiconductor Logo |
| &Z | = Assembly Plant Code |
| &3 | = Numeric Date Code |
| &K | = Lot Code |
| FDBL86361 | = Specific Device Code |

ORDERING INFORMATION

Device	Top Mark	Package	Shipping [†]
FDBL86361-F085	FDBL86361	H-PSOF8L	2000 Units/ Tape&Reel

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

FDBL86361–F085

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain-to-Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	80	–	–	V	
I _{DSS}	Drain-to-Source Leakage Current	V _{DS} = 80 V, V _{GS} = 0 V	T _J = 25°C	–	–	1	μA
			T _J = 175°C (Note 4)	–	–	1	mA
I _{GSS}	Gate-to-Source Leakage Current	V _{GS} = ±20 V	–	–	±100	μA	

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	2.0	3.0	4.0	V	
R _{DS(on)}	Drain to Source on Resistance	I _D = 80 A, V _{GS} = 10 V	T _J = 25°C	–	1.1	1.4	mΩ
			T _J = 175°C (Note 4)	–	2.4	3.1	mΩ

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz	–	12800	–	pF
C _{oss}	Output Capacitance		–	1925	–	pF
C _{rss}	Reverse Transfer Capacitance		–	139	–	pF
R _g	Gate Resistance	f = 1 MHz	–	2.7	–	Ω
Q _{g(toT)}	Total Gate Charge at 10 V	V _{GS} = 0 to 10 V V _{DD} = 64 V I _D = 80 A	–	172	188	nC
Q _{g(th)}	Threshold Gate Charge		–	23	27	nC
Q _{gs}	Gate-to-Source Gate Charge		–	51	–	nC
Q _{gd}	Gate-to-Drain "Miller" Charge		–	34	–	nC

SWITCHING CHARACTERISTICS

t _{on}	Turn-On Time	V _{DD} = 40 V, I _D = 80 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	–	128	ns
t _{d(on)}	Turn-On Delay		–	42	–	ns
t _r	Rise Time		–	73	–	ns
t _{d(off)}	Turn-Off Delay		–	87	–	ns
t _f	Fall Time		–	48	–	ns
t _{off}	Turn-Off Time		–	–	193	ns

DRAIN-SOURCE DIODE CHARACTERISTIC

V _{SD}	Source-to-Drain Diode Voltage	I _{SD} = 80 A, V _{GS} = 0 V	–	–	1.25	V
		I _{SD} = 40 A, V _{GS} = 0 V	–	–	1.2	V
t _{rr}	Reverse-Recovery Time	I _F = 80 A, dI _{SD} /dt = 100 A/μs, V _{DD} = 64 V	–	117	136	ns
Q _{rr}	Reverse-Recovery Charge		–	205	269	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

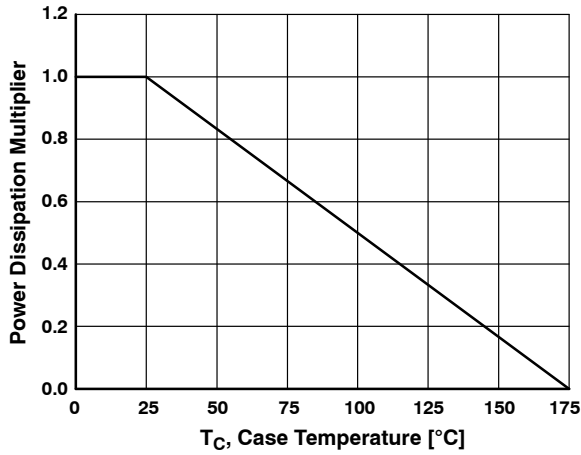


Figure 1. Normalized Power Dissipation vs. Case Temperature

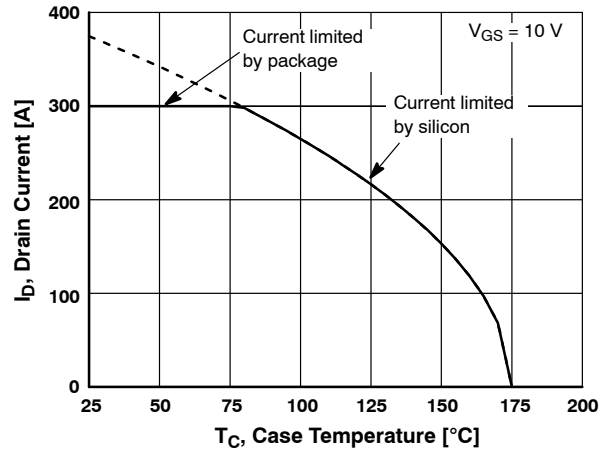


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

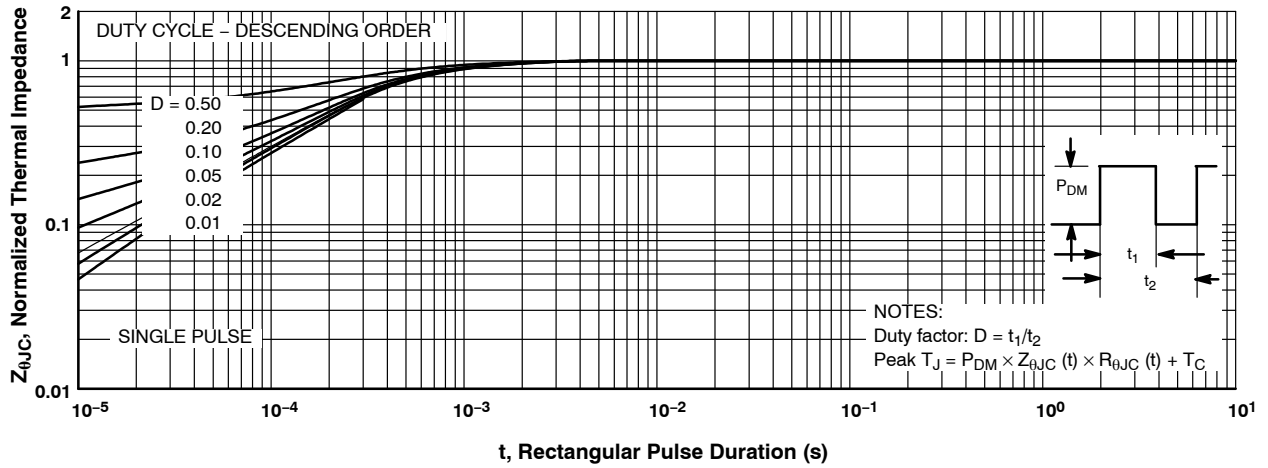


Figure 3. Normalized Maximum Transient Thermal Impedance

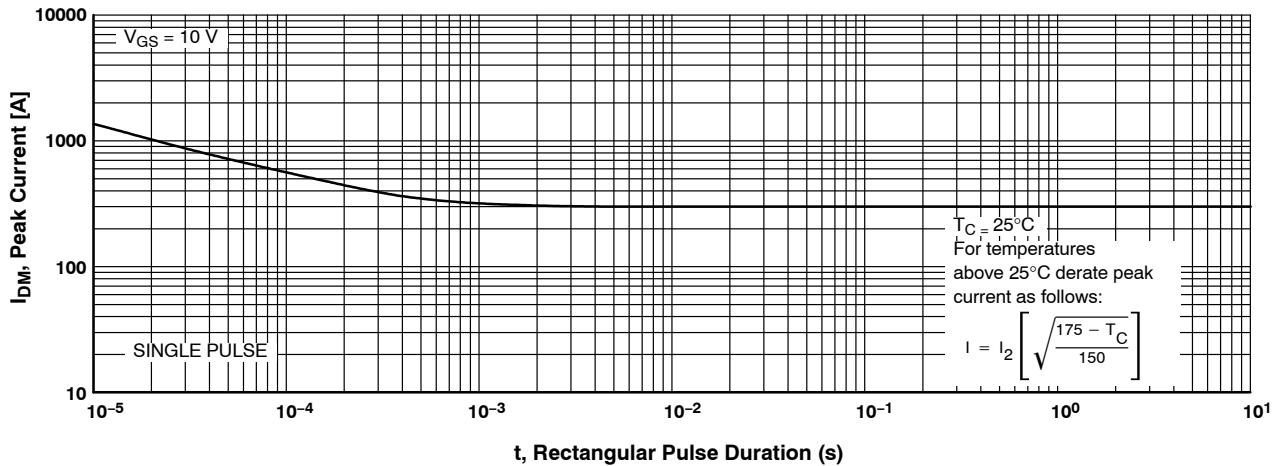


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

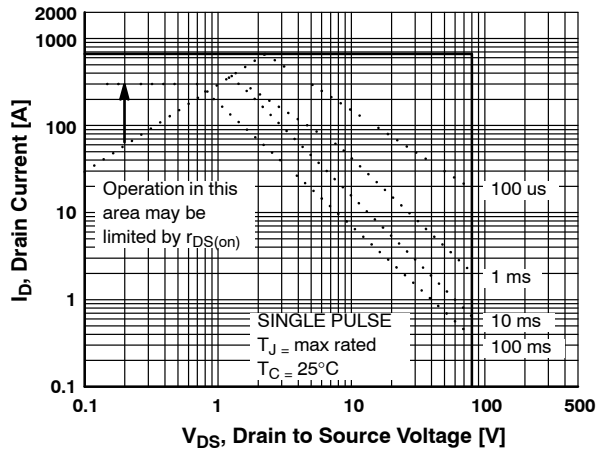
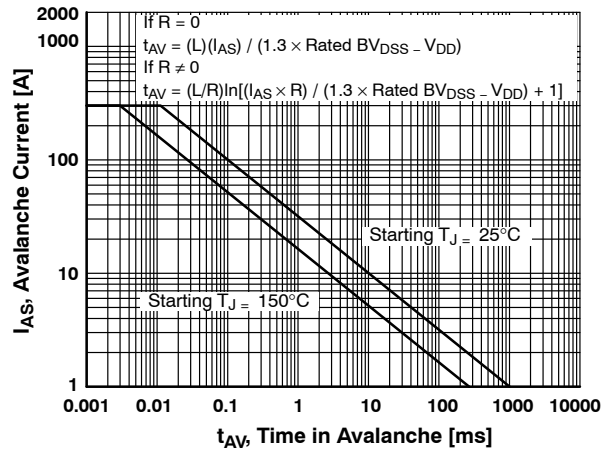


Figure 5. Forward Bias Safe Operating Area



Refer to ON Semiconductor Application Notes AN7514 and AN7515.

Figure 6. Unclamped Inductive Switching Capability

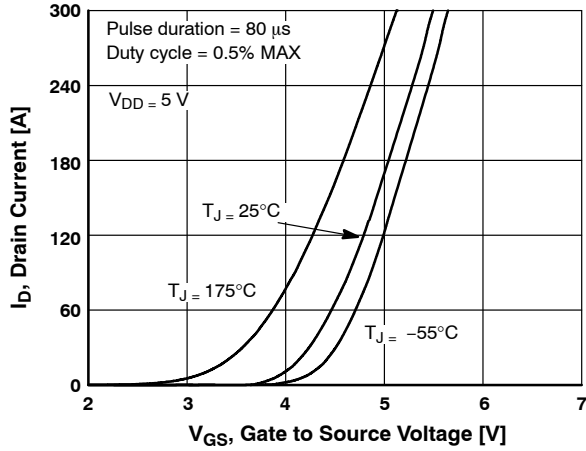


Figure 7. Transfer Characteristics

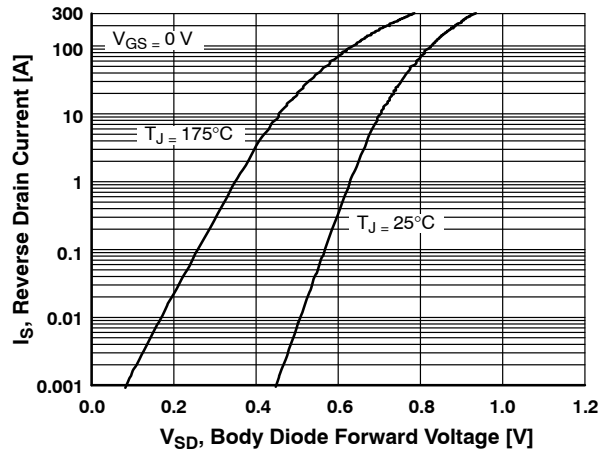


Figure 8. Forward Diode Characteristics

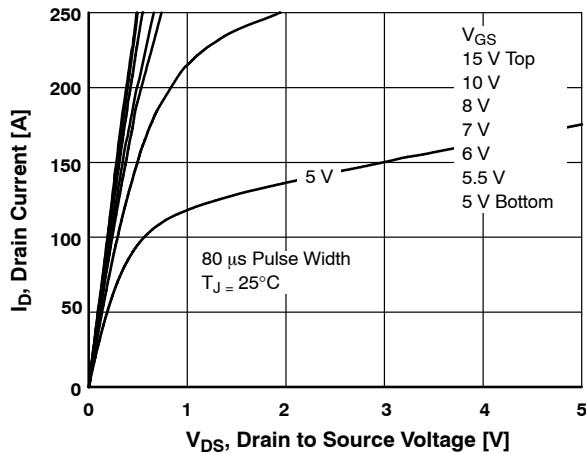


Figure 9. Saturation Characteristics

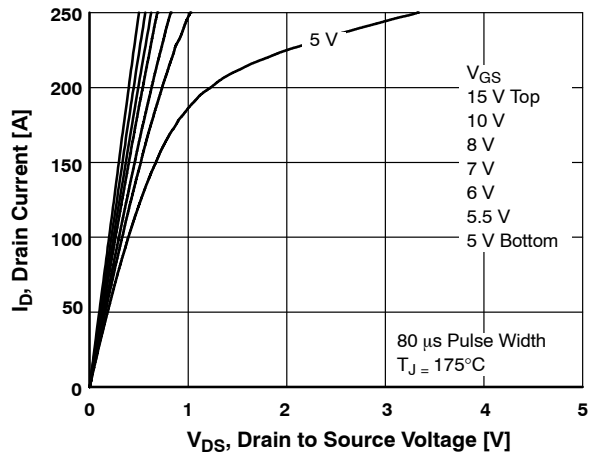


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (continued)

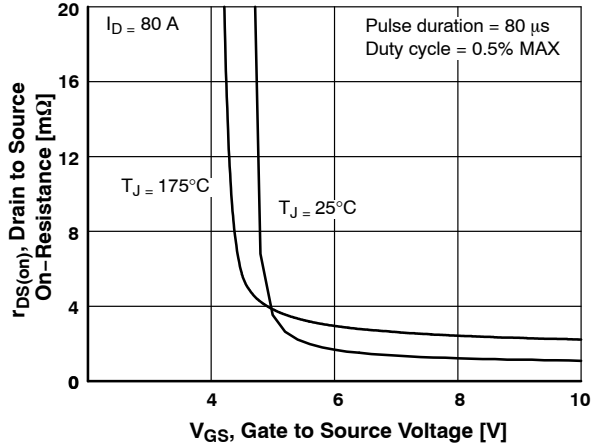


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

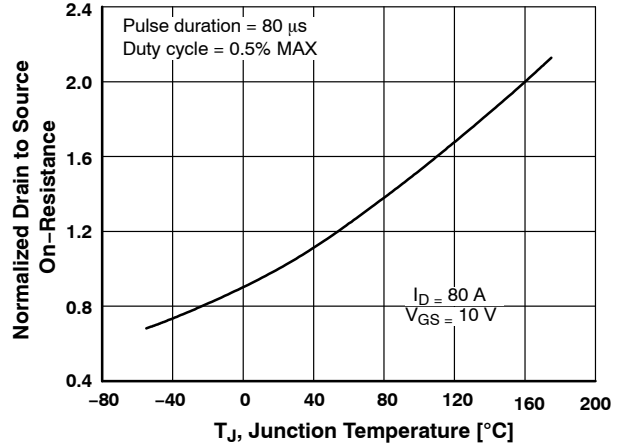


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

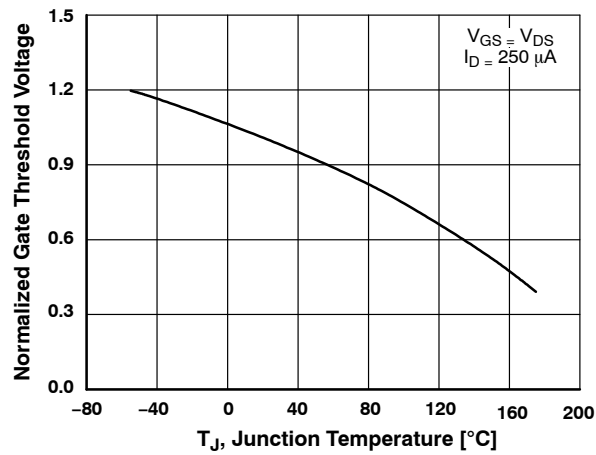


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

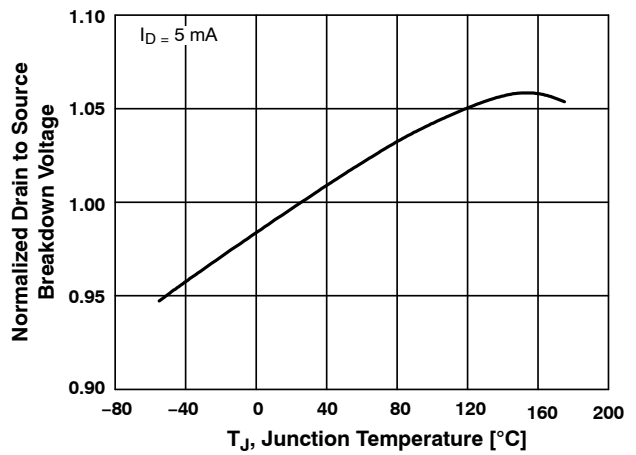


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

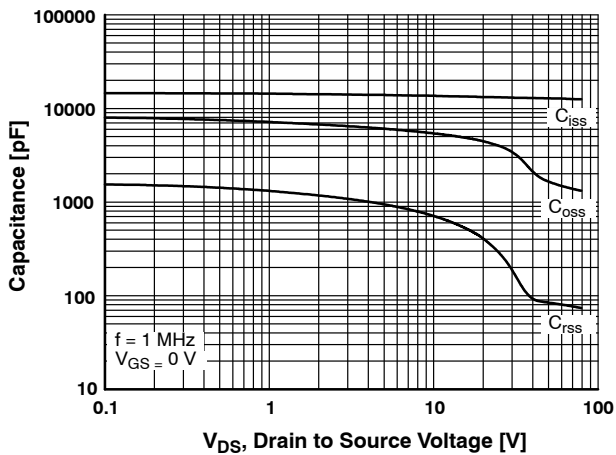


Figure 15. Capacitance vs. Drain to Source Voltage

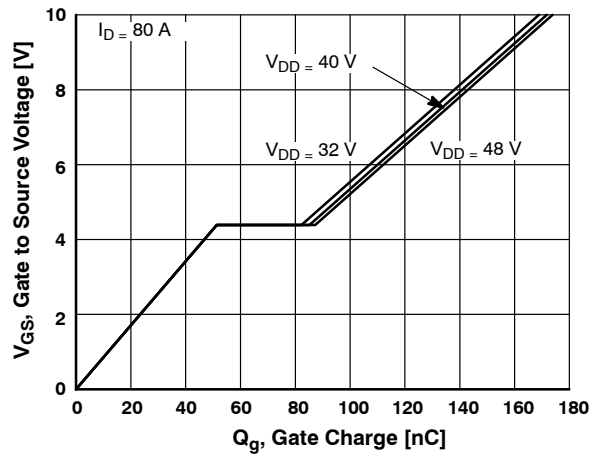


Figure 16. Gate Charge vs. Gate to Source Voltage

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

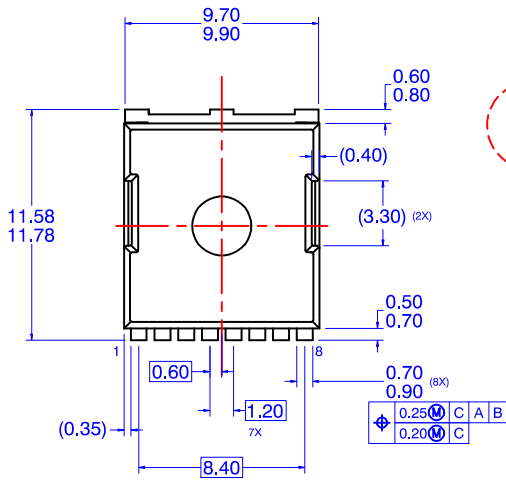
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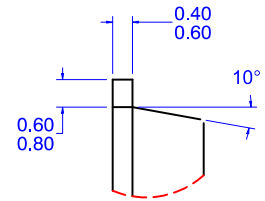
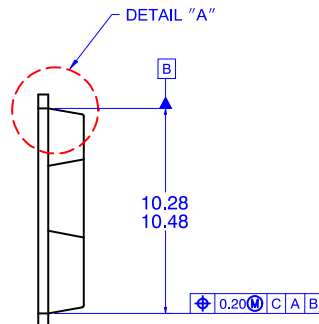
H-PSOF8L 11.68x9.80

CASE 100CU
ISSUE O

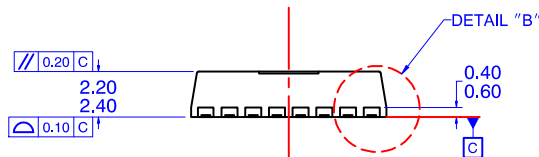
DATE 30 NOV 2016



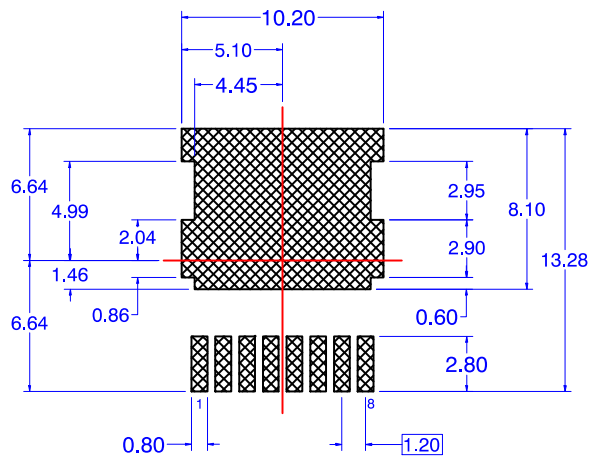
TOP VIEW



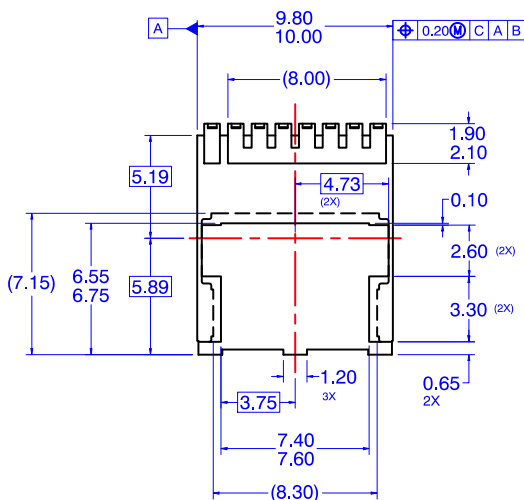
DETAIL "A"



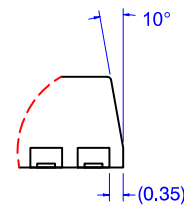
SIDE VIEW



LAND PATTERN RECOMMENDATION



BOTTOM VIEW



DETAIL "B"

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A, DATED NOVEMBER 2009.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
 - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

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