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April 2015

FDBL86366_F085

N-Channel PowerTrench[®] MOSFET 80 V, 220 A, 3.0 m Ω

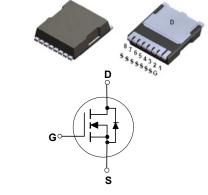
Features

- Typical $R_{DS(on)}$ = 2.4 m Ω at V_{GS} = 10V, I_D = 80 A
- Typical $Q_{q(tot)}$ = 86 nC at V_{GS} = 10V, I_D = 80 A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12V Systems





For current package drawing, please refer to the Fairchild website at http://www.fairchildsemi.com/dwg/PS/PSOF08A.pdf.

MOSFET Maximum Ratings T_J = 25°C unless otherwise noted.

Symbol	Parameter		Ratings	Units
V _{DSS}	Drain-to-Source Voltage		80	V
V _{GS}	Gate-to-Source Voltage		±20	V
	Drain Current - Continuous (V _{GS} =10) (Note 1)	T _C = 25°C	220	
I _D	Pulsed Drain Current	T _C = 25°C	See Figure 4	A
E _{AS}	Single Pulse Avalanche Energy	(Note 2)	205	mJ
D	Power Dissipation		300	W
P_{D}	Derate Above 25°C		2.0	W/°C
T _J , T _{STG}	Operating and Storage Temperature		-55 to + 175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case		0.5	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient	(Note 3)	43	°C/W

Notes

- 1: Current is limited by silicon
- 2: Starting T_J = 25°C, L = 0.1mH, I_{AS} = 64A, V_{DD} = 80V during inductor charging and V_{DD} = 0V during time in avalanche.
- 3: R_{0,JA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{0,JC} is guaranteed by design, while R_{0,JA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDBL86366	FDBL86366_F085	MO-299A	-	-	-

Units

Max.

Electrical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted.

Parameter

Off Characteristics							
B _{VDSS}	Drain-to-Source Breakdown Voltage	$I_D = 250 \mu A$	V _{GS} = 0V	80	-	-	V
I _{DSS}	Drain-to-Source Leakage Current	V _{DS} =80V,	$T_J = 25^{\circ}C$	-	-	1	μΑ
		$V_{GS} = 0V$	$T_J = 175^{\circ}C \text{ (Note 4)}$	-	-	1	mA
loco	Gate-to-Source Leakage Current	V ₀₀ = +20\	/	_	_	+100	nΔ

Test Conditions

Min.

Тур.

On Characteristics

Symbol

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$		2.0	3.0	4.0	٧
D	R _{DS(on)} Drain to Source On Resistance	I _D = 80A,	$T_{\rm J} = 25^{\rm o}{\rm C}$	-	2.4	3.0	mΩ
NDS(on)		V _{GS} = 10V	$T_J = 175^{\circ}C \text{ (Note 4)}$	ı	4.9	6.1	mΩ

Dynamic Characteristics

C _{iss}	Input Capacitance	.,		-	6320	-	pF
C _{oss}	Output Capacitance	→ v _{DS} = 40v, v _{GS} = 1 — f = 1MHz	$V_{DS} = 40V, V_{GS} = 0V,$		1030	-	pF
C _{rss}	Reverse Transfer Capacitance	-1 - 1WITZ		-	32	-	pF
R_g	Gate Resistance	f = 1MHz		-	2.1	-	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10V	$V_{GS} = 0$ to 10V	V _{DD} = 64V	-	86	112	nC
Q _{g(th)}	Threshold Gate Charge	$V_{GS} = 0 \text{ to } 2V$	I _D = 80A	-	12	18	nC
Q_{gs}	Gate-to-Source Gate Charge		_	-	30	-	nC
Q_{gd}	Gate-to-Drain "Miller" Charge			-	18	-	nC

Switching Characteristics

t _{on}	Turn-On Time		-	-	98	ns
t _{d(on)}	Turn-On Delay		-	30	-	ns
t _r	Rise Time	V _{DD} = 40V, I _D = 80A,	-	34	-	ns
t _{d(off)}	Turn-Off Delay	V_{GS} = 10V, R_{GEN} = 6Ω	-	40	-	ns
t _f	Fall Time		-	17	-	ns
t _{off}	Turn-Off Time		-	-	86	ns

Drain-Source Diode Characteristics

V	Source-to-Drain Diode Voltage	I _{SD} =80A, V _{GS} = 0V	-	-	1.25	V
V_{SD}	Source-to-Drain blode voltage	$I_{SD} = 40A, V_{GS} = 0V$	-	-	1.2	V
t _{rr}	Reverse-Recovery Time	$I_F = 80A$, $dI_{SD}/dt = 100A/\mu s$,	-	80	120	ns
Q _{rr}	Reverse-Recovery Charge	V _{DD} =64V	-	95	140	nC

Note:

4: The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

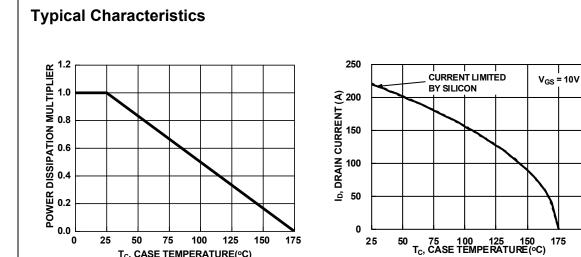


Figure 1. Normalized Power Dissipation vs. Case **Temperature**

T_C, CASE TEMPERATURE(°C)

Figure 2. Maximum Continuous Drain Current vs. **Case Temperature**

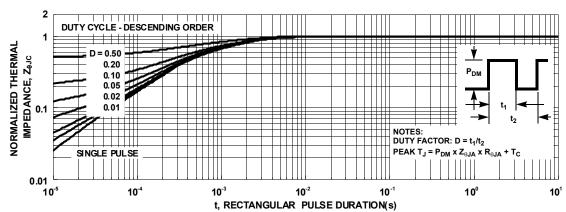


Figure 3. Normalized Maximum Transient Thermal Impedance

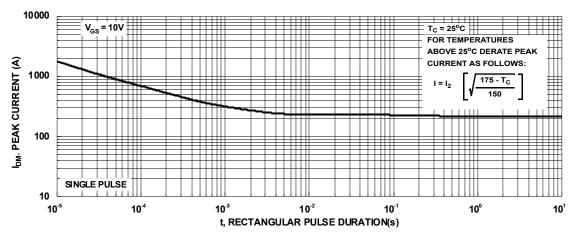


Figure 4. Peak Current Capability

Typical Characteristics

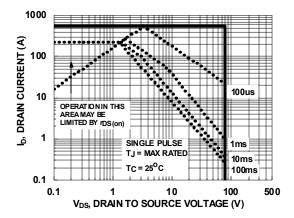
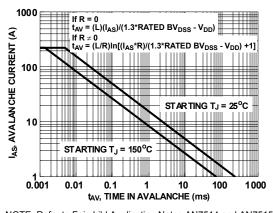


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching

Capability

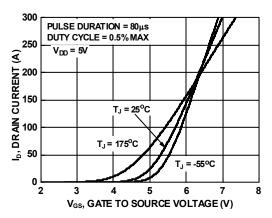


Figure 7. Transfer Characteristics

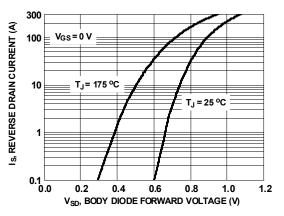


Figure 8. Forward Diode Characteristics

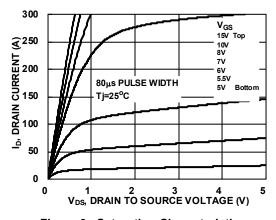


Figure 9. Saturation Characteristics

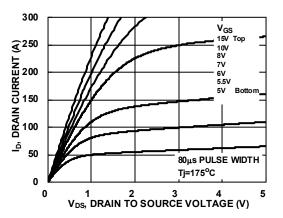


Figure 10. Saturation Characteristics

Typical Characteristics

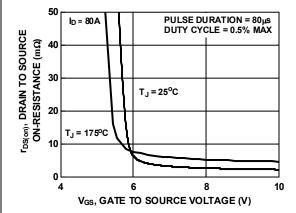


Figure 11. R_{DSON} vs. Gate Voltage

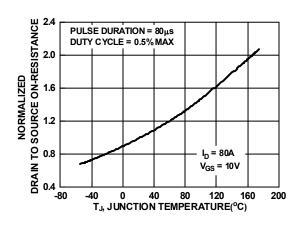


Figure 12. Normalized R_{DSON} vs. Junction Temperature

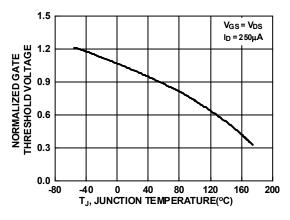


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

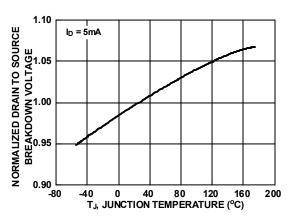


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

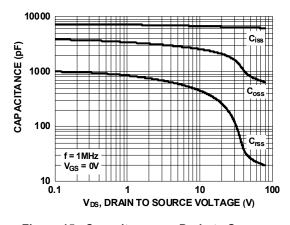


Figure 15. Capacitance vs. Drain to Source Voltage

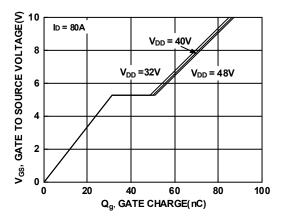


Figure 16. Gate Charge vs. Gate to Source Voltage





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