



ON Semiconductor®

FDC655BN

Single N-Channel, Logic Level, PowerTrench® MOSFET 30 V, 6.3 A, 25 mΩ

Features

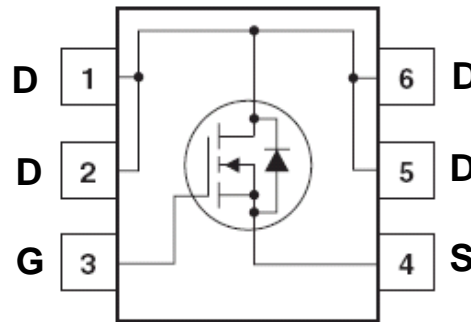
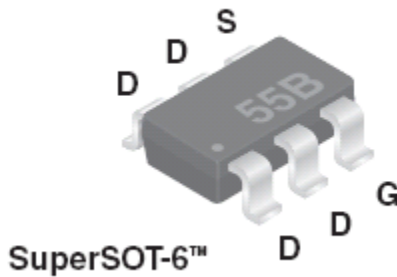
- Max $r_{DS(on)}$ = 25 mΩ at $V_{GS} = 10$ V, $I_D = 6.3$ A
- Max $r_{DS(on)}$ = 33 mΩ at $V_{GS} = 4.5$ V, $I_D = 5.5$ A
- Fast switching
- Low gate charge
- High performance technology for extremely low $r_{DS(on)}$
- Termination is Lead-free and RoHS Compliant



General Description

This N-Channel Logic Level MOSFET is produced using ON Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Ratings | Units |
|----------------|--|--------------|------------------|
| V_{DS} | Drain to Source Voltage | 30 | V |
| V_{GS} | Gate to Source Voltage | ± 20 | V |
| I_D | -Continuous $T_A = 25^\circ\text{C}$ (Note 1a) | 6.3 | A |
| | -Pulsed | 20 | |
| P_D | Power Dissipation (Note 1a) | 1.6 | W |
| | Power Dissipation (Note 1b) | 0.8 | |
| T_J, T_{STG} | Operating and Storage Junction Temperature Range | -55 to + 150 | $^\circ\text{C}$ |

Thermal Characteristics

| | | | | |
|-----------------|---|-----------|----|--------------------|
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | (Note 1a) | 78 | $^\circ\text{C/W}$ |
|-----------------|---|-----------|----|--------------------|

Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|----------------|----------|---------|-----------|------------|------------|
| .55B | FDC655BN | SSOT-6™ | 7" | 8 mm | 3000 units |

FDC655BN Single N-Channel, Logic Level, PowerTrench® MOSFET

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------|-----------|-----------------|-----|-----|-----|-------|
|--------|-----------|-----------------|-----|-----|-----|-------|

Off Characteristics

| | | | | | | |
|--------------------------------------|---|--|----|----|-----------|----------------------|
| BV_{DSS} | Drain to Source Breakdown Voltage | $I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$ | 30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250 \mu\text{A}$, referenced to 25°C | | 25 | | mV/ $^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$ | | | 1 | μA |
| I_{GSS} | Gate to Source Leakage Current | $V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$ | | | ± 100 | nA |

On Characteristics

| | | | | | | |
|--|--|---|---|-----|----|----------------------|
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$ | 1 | 1.9 | 3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D = 250 \mu\text{A}$, referenced to 25°C | | -5 | | mV/ $^\circ\text{C}$ |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS} = 10 \text{ V}, I_D = 6.3 \text{ A}$ | | 21 | 25 | m Ω |
| | | $V_{GS} = 4.5 \text{ V}, I_D = 5.5 \text{ A}$ | | 26 | 33 | |
| | | $V_{GS} = 10 \text{ V}, I_D = 6.3 \text{ A}, T_J = 125^\circ\text{C}$ | | 30 | 36 | |
| g_{FS} | Forward Transconductance | $V_{DS} = 10 \text{ V}, I_D = 6.3 \text{ A}$ | | 35 | | S |

Dynamic Characteristics

| | | | | | | |
|-----------|------------------------------|--|--|-----|-----|----------|
| C_{iss} | Input Capacitance | $V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1\text{MHz}$ | | 470 | 620 | pF |
| C_{oss} | Output Capacitance | | | 100 | 130 | pF |
| C_{rss} | Reverse Transfer Capacitance | | | 60 | 90 | pF |
| R_g | Gate Resistance | | | 3.0 | | Ω |

Switching Characteristics

| | | | | | | | |
|--------------|-------------------------------|---|---|--|----|----|----|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD} = 15 \text{ V}, I_D = 1 \text{ A}, V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$ | | 6 | 11 | ns | |
| t_r | Rise Time | | | 2 | 10 | ns | |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 15 | 26 | ns | |
| t_f | Fall Time | | | 2 | 10 | ns | |
| Q_g | Total Gate Charge | | $V_{GS} = 0 \text{ V to } 10 \text{ V}$ | $V_{DD} = 15 \text{ V}, I_D = 6.3 \text{ A}$ | 9 | 13 | nC |
| Q_g | Total Gate Charge | | $V_{GS} = 0 \text{ V to } 5 \text{ V}$ | | 5 | 7 | nC |
| Q_{gs} | Gate to Source Charge | | 1.4 | | | nC | |
| Q_{gd} | Gate to Drain "Miller" Charge | | 1.6 | | | nC | |

Drain-Source Diode Characteristics

| | | | | | | |
|----------|---|--|--|-----|-----|----|
| I_S | Maximum Continuous Drain-Source Diode Forward Current | | | 1.3 | A | |
| V_{SD} | Source-Drain Diode Forward Voltage | $V_{GS} = 0 \text{ V}, I_S = 1.3 \text{ A}$ (Note 2) | | 0.8 | 1.2 | V |
| t_{rr} | Reverse Recovery Time | $I_F = 6.3 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ | | 15 | 26 | ns |
| Q_{rr} | Reverse Recovery Charge | | | 4 | 10 | nC |

Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

- a. $78 \text{ }^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2 oz copper on FR-4 board.
- b. $156 \text{ }^\circ\text{C/W}$ when mounted on a minimum pad.

2: Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

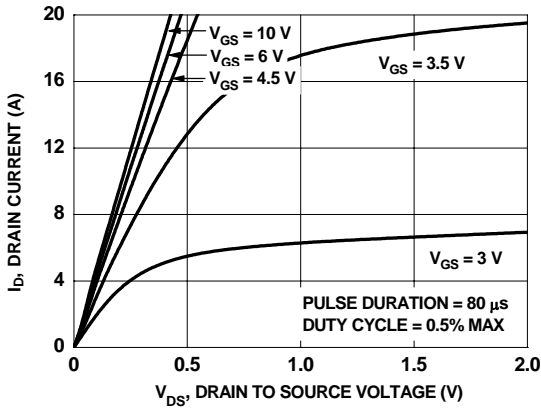


Figure 1. On Region Characteristics

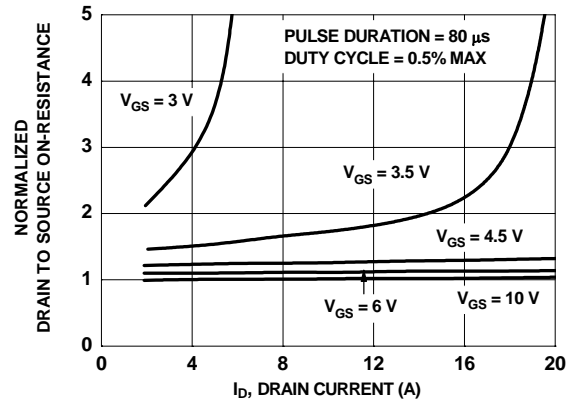


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

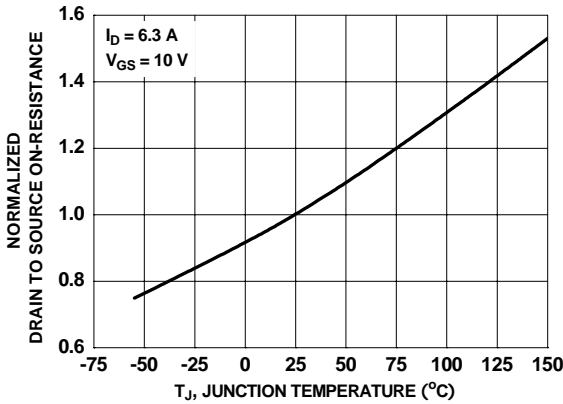


Figure 3. Normalized On Resistance vs Junction Temperature

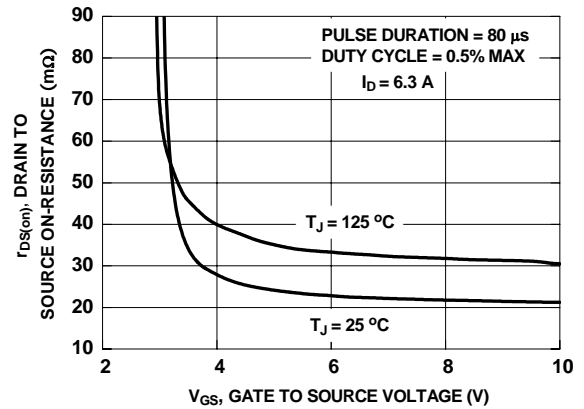


Figure 4. On-Resistance vs Gate to Source Voltage

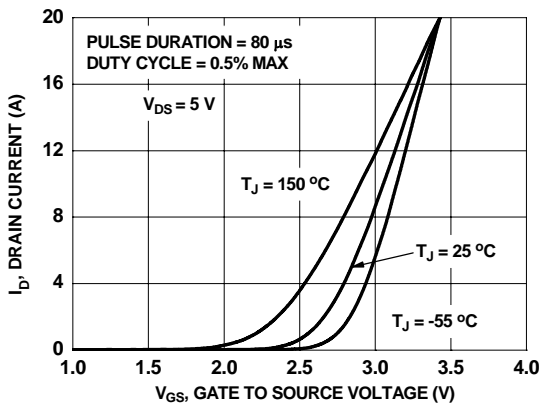


Figure 5. Transfer Characteristics

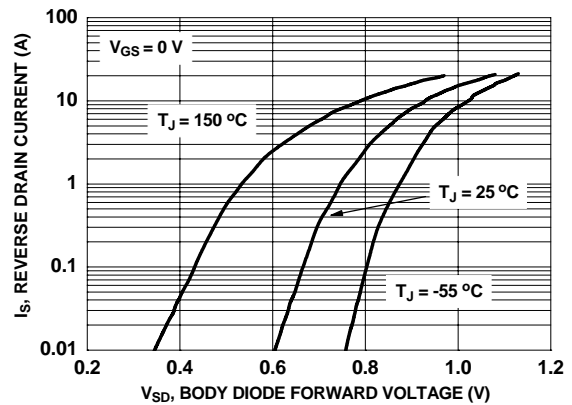


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

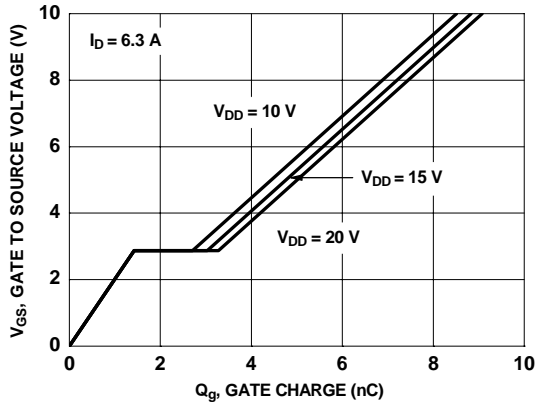


Figure 7. Gate Charge Characteristics

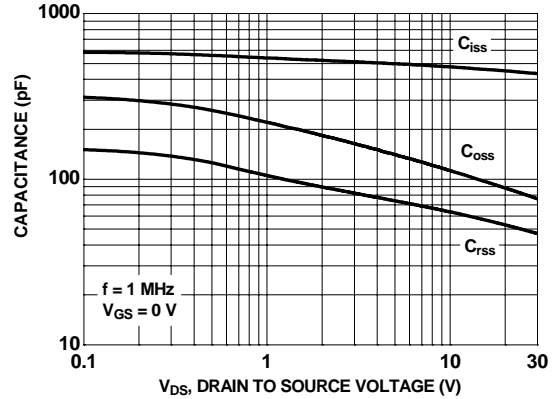


Figure 8. Capacitance vs Drain to Source Voltage

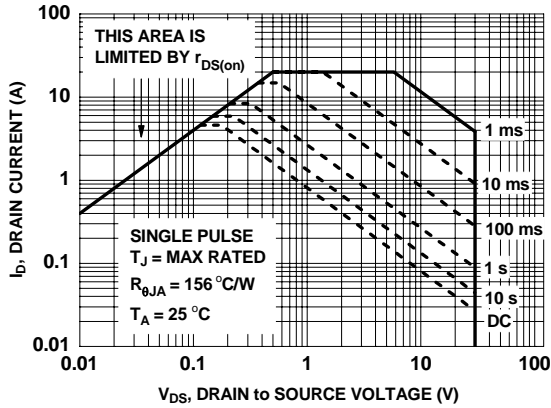


Figure 9. Forward Bias Safe Operating Area

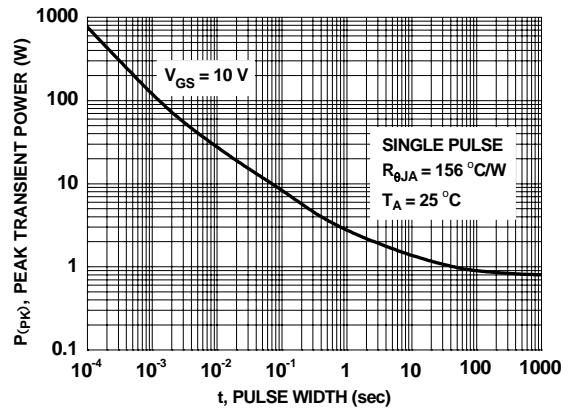


Figure 10. Single Pulse Maximum Power Dissipation

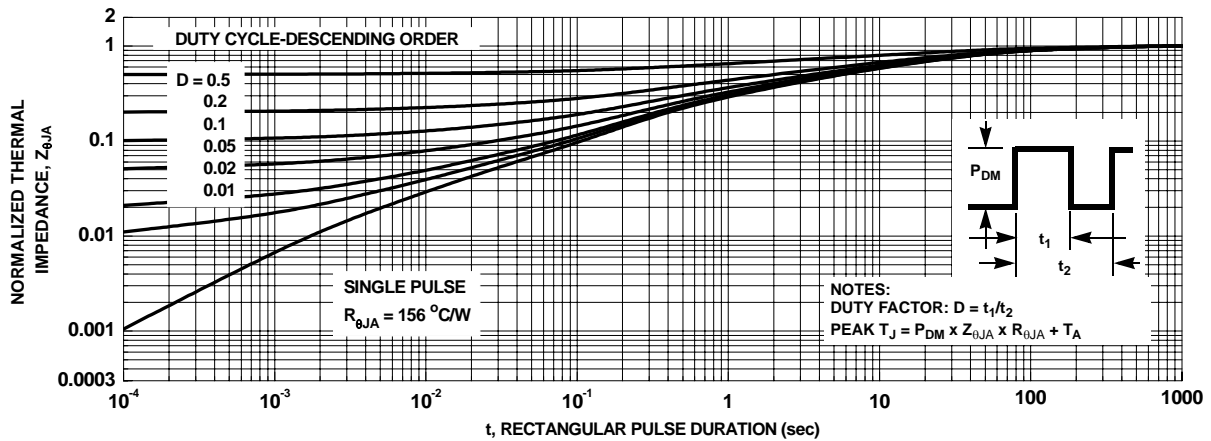



Figure 11. Junction-to-Ambient Transient Thermal Response Curve

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative