ON Semiconductor®

FDD24AN06LA0-F085

## N-Channel Logic Level PowerTrench® MOSFET

60V, 36A, 24mΩ

Features

- $r_{DS(ON)}$ = 20mΩ (Typ.), V_{GS} = 5V, I_D = 36A
- Q_g(tot) = 16nC (Typ.), V_{GS} = 5V
- Low Miller Charge
- Low Q_{RR} Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- Qualified to AEC Q101
- RoHS Compliant

Formerly developmental type 83547

Applications

- Motor / Body Load Control
- ABS Systems
- Powertrain Management
- Injection Systems
- DC-DC converters and Off-line UPS
- Distributed Power Architectures and VRMs
- Primary Switch for 12V and 24V systems

100% RoHS COMPLIANT

DRAIN (FLANGE)

GATE

SOURCE

TO-252AA

FDD SERIES

D

G

S
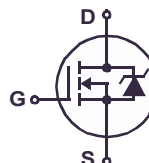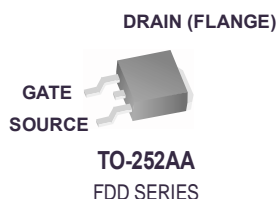
MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current		
	Continuous (T_C = 25°C, V_{GS} = 10V)	40	A
	Continuous (T_C = 25°C, V_{GS} = 5V)	36	A
	Continuous (T_C = 100°C, V_{GS} = 5V)	25	A
	Continuous (T_A = 25°C, V_{GS} = 5V, $R_{\theta JA}$ = 52°C/W)	7.1	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	32	mJ
P_D	Power dissipation	75	W
	Derate above 25°C	0.5	W/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-252	2.0	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252	100	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, 1in² copper pad area	52	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD24AN06LA0	FDD24AN06LA0	TO-252AA	330mm	16mm	2500 units

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
Off Characteristics							
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250µA, V_{GS} = 0V		60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 50V		-	-	1	µA
		V_{GS} = 0V	T_C = 150°C	-	-	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V		-	-	±100	nA
On Characteristics							
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250µA		1	-	2	V
$r_{DS(ON)}$	Drain to Source On Resistance	I_D = 40A, V_{GS} = 10V		-	0.016	0.019	Ω
		I_D = 36A, V_{GS} = 5V		-	0.020	0.024	
		I_D = 36A, V_{GS} = 5V, T_J = 175°C		-	0.047	0.056	
Dynamic Characteristics							
C_{ISS}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	1850	-	pF
C_{OSS}	Output Capacitance			-	180	-	pF
C_{RSS}	Reverse Transfer Capacitance			-	75	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 5V	V_{GS} = 0V to 5V			16	21	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0V to 1V	V_{DD} = 30V	-	1.8	2.4	nC
Q_{gs}	Gate to Source Gate Charge		I_D = 36A	-	6.3	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		I_g = 1.0mA	-	4.5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			-	5.0	-	nC
Switching Characteristics (V_{GS} = 5V)							
t_{ON}	Turn-On Time	V_{DD} = 30V, I_D = 36A, V_{GS} = 5V, R_{GS} = 9.1Ω		-	-	195	ns
$t_{d(ON)}$	Turn-On Delay Time			-	12	-	ns
t_r	Rise Time			-	118	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time			-	26	-	ns
t_f	Fall Time			-	41	-	ns
t_{OFF}	Turn-Off Time			-	-	101	ns
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 36A		-	-	1.25	V
		I_{SD} = 18A		-	-	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 36A, dI_{SD}/dt = 100A/µs		-	-	34	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 36A, dI_{SD}/dt = 100A/µs		-	-	30	nC

Notes:
1: Starting T_J = 25°C, L = 80µH, I_{AS} = 28A.

Typical Characteristics T_C = 25°C unless otherwise noted

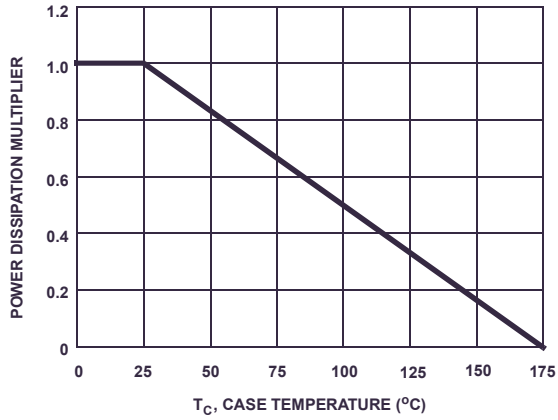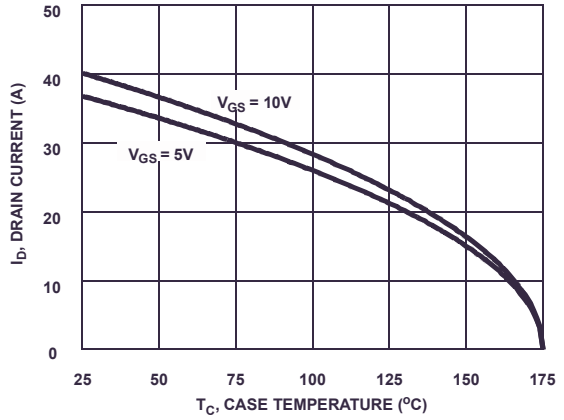**Figure 1. Normalized Power Dissipation vs Ambient Temperature**

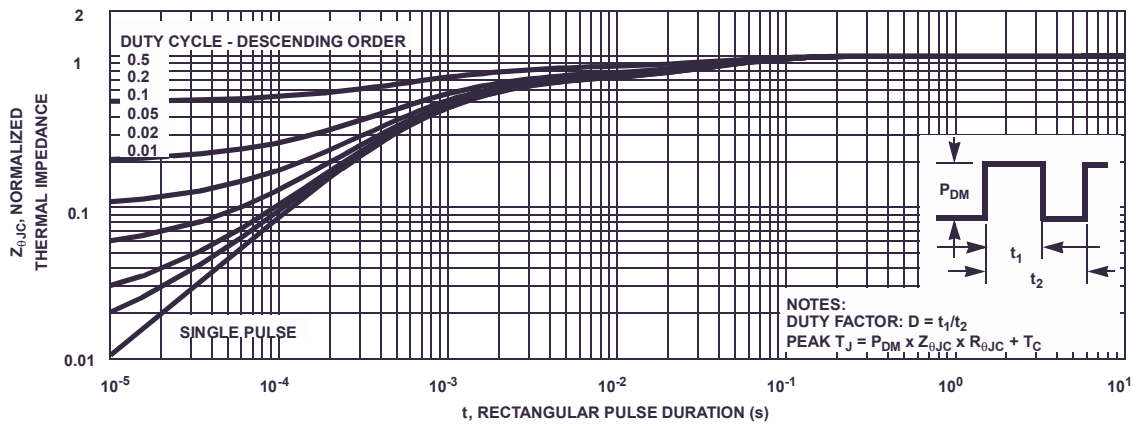**Figure 2. Maximum Continuous Drain Current vs Case Temperature**

NOTES:
DUTY FACTOR: D = t_1/t_2
PEAK T_J = P_{DM} x $Z_{\theta JC}$ x $R_{\theta JC}$ + T_C

Figure 3. Normalized Maximum Transient Thermal Impedance

T_C = 25°C
FOR TEMPERATURES
ABOVE 25°C DERATE PEAK
CURRENT AS FOLLOWS:

$$I = I_{25} \sqrt{\frac{175 - T_C}{150}}$$
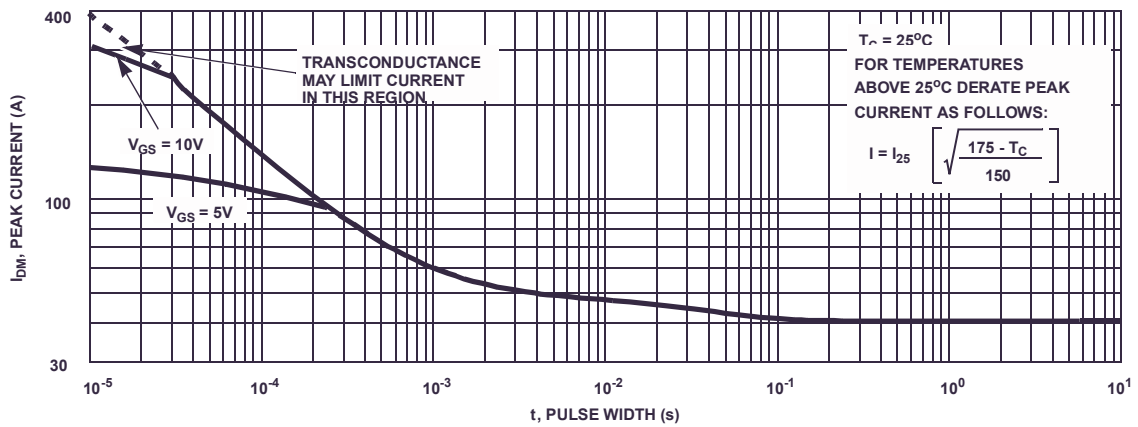
Figure 4. Peak Current Capability

Typical Characteristics T_C = 25°C unless otherwise noted
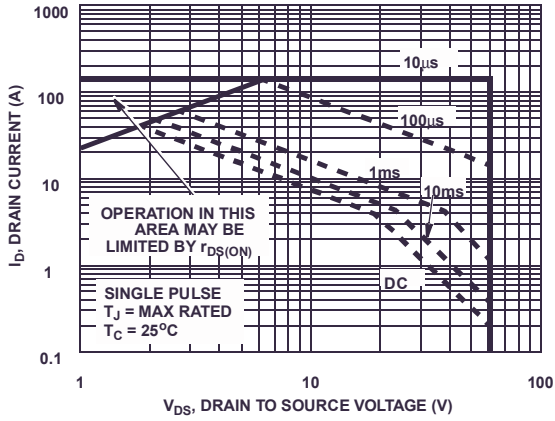
Figure 5. Forward Bias Safe Operating Area
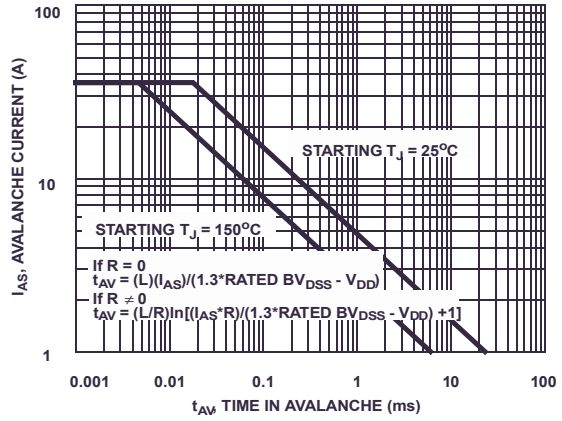
Figure 6. Unclamped Inductive Switching Capability
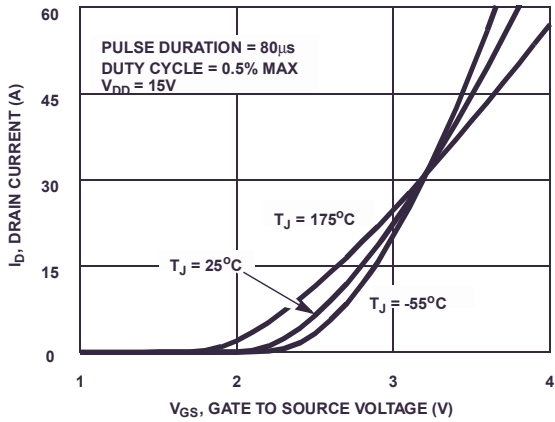
Figure 7. Transfer Characteristics
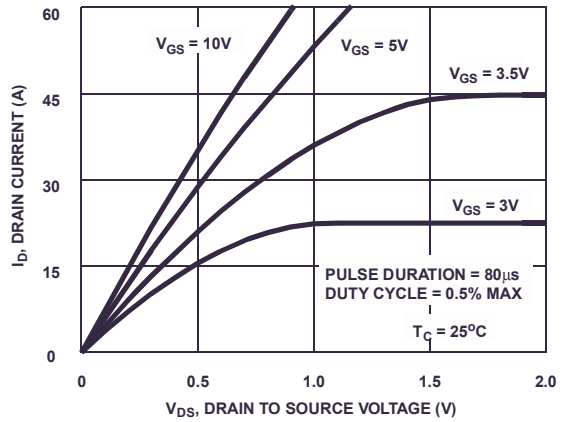
Figure 8. Saturation Characteristics
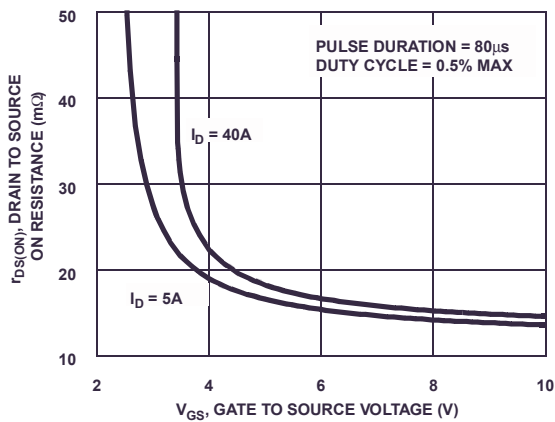
Figure 9. Drain to Source On Resistance vs Gate Voltage and Drain Current
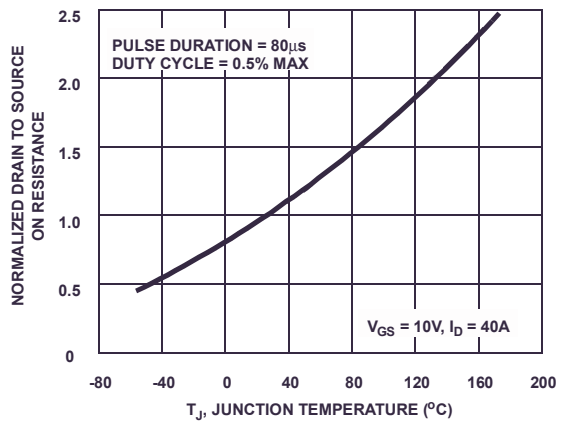
Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics T_C = 25°C unless otherwise noted
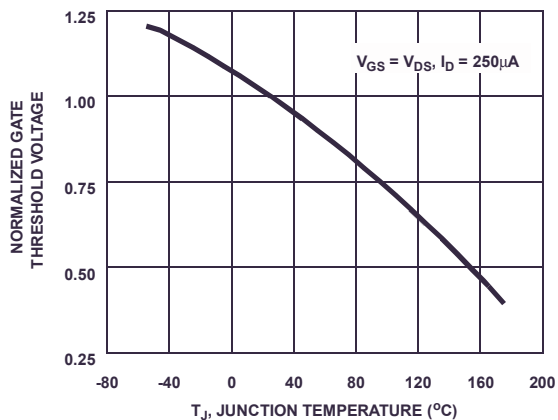
Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

$V_{GS} = V_{DS}$, $I_D = 250\mu A$
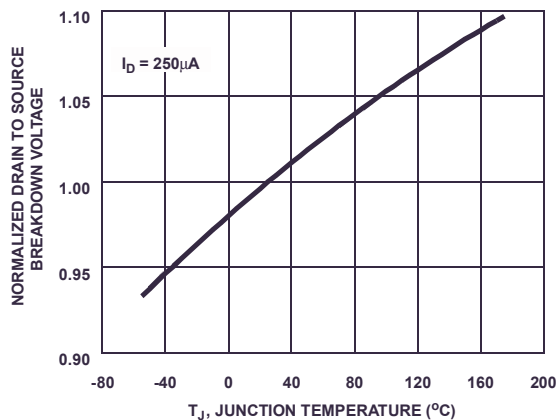
Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

$I_D = 250\mu A$

$C_{ISS} = C_{GS} + C_{GD}$

$C_{OSS} \cong C_{DS} + C_{GD}$

$C_{RSS} = C_{GD}$

$V_{GS} = 0V$, $f = 1MHz$
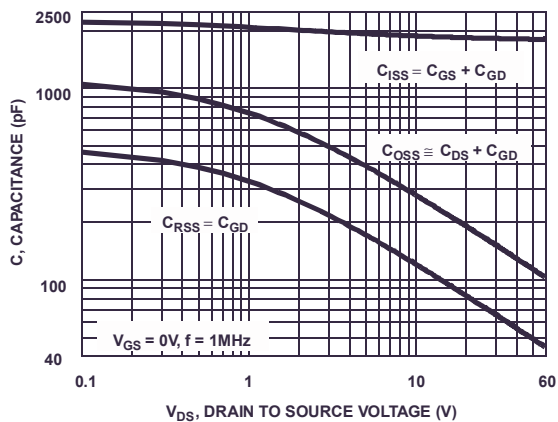
Figure 13. Capacitance vs Drain to Source Voltage

$V_{DD} = 30V$

WAVEFORMS IN DESCENDING ORDER:
$I_D = 36A$
$I_D = 5A$
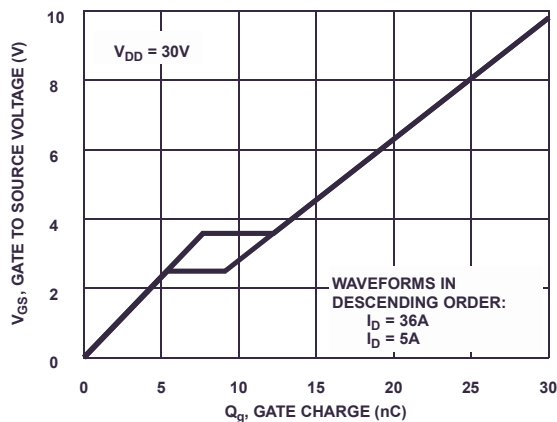
Figure 14. Gate Charge Waveforms for Constant Gate Current

Test Circuits and Waveforms
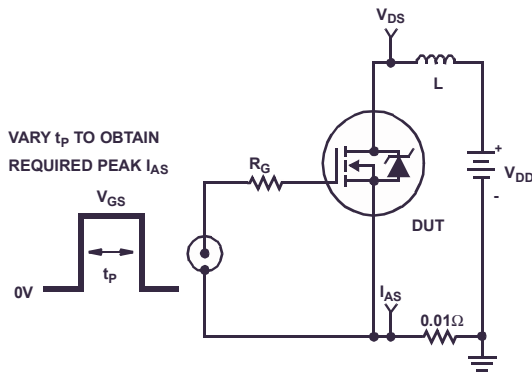
Figure 15. Unclamped Energy Test Circuit
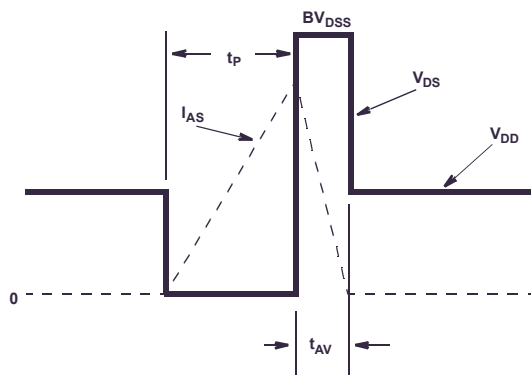
Figure 16. Unclamped Energy Waveforms
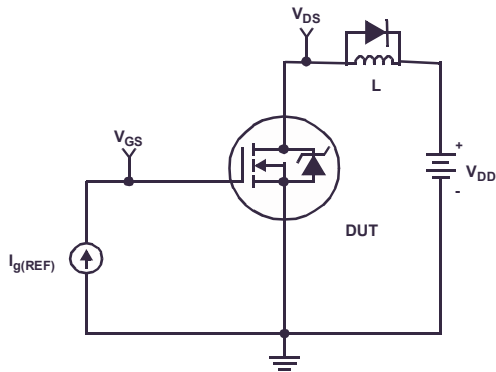
Figure 17. Gate Charge Test Circuit
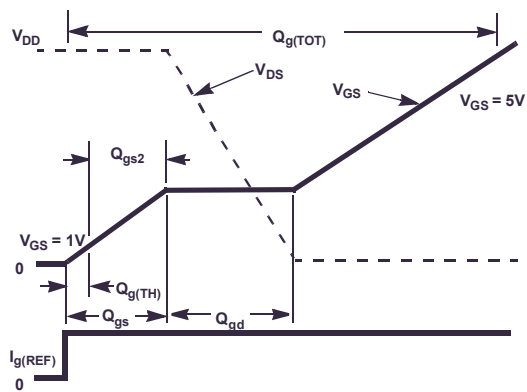
Figure 18. Gate Charge Waveforms
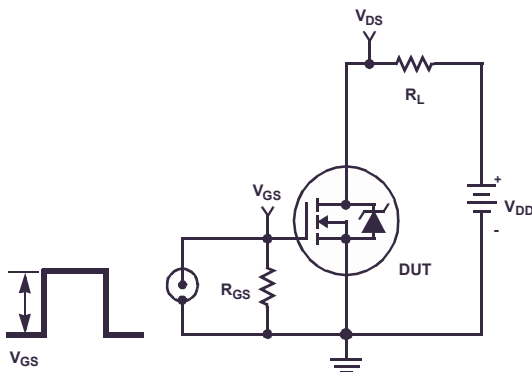
Figure 19. Switching Time Test Circuit
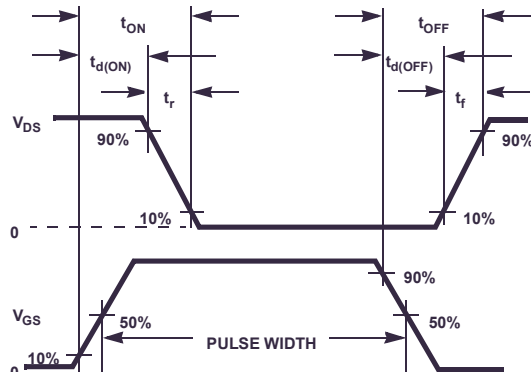
Figure 20. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A (^oC), and thermal resistance $R_{\theta JA}$ ($^oC/W$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \qquad \text{(EQ. 1)}$$

In using surface mount devices such as the TO-252 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.

2. The number of copper layers and the thickness of the board.

3. The use of external heat sinks.

4. The use of thermal vias.

5. Air flow and board orientation.

6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

ON Semiconductor provides thermal information to assist the designer's preliminary application evaluation. Figure 21
defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the ON Semiconductor device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 33.32 + \frac{23.84}{(0.268 + Area)} \qquad \text{(EQ. 2)}$$

Area in Inches Squared

$$R_{\theta JA} = 33.32 + \frac{154}{(1.73 + Area)} \qquad \text{(EQ. 3)}$$
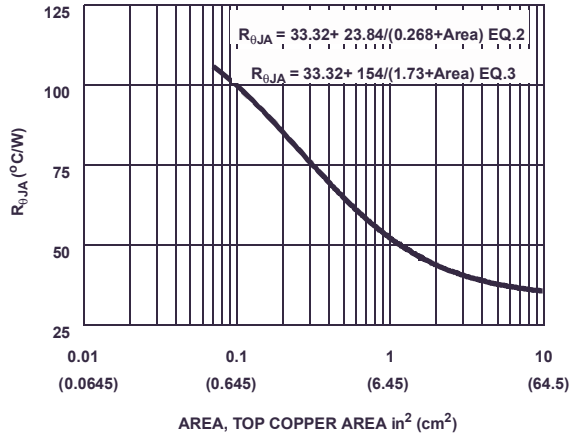
Area in Centimeters Squared

Figure 21. Thermal Resistance vs Mounting Pad Area

PUBLICATION ORDERING INFORMATION