

FDD86569

MOSFET – N-Channel, POWERTRENCH®

60 V, 90 A, 5.7 mΩ

Features

- Typical $R_{DS(on)} = 4.2\text{ m}\Omega$ at $V_{GS} = 10\text{ V}$, $I_D = 80\text{ A}$
- Typical $Q_{g(tot)} = 35\text{ nC}$ at $V_{GS} = 10\text{ V}$, $I_D = 80\text{ A}$
- UIS Capability
- This Device is Pb-Free and is RoHS Compliant

Applications

- Primary Switch for 12 V Systems

MOSFET MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

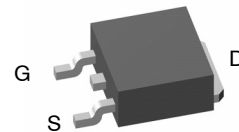
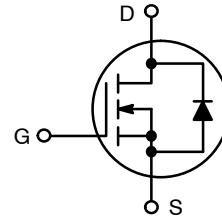
Symbol	Parameter	Ratings	Units
V_{DS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Drain Current - Continuous ($V_{GS} = 10$) (Note 1) $T_C = 25^\circ\text{C}$	90	A
	Pulsed Drain Current $T_C = 25^\circ\text{C}$	See Figure 4	
EAS	Single Pulse Avalanche Energy (Note 2)	41	mJ
P_D	Power Dissipation	150	W
	Derate Above 25°C	1.0	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to $+175$	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.0	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	52	$^\circ\text{C}/\text{W}$

1. Current is limited by bondwire configuration.
2. Starting $T_J = 25^\circ\text{C}$, $L = 15\text{ }\mu\text{H}$, $I_{AS} = 74\text{ A}$, $V_{DD} = 60\text{ V}$ during inductor charging and $V_{DD} = 0\text{ V}$ during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2oz copper.



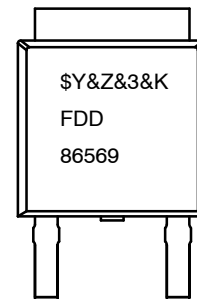
ON Semiconductor®

www.onsemi.com



**DPAK3
CASE 369AS**

MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDD86569	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDD86569

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD86569	FDD86569	D-PAK(TO-252)	13"	16mm	2500 Units

ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ Unless Otherwise Noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

OFF CHARACTERISTICS

B_{VDSS}	Drain-to-Source Breakdown Voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0 \text{ V}$	60	-	-	V	
I_{DSS}	Drain-to-Source Leakage Current	$V_{DS} = 60 \text{ V}$, $V_{GS} = 0 \text{ V}$	$T_J = 25^\circ\text{C}$	-	-	1	μA
			$T_J = 175^\circ\text{C}$ (Note 4)	-	-	1	mA
I_{GSS}	Gate-to-Source Leakage Current	$V_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA	

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250 \mu\text{A}$	2	2.8	4	V	
$R_{DS(on)}$	Drain to Source On Resistance	$I_D = 80 \text{ A}$, $V_{GS} = 10 \text{ V}$	$T_J = 25^\circ\text{C}$	-	4.2	5.7	$\text{m}\Omega$
			$T_J = 175^\circ\text{C}$ (Note 4)	-	8.3	11.3	$\text{m}\Omega$

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	-	2520	-	pF
C_{oss}	Output Capacitance		-	690	-	pF
C_{rss}	Reverse Transfer Capacitance		-	47	-	pF
R_g	Gate Resistance	$V_{GS} = 0.5 \text{ V}$, $f = 1 \text{ MHz}$	-	2.0	-	Ω
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0$ to 10 V	-	35	52	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0$ to 2 V				
Q_{gs}	Gate-to-Source Gate Charge		-	14	-	nC
Q_{gd}	Gate-to-Drain "Miller" Charge		-	7.4	-	nC

SWITCHING CHARACTERISTICS

t_{on}	Turn-On Time	$V_{DD} = 30 \text{ V}$, $I_D = 80 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_{GEN} = 6 \Omega$	-	-	53	ns
$t_{d(on)}$	Turn-On Delay		-	15	-	ns
t_r	Rise Time		-	20	-	ns
$t_{d(off)}$	Turn-Off Delay		-	22	-	ns
t_f	Fall Time		-	8	-	ns
t_{off}	Turn-Off Time		-	-	45	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source-to-Drain Diode Voltage	$I_{SD} = 80 \text{ A}$, $V_{GS} = 0 \text{ V}$	-	-	1.25	V
		$I_{SD} = 40 \text{ A}$, $V_{GS} = 0 \text{ V}$	-	-	1.2	V
t_{rr}	Reverse-Recovery Time	$V_{DD} = 48 \text{ V}$, $I_F = 80 \text{ A}$, $di_{SD}/dt = 100 \text{ A}/\mu\text{s}$	-	52	68	ns
Q_{rr}	Reverse-Recovery Charge		-	43	65	nC

4. The maximum value is specified by design at $T_J = 175^\circ\text{C}$. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

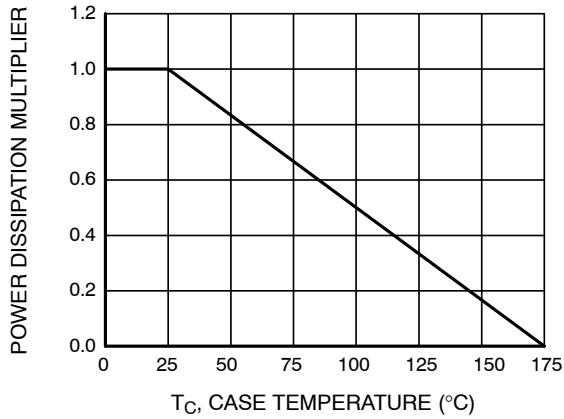


Figure 1. Normalized Power Dissipation vs. Case Temperature

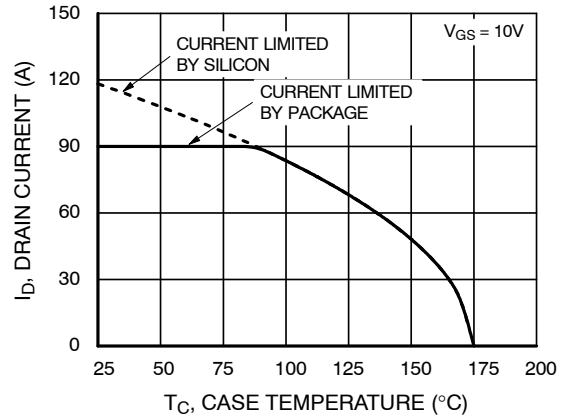


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

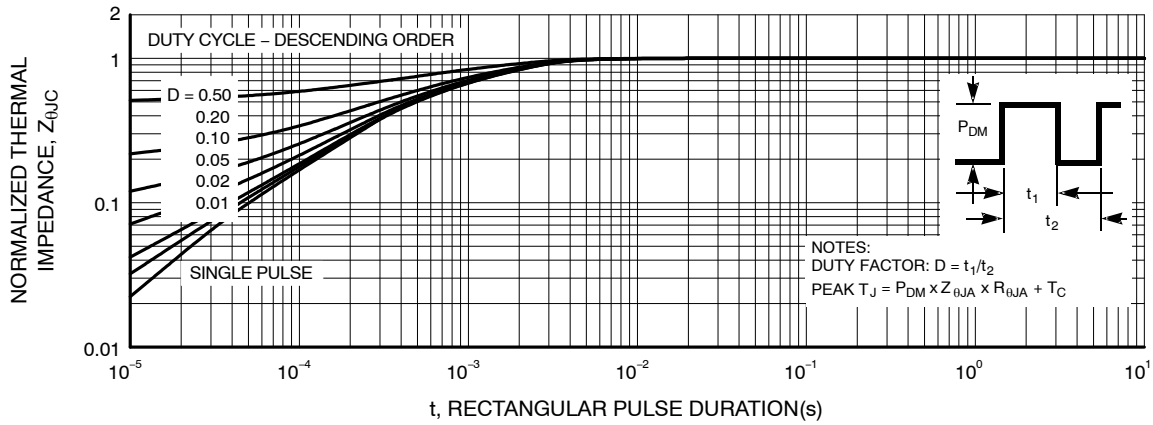


Figure 3. Normalized Maximum Transient Thermal Impedance

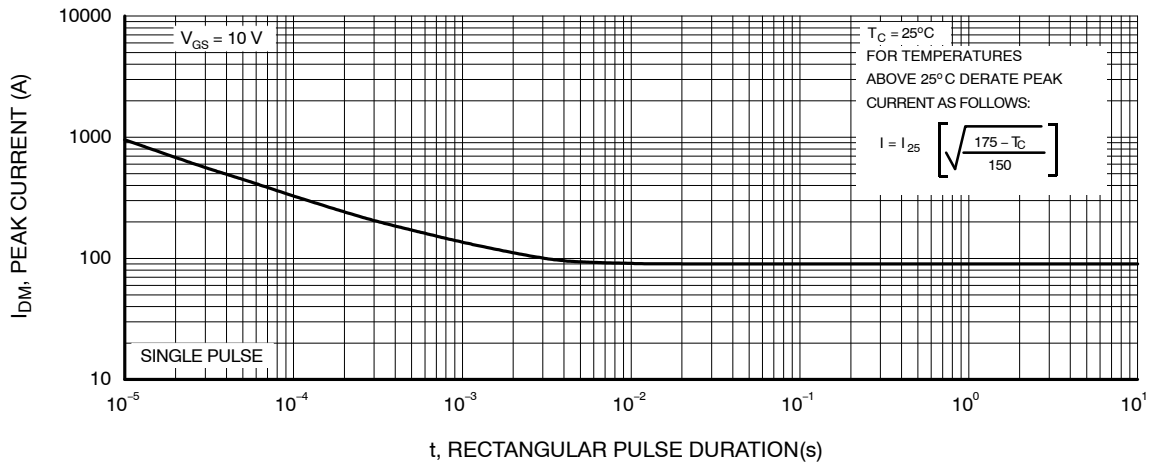


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

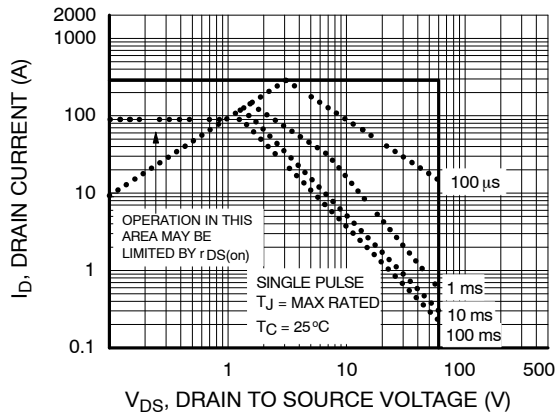
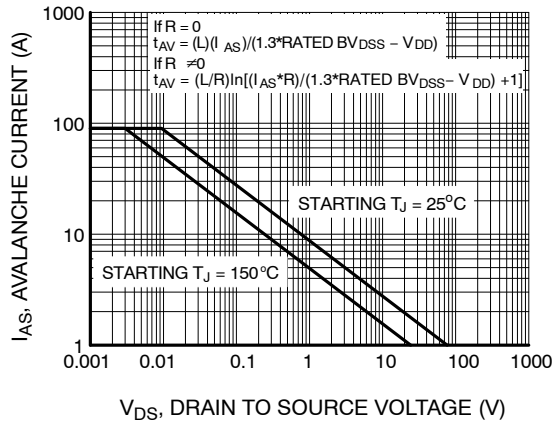


Figure 5. Forward Bias Safe Operating Area



NOTE:
Refer to ON Semiconductor Application Notes AN7514 and AN7515.

Figure 6. Unclamped Inductive Switching Capability

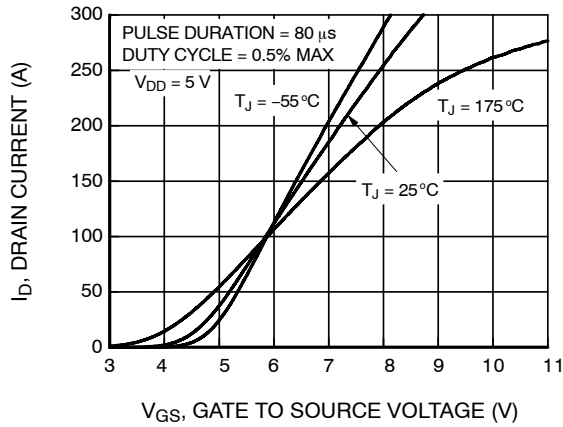


Figure 7. Transfer Characteristics

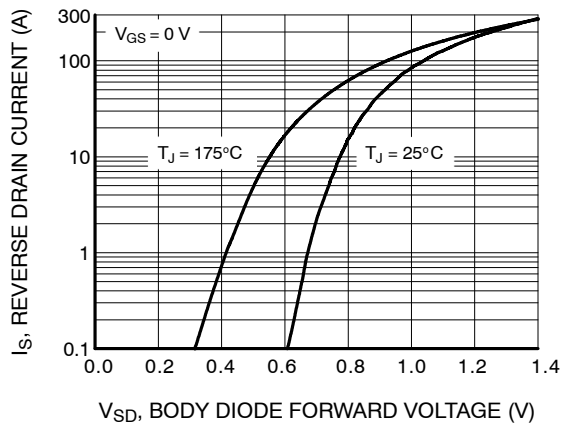


Figure 8. Forward Diode Characteristics

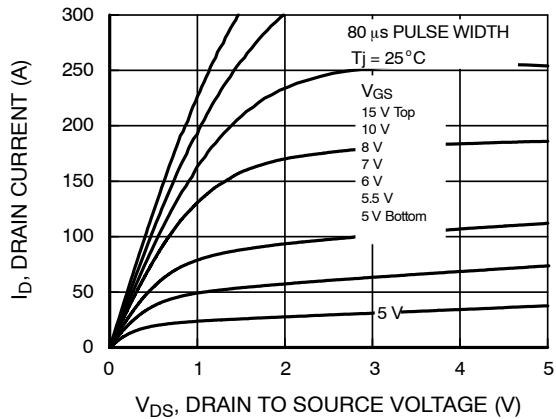


Figure 9. Saturation Characteristics

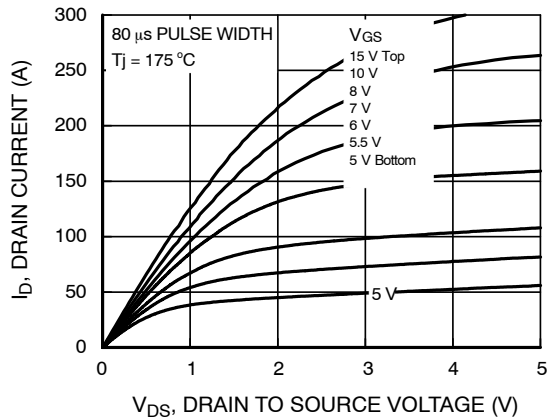


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (continued)

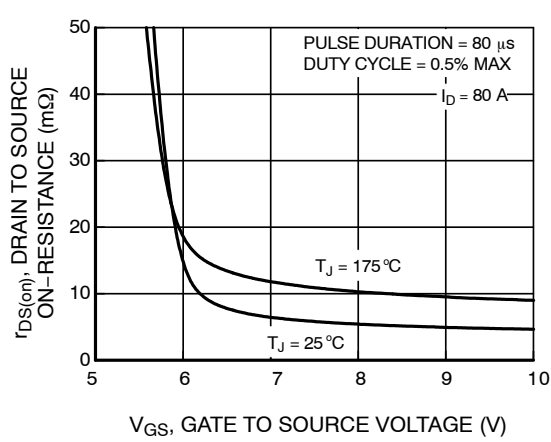


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

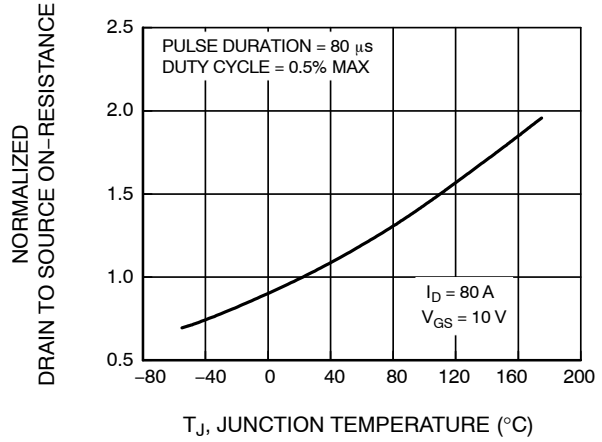


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

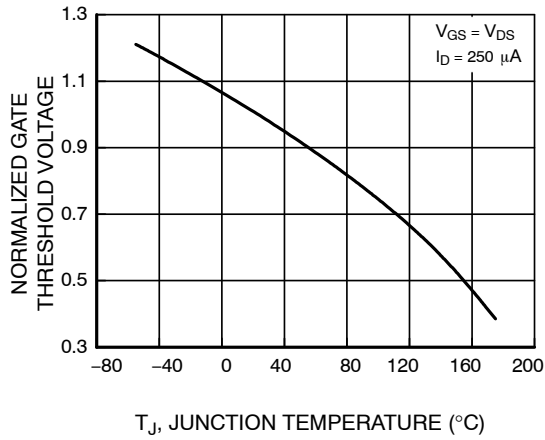


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

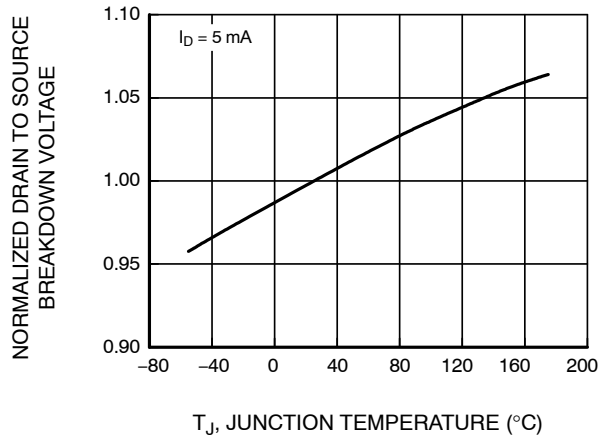


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

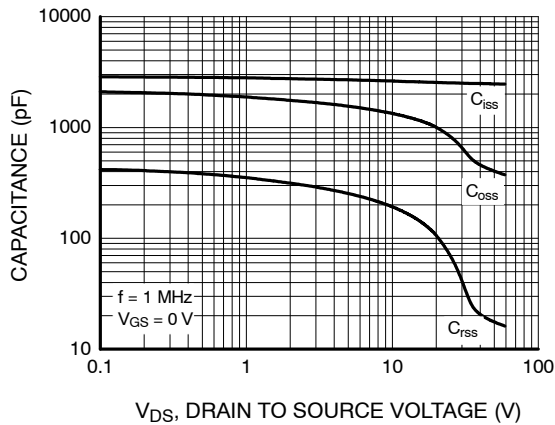


Figure 15. Capacitance vs. Drain to Source Voltage

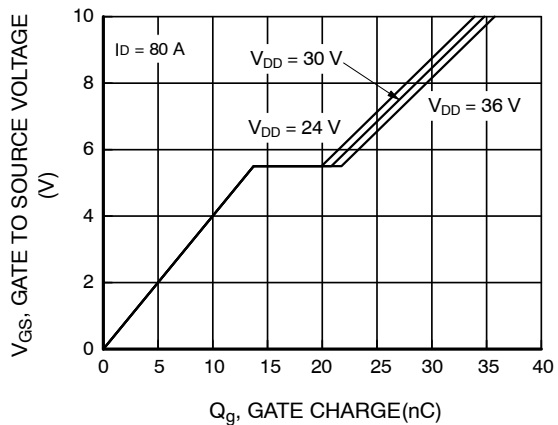
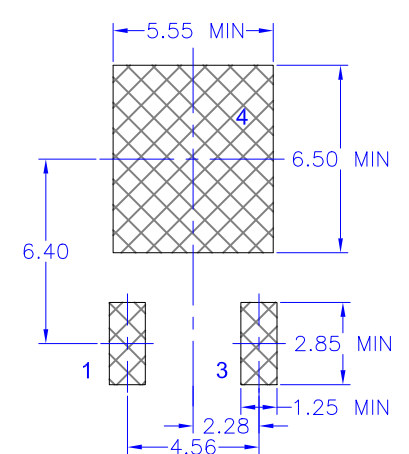
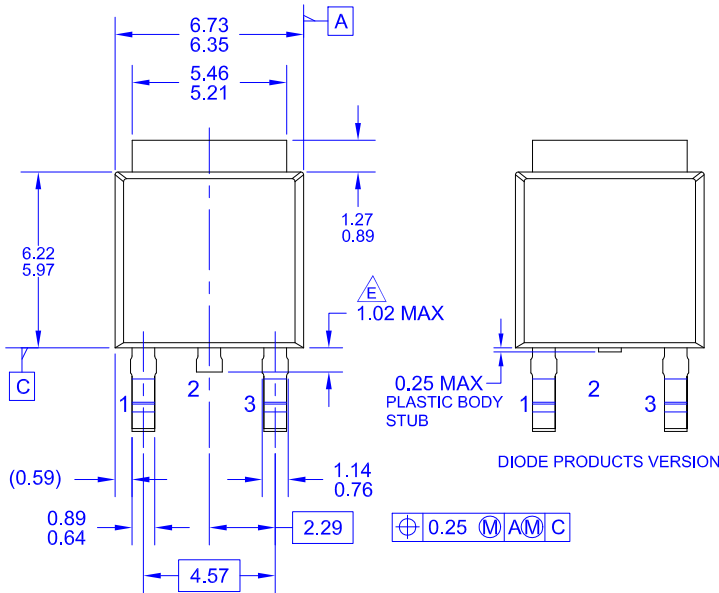


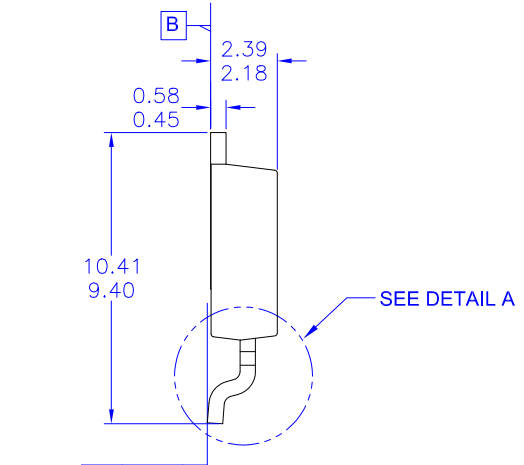
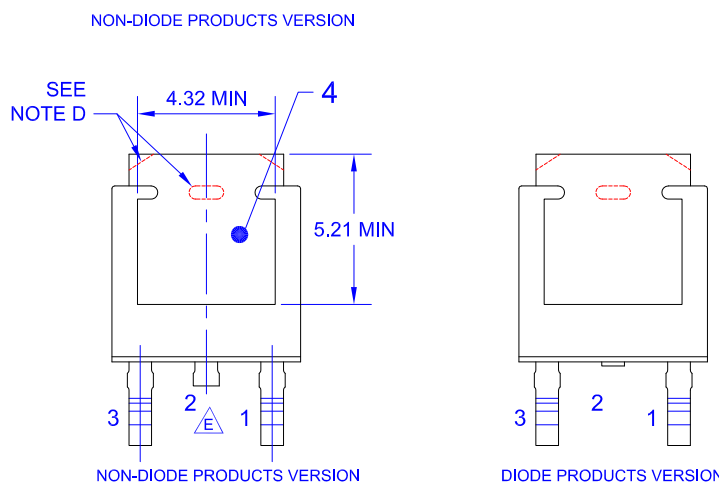
Figure 16. Gate Charge vs. Gate to Source Voltage

PACKAGE DIMENSIONS

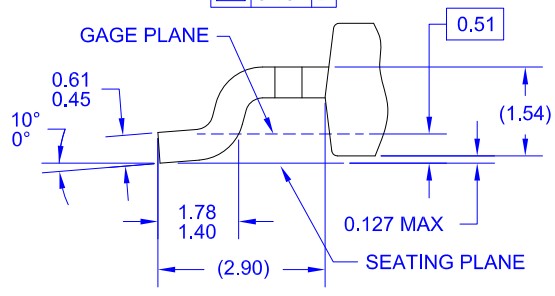
DPAK3 (TO-252 3 LD)
CASE 369AS
ISSUE O



LAND PATTERN RECOMMENDATION




- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
 - D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
 - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



DETAIL A
(ROTATED -90°)
SCALE: 12X

POWERTRENCH is registered trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative