FDG6317NZ

MOSFET – Dual, N-Channel, POWERTRENCH®

20 V, 2.1 A, 550 mΩ

ON Semiconductor®

www.onsemi.com

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
20 V	550 mΩ	2.1 A

General Description

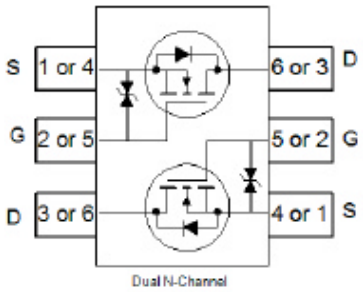
This dual N−Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized use in small switching regulators, providing an extremely low $R_{DS(ON)}$ and gate charge (QG) in a small package.

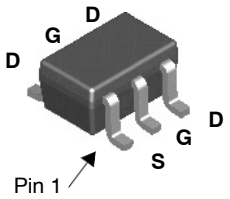
Features

- 0.7 A, 20 V
  - $R_{DS(ON)}$ = 400 mΩ @ V_{GS} = 4.5 V
  - $R_{DS(ON)}$ = 550 mΩ @ V_{GS} = 2.5 V
- Gate−Source Zener for ESD ruggedness
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- Compact Industry Standard SC70−6 Surface Mount Package
- These Devices are Pb−Free and are RoHS Compliant

Applications

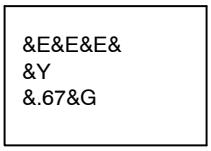
- DC/DC Converter
- Power Management
- Load Switch





SC70−6
CASE 419B

MARKING DIAGRAM



&Y = Data Code
&.67&G = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain−Source Voltage	20	V
V_{GSS}	Gate−Source Voltage	±12	V
I_D	Drain Current: Continuous (Note1) Pulsed	 0.7 2.1	A
P_D	Power Dissipation for Single Operation	0.3	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	FDG6317NZ	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, (Note 1)	415	°C/W

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. $R_{\theta JA}$ = 415°C/W when mounted on a minimum pad.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Reel Size	Tape Width	Quantity
.67	FDG6317NZ	7”	8 mm	3000 units

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	20	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	13	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate−Body Leakage	V_{GS} = ±12 V, V_{DS} = 0 V	–	–	±10	μA
I_{GSS}	Gate−Body Leakage	V_{GS} = ±4.5 V, V_{DS} = 0 V			±1	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	0.6	1.2	1.5	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temperature Coefficient	I_D = −250 μA, Referenced to 25°C	–	−2		mV/°C
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 4.5 V, I_D = 0.7 A V_{GS} = 2.5 V, I_D = 0.6 A V_{GS} = 4.5 V, I_D = 0.7 A, T_J = 125°C		300 450 390	400 550 560	mΩ
$I_{D(on)}$	On−State Drain Current	V_{GS} = 10 V, V_{DS} = 0 V	1			A
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 5 A	–	1.8	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	–	66.5	–	pF
C_{oss}	Output Capacitance		–	19	–	pF
$C_{rss(eff.)}$	Reverse Transfer Capacitance		–	10	–	pF
R_G	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz	–	5.8	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω	–	5.5	11	ns
t_r	Turn-On Rise Time		–	7	15	ns
$t_{d(off)}$	Turn-Off Delay Time		–	7.5	15	ns
t_f	Turn-Off Fall Time		–	2.5	5	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 0.7 A, V_{GS} = 4.5 V,		0.76	1.1	nC
Q_{gs}	Gate−Source Charge			0.18		nC
Q_{gd}	Gate−Drain Charge			0.20		nC
DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Source to Drain Diode Forward Current		–	–	0.25	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.25 A (Note 2)	–	0.8	1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = 0.7 A, dI_F/dt = 100 A/μs	–	8.3	–	nS
Q_{rr}	Diode Reverse Recovery Charge		–	1.2	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

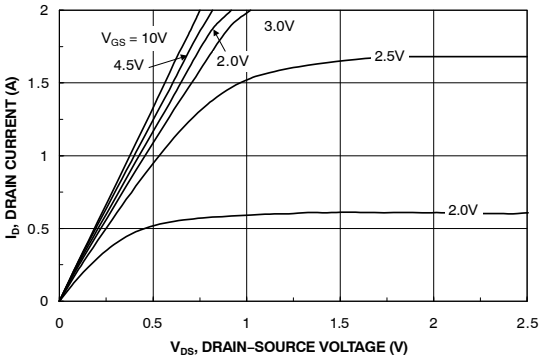


Figure 1. On−Region Characteristics

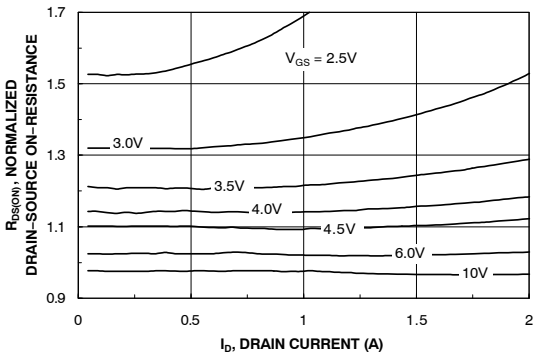


Figure 2. On−Resistance Variation with Drain Current and Gate Voltage

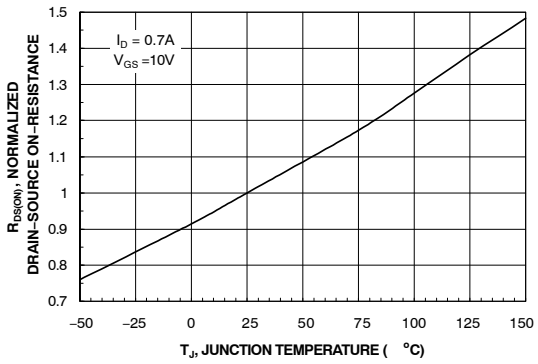


Figure 3. On−Resistance Variation with Temperature

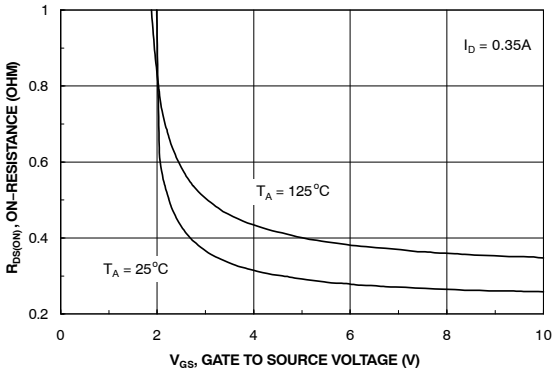


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

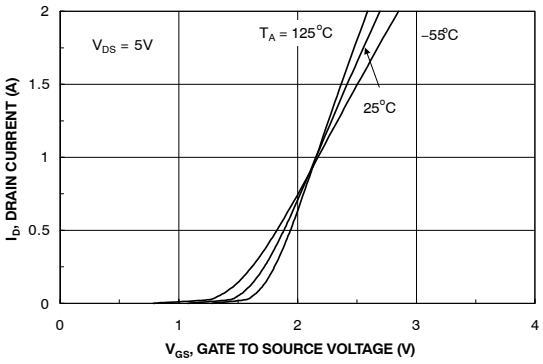


Figure 5. Transfer Characteristics

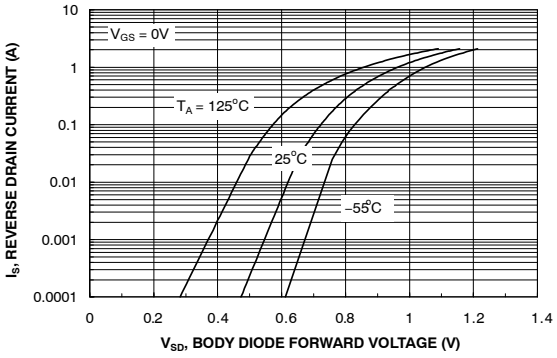


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

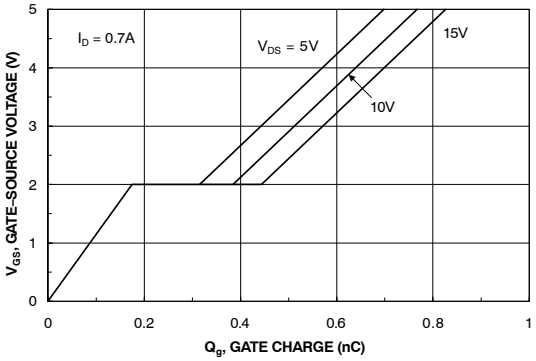


Figure 7. Gate Charge Characteristics

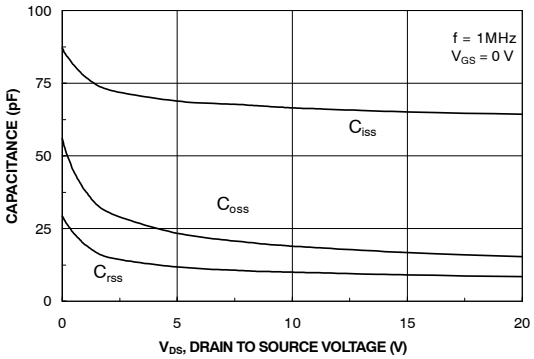


Figure 8. Capacitance Characteristics

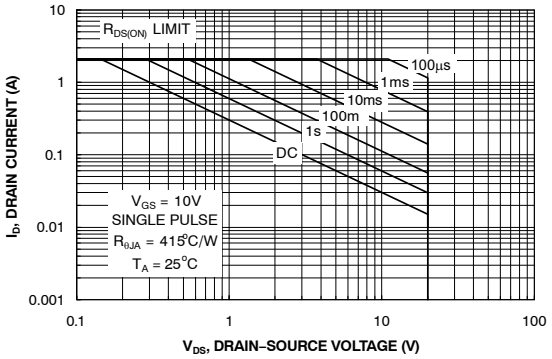


Figure 9. Maximum Safe Operating Area

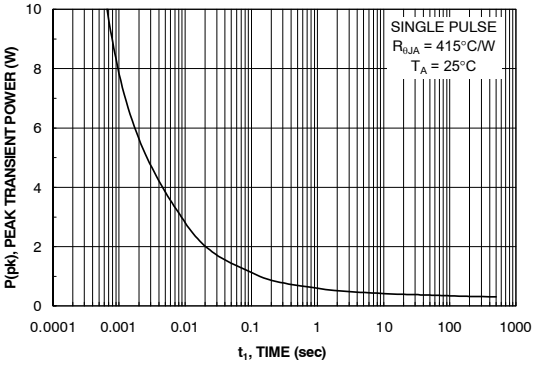


Figure 10. Single Pulse Maximum Power Dissipation

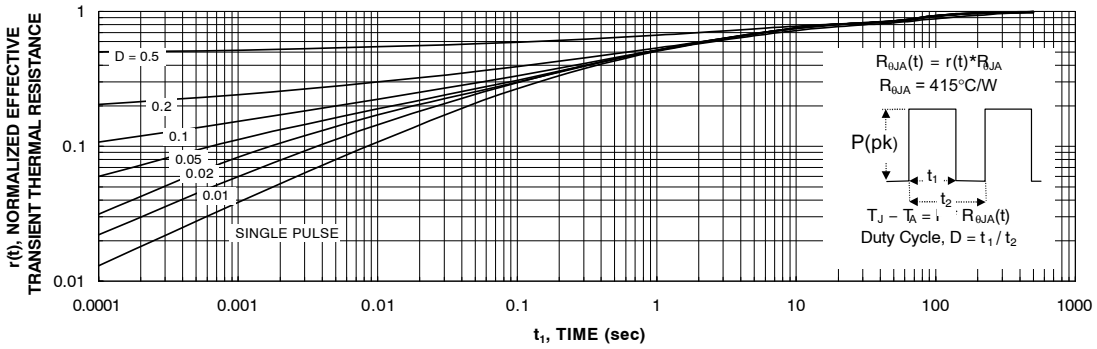
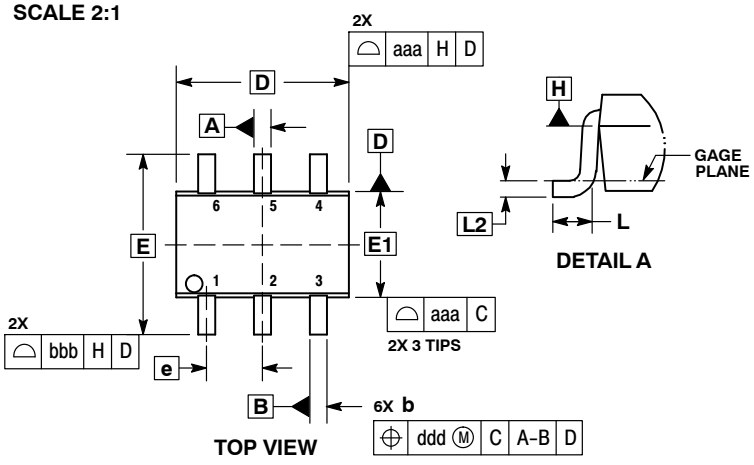


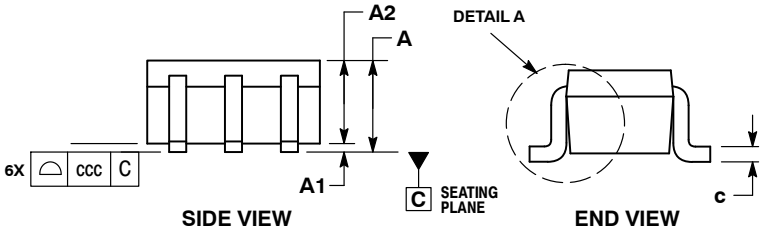
Figure 11. Transient Thermal Response Curve

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012

1
SCALE 2:1

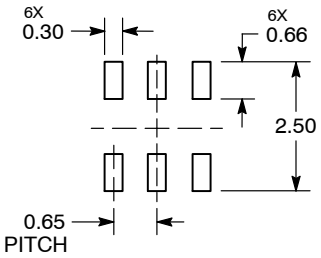




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	−−−	−−−	1.10	−−−	−−−	0.043
A1	0.00	−−−	0.10	0.000	−−−	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

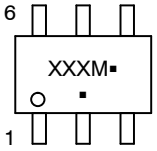
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

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STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

ISSUE	REVISION	DATE
H	REVISION TO CHANGE LEGAL OWNER OF DOCUMENT FROM MOTOROLA TO ON SEMICONDUCTOR. DELETED DIM “V” WAS 0.3 MM–0.4 MM/0.012–0.016 IN. REQ BY G KWONG	14 JUN 01
J	ADDED STYLE 20. REQ BY M. ATANOVICH.	11 OCT 01
K	UPDATED STYLE 15 WAS PIN 1, 2 AND 3: ANODE. PIN 4, 5, AND 6 CATHODE. ADDED STYLE 21. REQ BY M. ATANOVICH	03 APR 02
L	ADDED STYLE 22. REQ BY S. CHANG	25 OCT 02
M	ADDED STYLE 23. REQ BY B. BLACKMON	04 DEC 02
N	ADDED STYLE 24. REQ BY B. BLACKMON	09 JAN 03
P	ADDED STYLE 25. REQ BY S. CHANG	09 MAY 03
R	REMOVED THE “1” AFTER EMITTER. REQ BY S. CHANG	03 JUN 03
S	ADDED STYLE 26. REQ BY A. BINEYARD	18 AUG 03
T	ADDED STYLE 27. REQ. BY M. SWEADOR	23 OCT 2003
U	ADDED STYLES 28 AND 29. REQ. BY A. BINEYARD AND S. BACHMAN	22 JAN 2004
V	ADDED NOM VALUES AND CHANGED DIMS TO INDUSTRY STANDARD. REQ. BY D. TRUHITTE	31 JAN 2005
W	ADDED STYLE 30. REQ. BY L. DELUCA.	26 JAN 2006
Y	UPDATED & REDREW TO JEDEC STANDARDS. REQ. BY D. TRUHITTE.	11 DEC 2012

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

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