ON Semiconductor®

FDMC6676PZ

P-Channel Power Trench® MOSFET
-30 V, -20 A, 14.4 mΩ

Features

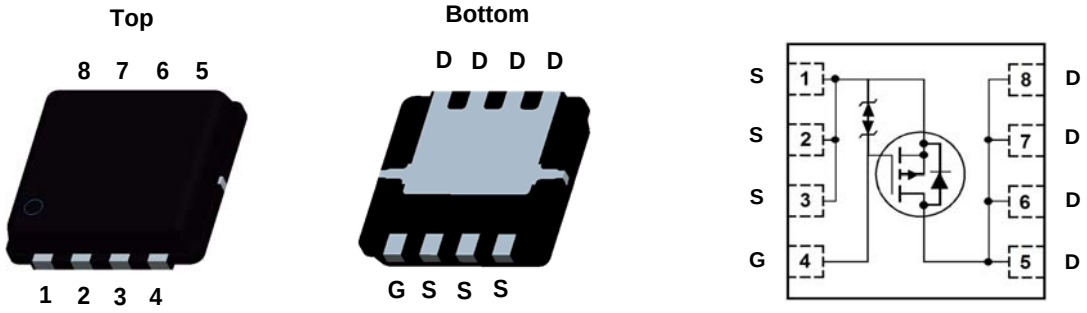
- Max $r_{DS(on)}$ = 14.4 mΩ at V_{GS} = -10 V, I_D = -9.5 A
- Max $r_{DS(on)}$ = 27.0 mΩ at V_{GS} = -4.5 V, I_D = -6.9 A
- HBM ESD protection level of 8 kV typical(note 3)
- Extended V_{GSS} range (-25 V) for battery applications
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability
- Termination is Lead-free and RoHS Compliant

General Description

The FDMC6676PZ has been designed to minimize losses in load switch applications. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ and ESD protection.

Application

- Load Switch in Notebook and Server
- Notebook Battery Pack Power Management



MLP 3.3x3.3

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			-30	V
V_{GS}	Gate to Source Voltage			±25	V
I_D	Drain Current -Continuous (Package limited)	T_C = 25 °C		-20	A
	-Continuous (Silicon limited)	T_C = 25 °C		-40	
	-Continuous	T_A = 25 °C	(Note 1a)	-9.5	
	-Pulsed			-32	
P_D	Power Dissipation	T_C = 25 °C		36	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		3.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	53	
$R_{\theta JB}$	Thermal Resistance, Junction to Board	(Note 1c)	7.4	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
WUCIN	FDMC6676PZ	MLP 3.3X3.3	13 ”	12 mm	3000 units

August-2017, Rev.2

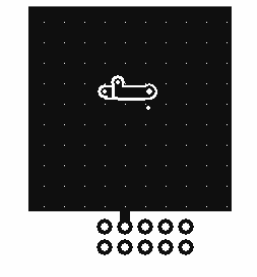
Publication Order Number:
FDMC6676PZ/D

Electrical Characteristics T_J = 25 °C unless otherwise noted

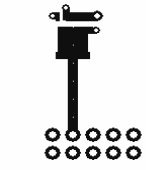
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250 μA, V_{GS} = 0 V	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		20		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-1	μA
		V_{DS} = -24 V, V_{GS} = 0 V, T_J = 125 °C			-100	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±25 V, V_{DS} = 0 V			±10	μA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250 μA	-1.0	-1.9	-3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -10 V, I_D = -9.5 A		10.7	14.4	mΩ
		V_{GS} = -4.5 V, I_D = -6.9 A		17.4	27.0	mΩ
		V_{GS} = -10 V, I_D = -9.5 A, T_J = 125 °C		15.2	20.5	mΩ
g_{FS}	Forward Transconductance	V_{DD} = -5 V, I_D = -9.5 A		28		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz		2154	2865	pF
C_{oss}	Output Capacitance			392	525	pF
C_{rss}	Reverse Transfer Capacitance			349	525	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -15 V, I_D = -9.5 A, V_{GS} = -10 V, R_{GEN} = 6 Ω		11	20	ns
t_r	Rise Time			10	20	ns
$t_{d(off)}$	Turn-Off Delay Time			44	71	ns
t_f	Fall Time			26	42	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to -10 V, V_{DD} = -15 V, I_D = -9.5 A		46	65	nC
	Total Gate Charge	V_{GS} = 0 V to -5 V, V_{DD} = -15 V, I_D = -9.5 A		26	37	nC
Q_{gs}	Gate to Source Charge	V_{DD} = -15 V, I_D = -9.5 A		6.4		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = -15 V, I_D = -9.5 A		13		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = -9.5 A (Note 2)		0.89	1.3	V
		V_{GS} = 0 V, I_S = -1.6 A (Note 2)		0.73	1.2	V
t_{rr}	Reverse Recovery Time	I_F = -9.5 A, di/dt = 100 A/μs		24	38	ns
Q_{rr}	Reverse Recovery Charge			15	27	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b.125 °C/W when mounted on a minimum pad of 2 oz copper

c. 7.4 °C/W when mounted on PCB and tested per EIA/JEDEC

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.

3. The diode connected between the gate and source servers only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics T_J = 25 °C unless otherwise noted

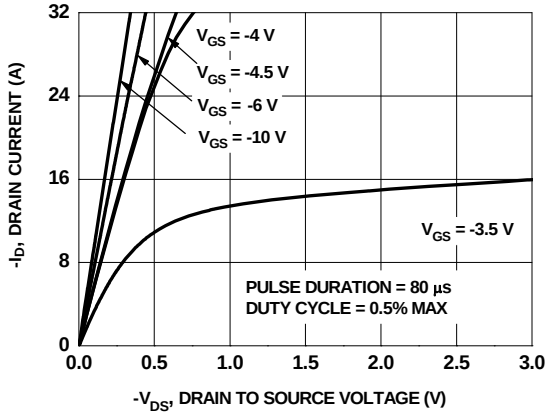


Figure 1. On Region Characteristics

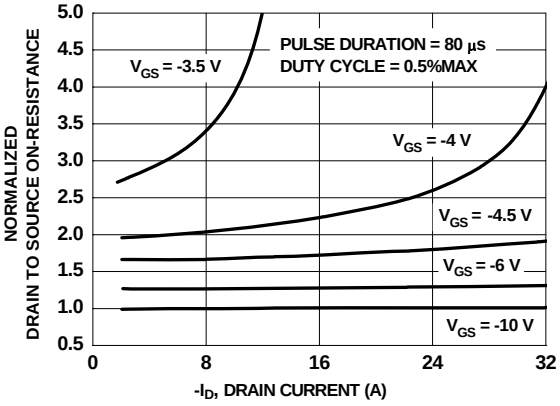


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

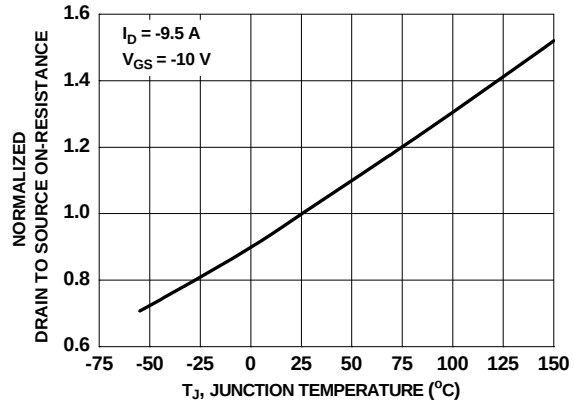


Figure 3. Normalized On Resistance vs Junction Temperature

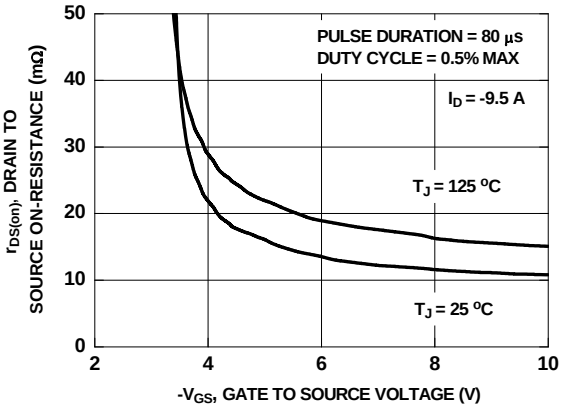


Figure 4. On-Resistance vs Gate to Source Voltage

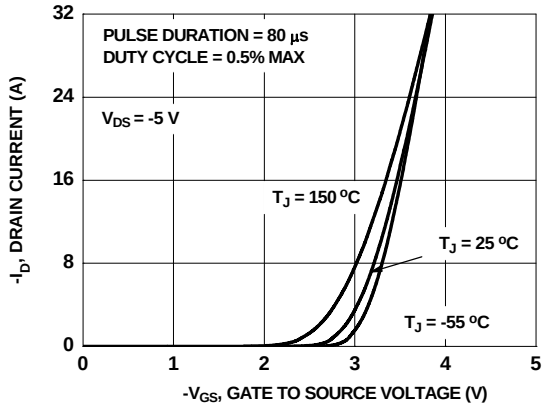


Figure 5. Transfer Characteristics

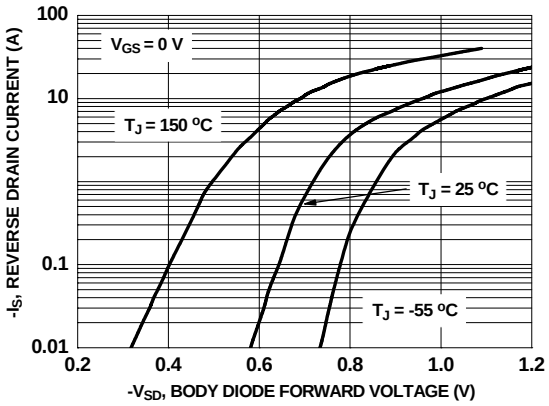


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

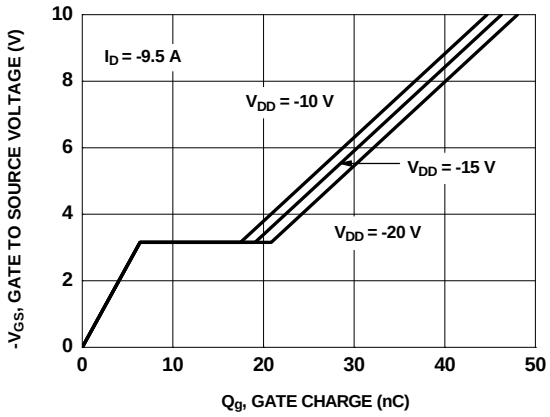


Figure 7. Gate Charge Characteristics

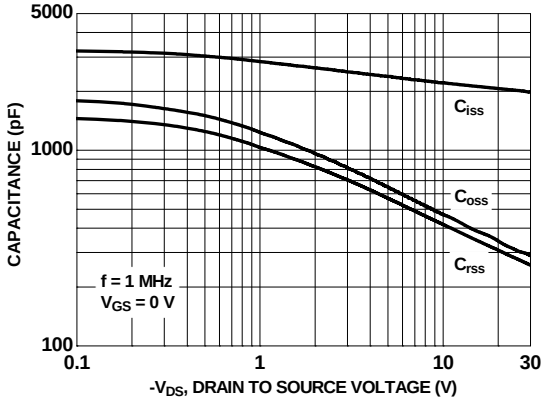


Figure 8. Capacitance vs Drain to Source Voltage

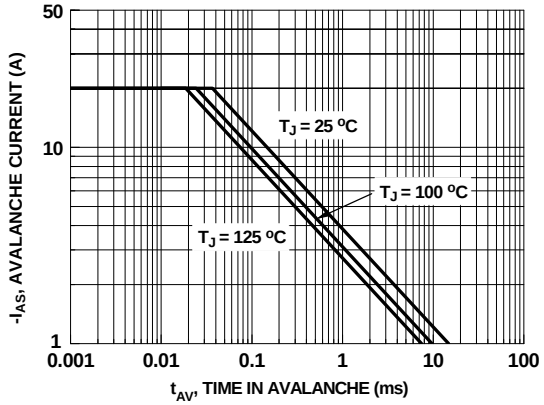


Figure 9. Unclamped Inductive Switching Capability

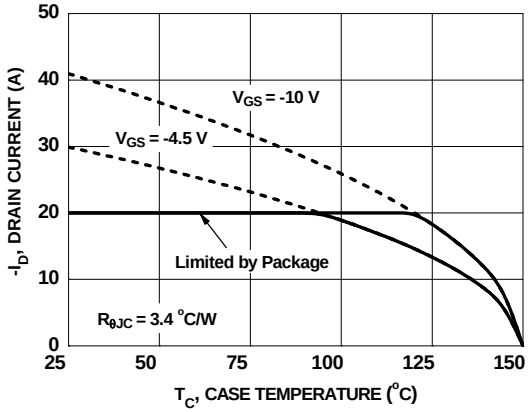


Figure 10. Maximum Continuous Drain Current vs Case Temperature

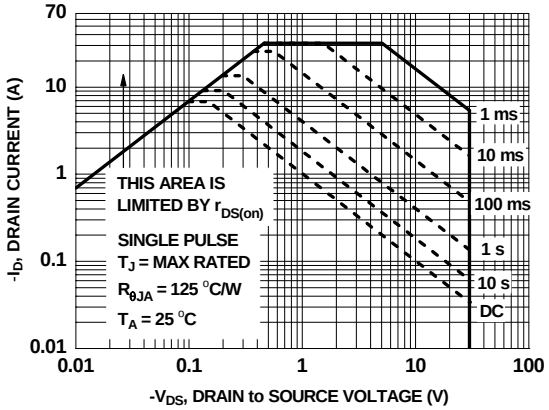


Figure 11. Forward Bias Safe Operating Area

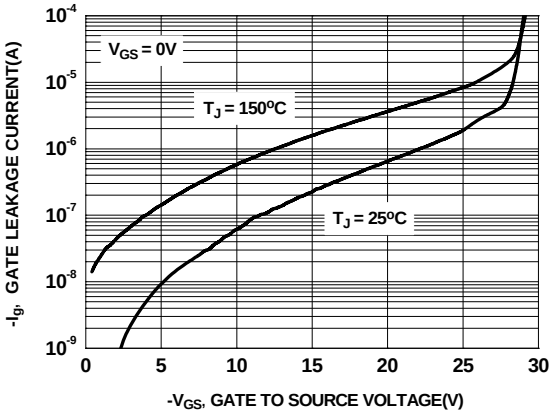


Figure 12. I_{gss} vs V_{gss}

Typical Characteristics T_J = 25 °C unless otherwise noted

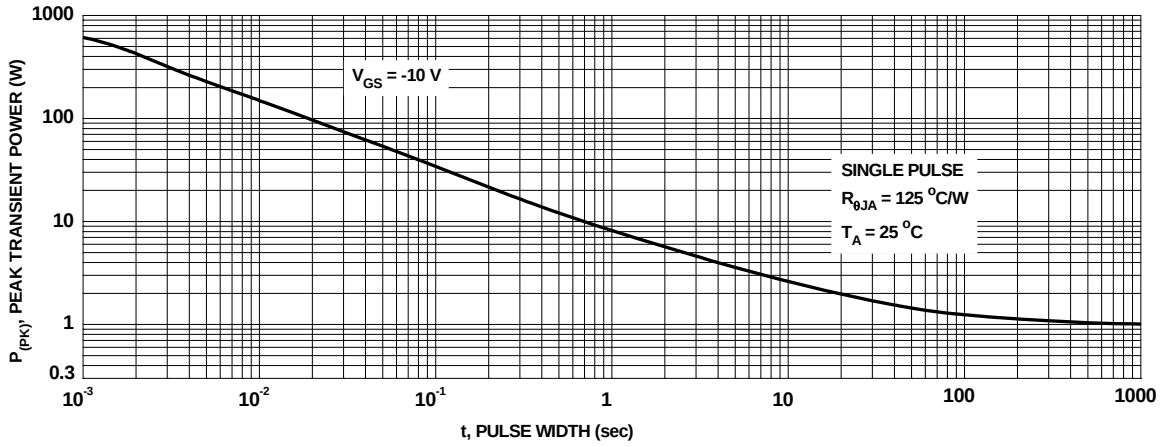


Figure 13. Single Pulse Maximum Power Dissipation

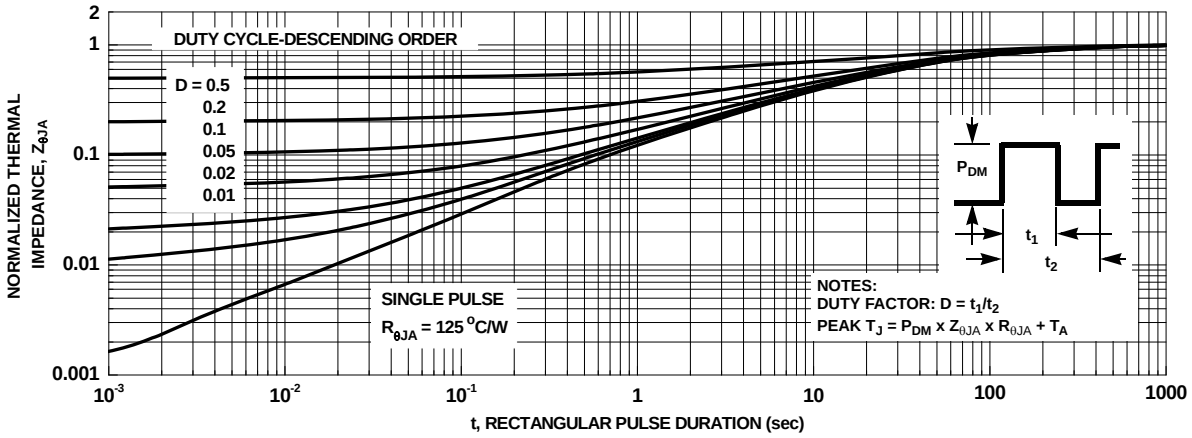
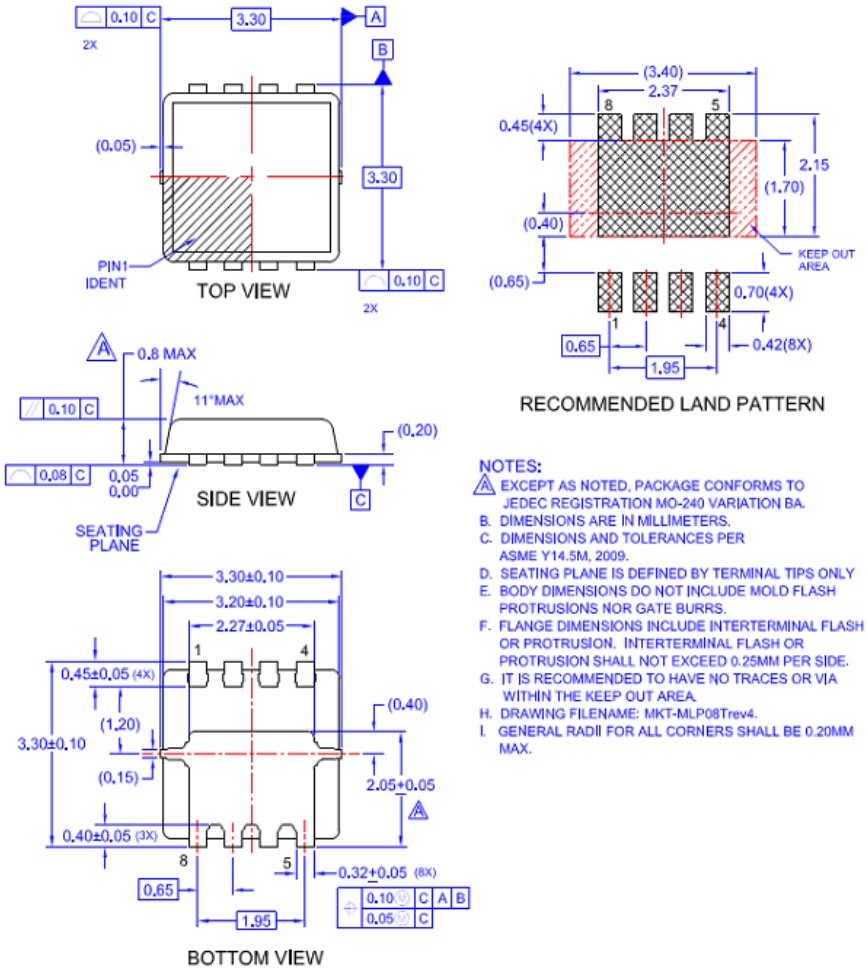


Figure 14. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout



NOTES:

A. EXCEPT AS NOTED, PACKAGE CONFORMS TO JEDEC REGISTRATION MO-240 VARIATION BA.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
D. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY
E. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS.
F. FLANGE DIMENSIONS INCLUDE INTERTERMINAL FLASH OR PROTRUSION. INTERTERMINAL FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.
G. IT IS RECOMMENDED TO HAVE NO TRACES OR VIA WITHIN THE KEEP OUT AREA.
H. DRAWING FILENAME: MKT-MLP08Trev4.
I. GENERAL RADII FOR ALL CORNERS SHALL BE 0.20MM MAX.

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