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February 2015

# FDMC6688P

## P-Channel PowerTrench<sup>®</sup> MOSFET

-20 V, -56 A, 6.5 mΩ

### Features

- Max  $r_{DS(on)}$  = 6.5 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -14$  A
- Max  $r_{DS(on)}$  = 9.8 mΩ at  $V_{GS} = -2.5$  V,  $I_D = -11$  A
- Max  $r_{DS(on)}$  = 20 mΩ at  $V_{GS} = -1.8$  V,  $I_D = -9$  A
- High performance trench technology for extremely low  $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- Lead-free and RoHS Compliant

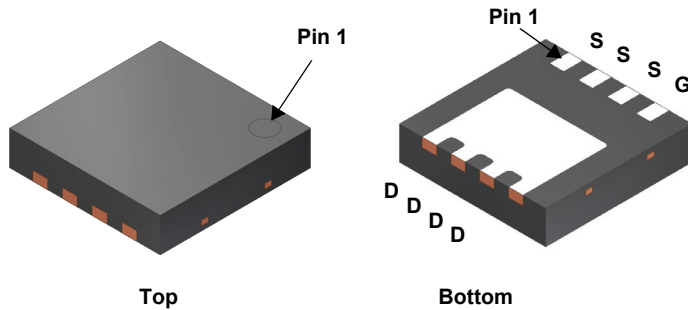


### General Description

This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that has been optimized for  $r_{DS(ON)}$ , switching performance and ruggedness.

### Applications

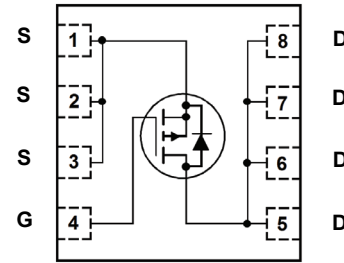
- Load Switch
- Battery Management
- Power Management
- Reverse Polarity Protection



Top

Bottom

Power 33



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	-20	V
$V_{GS}$	Gate to Source Voltage	±8	V
$I_D$	Drain Current -Continuous $T_C = 25$ °C	-56	A
	-Continuous $T_A = 25$ °C (Note 1a)	-14	
	-Pulsed (Note 3)	-226	
$P_D$	Power Dissipation $T_C = 25$ °C	30	W
	Power Dissipation $T_A = 25$ °C (Note 1a)	2.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC6688P	FDMC6688P	Power 33	13 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-16		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}$ , $V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 8\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = -250\text{ }\mu\text{A}$	-0.4	-0.75	-1	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		3		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -4.5\text{ V}$ , $I_D = -14\text{ A}$		5.3	6.5	m $\Omega$
		$V_{GS} = -2.5\text{ V}$ , $I_D = -11\text{ A}$		7	9.8	
		$V_{GS} = -1.8\text{ V}$ , $I_D = -9\text{ A}$		10.7	20	
		$V_{GS} = -4.5\text{ V}$ , $I_D = -14\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		7.3	11	
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}$ , $I_D = -14\text{ A}$		80		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -10\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		4956	7435	pF
$C_{oss}$	Output Capacitance			678	1020	pF
$C_{rss}$	Reverse Transfer Capacitance			618	930	pF
$R_g$	Gate Resistance			4.5		$\Omega$

### Switching Characteristics

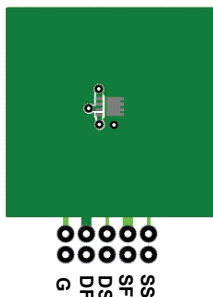
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -10\text{ V}$ , $I_D = -14\text{ A}$ , $V_{GS} = -4.5\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		19	35	ns	
$t_r$	Rise Time			33	53	ns	
$t_{d(off)}$	Turn-Off Delay Time			119	190	ns	
$t_f$	Fall Time			68	109	ns	
$Q_g$	Total Gate Charge		$V_{DD} = -10\text{ V}$ , $I_D = -14\text{ A}$ , $V_{GS} = -4.5\text{ V}$		44	61	nC
$Q_{gs}$	Gate to Source Charge				7.4		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			11		nC	

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = -14\text{ A}$ (Note 2)		-0.8	-1.2	V
		$V_{GS} = 0\text{ V}$ , $I_S = -2\text{ A}$ (Note 2)		-0.6	-1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = -14\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		26	41	ns
$Q_{rr}$	Reverse Recovery Charge			10	20	nC

#### Notes:

1:  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



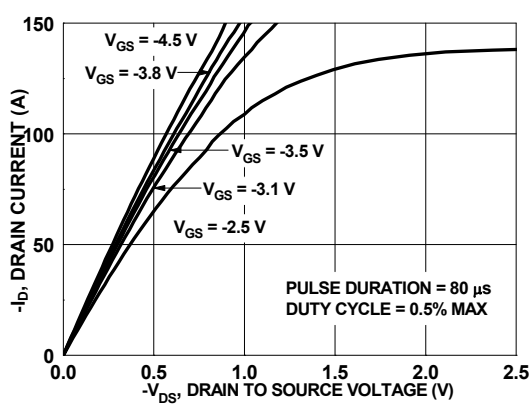
a. 53  $^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



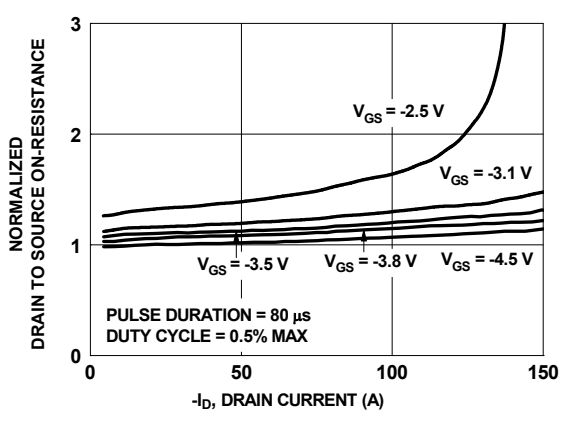
b. 125  $^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

2: Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0 %.  
3: Pulse  $I_d$  refers to Forward Bias Safe Operation Area.

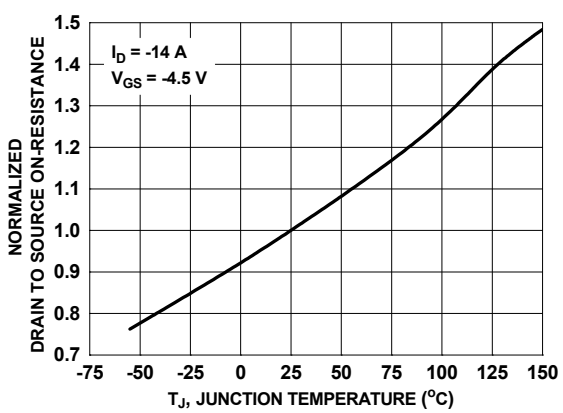
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



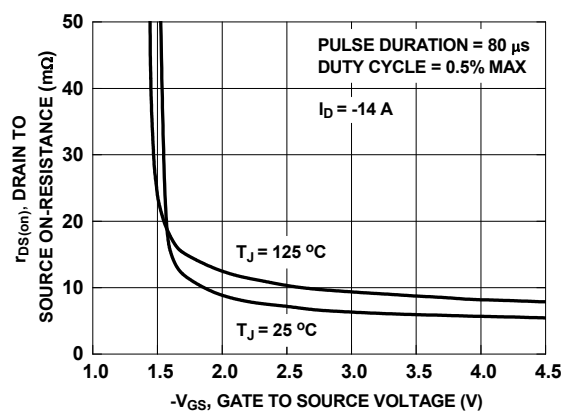
**Figure 1. On Region Characteristics**



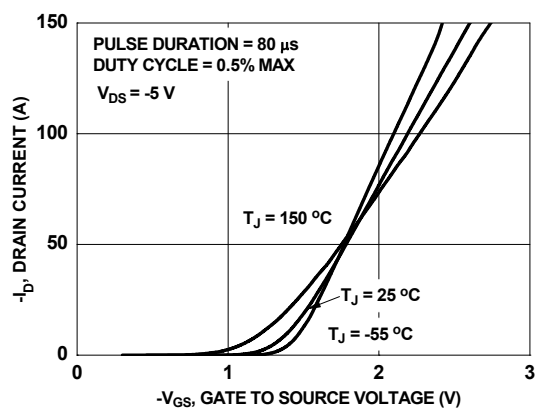
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



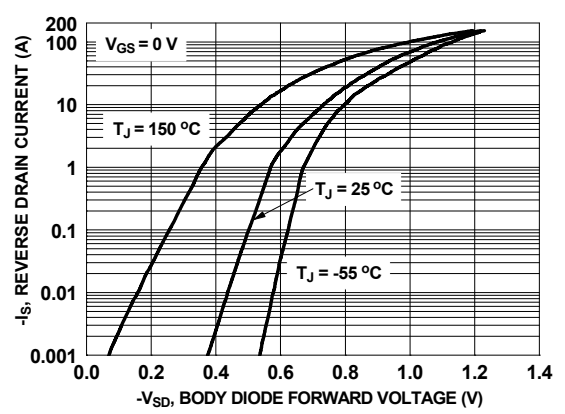
**Figure 3. Normalized On Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

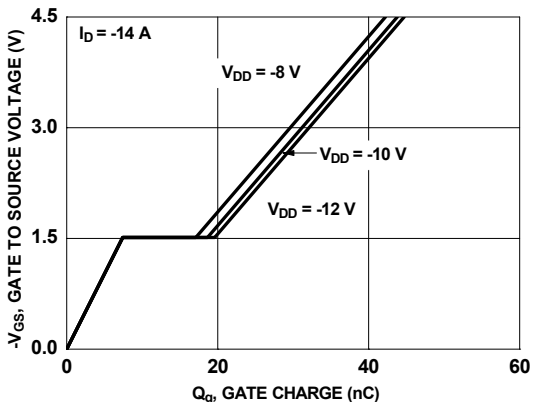


**Figure 5. Transfer Characteristics**

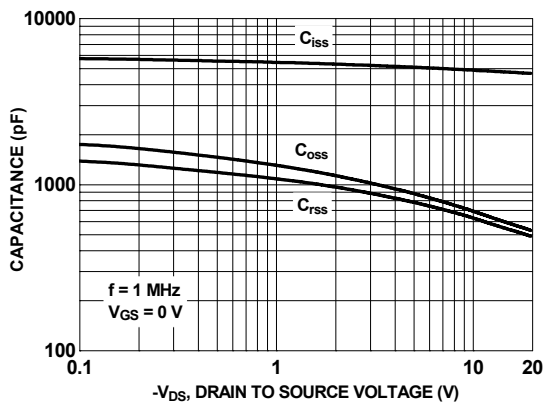


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

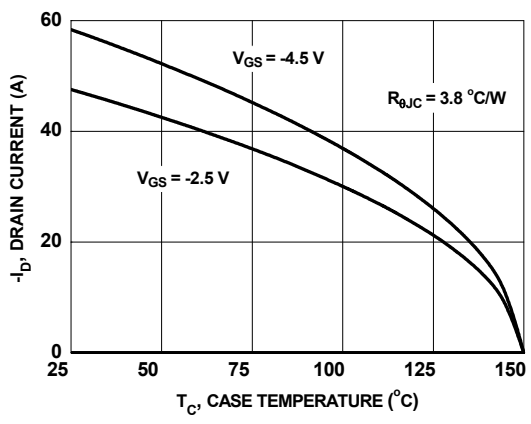
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



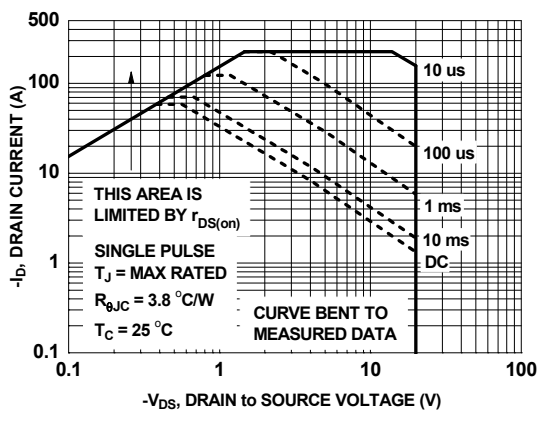
**Figure 7. Gate Charge Characteristics**



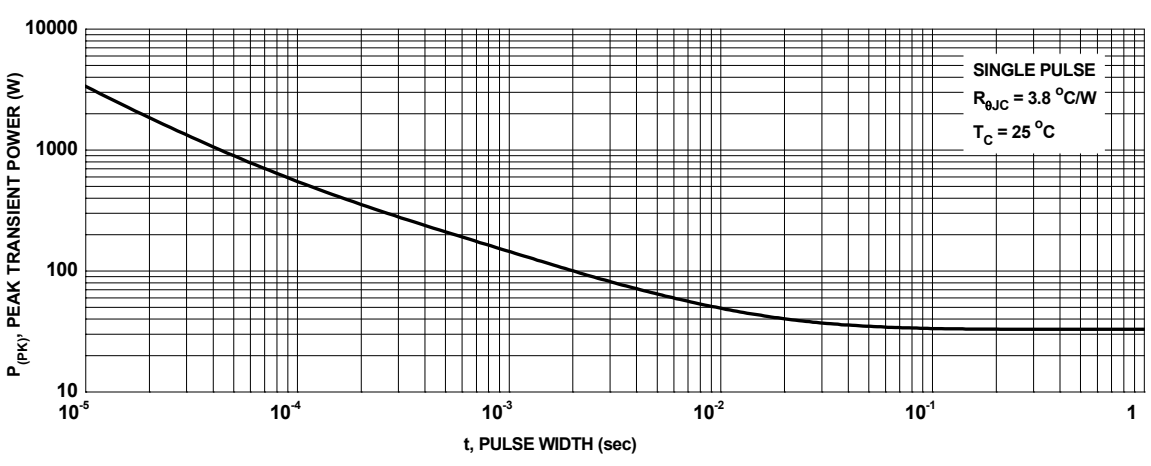
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Maximum Continuous Drain Current vs Case Temperature**

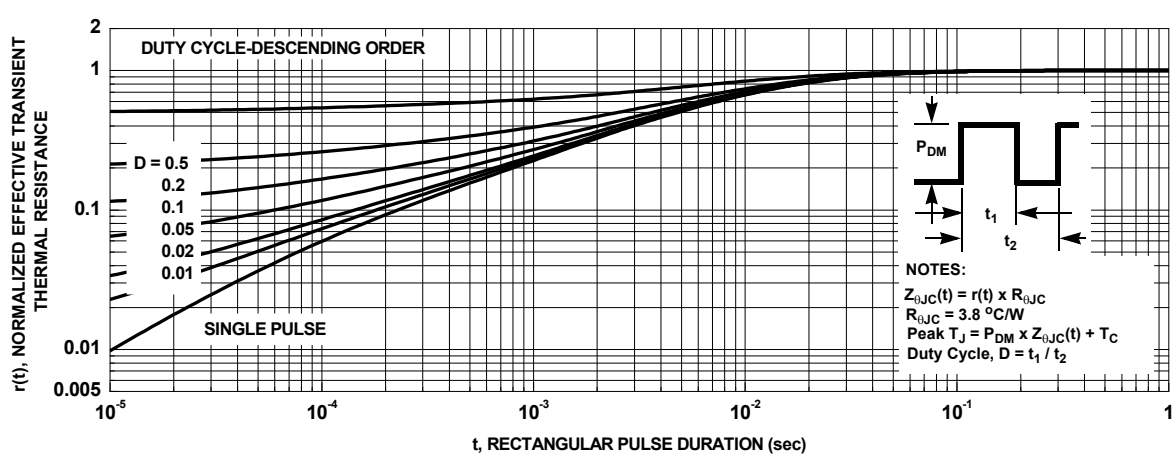


**Figure 10. Forward Bias Safe Operating Area**

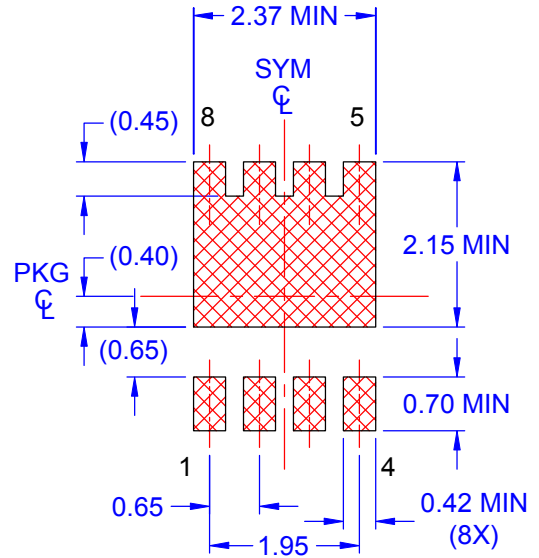
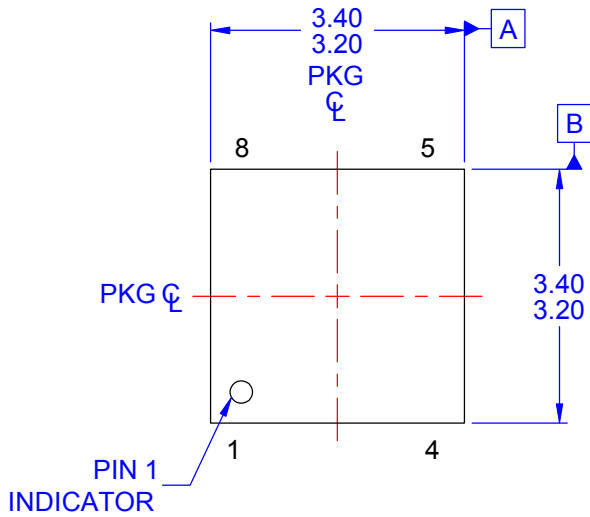


**Figure 11. Single Pulse Maximum Power Dissipation**

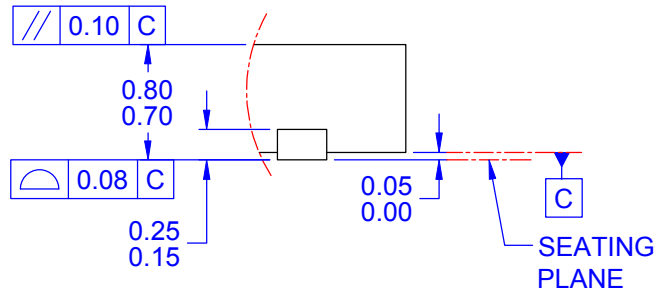
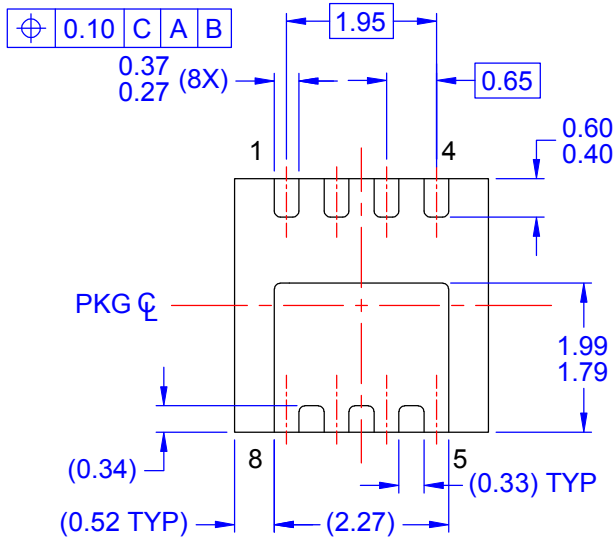
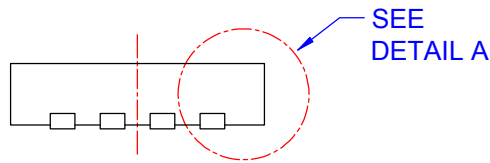
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 12. Junction-to-Case Transient Thermal Response Curve**



LAND PATTERN RECOMMENDATION



DETAIL A  
SCALE: 2X

NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E) DRAWING FILE NAME: MKT-PQFN08SREV1



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