FDMC8010ET30

MOSFET – N-Channel, POWERTRENCH®
30 V, 174 A, 1.3 mΩ

General Description

This N−Channel MOSFET is produced using ON Semiconductor's advanced POWERTRENCH process that has been especially tailored to minimize the on−state resistance. This device is well suited for applications where ultra low $r_{DS(on)}$ is required in small spaces such as High performance VRM, POL and Oring functions.

Features

- Extended T_J Rating to 175°C
- Max $r_{DS(on)}$ = 1.3 mΩ at V_{GS} = 10 V, I_D = 30 A
- Max $r_{DS(on)}$ = 1.8 mΩ at V_{GS} = 4.5 V, I_D = 25 A
- High Performance Technology for Extremely Low $r_{DS(on)}$
- These Devices are Pb−Free and are RoHS Compliant

Applications

- DC – DC Buck Converters
- Point of Load
- High Efficiency Load Switch and Low Side Switching
- Oring FET

MOSFET MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Volage (Note 4)	±20	V
I_D	Drain Current −Continuous T_C = 25°C (Note 6) −Continuous T_C = 100°C (Note 6) −Continuous T_A = 25°C (Note 1a) −Pulsed (Note 5)	 174 123 30 835	A
E_{AS}	Single Pulse Avalance Energy (Note 3)	153	mJ
P_D	Power Dissipation T_C = 25°C	65	W
	Power Dissipation T_A = 25°C (Note 1a)	2.8	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	°C/W

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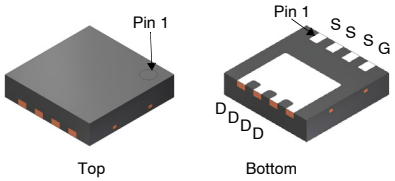
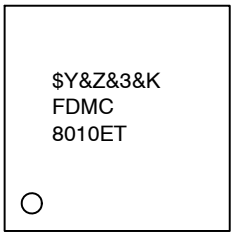
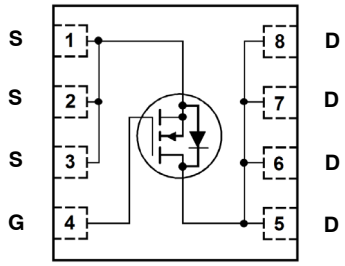


PQFN8 3.3x3.3, 0.65P
CASE 483AW
Power 33

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDMC8010ET	= Specific Device Code



ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 2 of this data sheet.

PACKAGE MARKING AND ORDERING INFORMATION

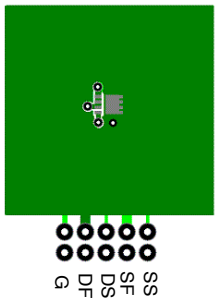
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8010ET	FDMC8010ET30	Power 33	13”	12 mm	3000 Units

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

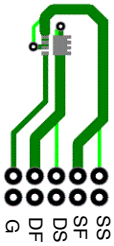
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0 V	30			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, referenced to 25°C		15		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 1 mA	1.2	1.5	2.5	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 1 mA, referenced to 25°C		−5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 30 A		0.9	1.3	mΩ
		V_{GS} = 4.5 V, I_D = 25 A		1.3	1.8	
		V_{GS} = 10 V, I_D = 30 A, T_J = 125°C		1.3	2	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 30 A		188		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz		4405	5860	pF
C_{oss}	Output Capacitance			1570	2090	pF
C_{rss}	Reverse Transfer Capacitance			167	250	pF
R_g	Gate Resistance		0.1	0.5	1.25	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 15 V, I_D = 30 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		15	27	ns
t_r	Rise Time			7.5	15	ns
$t_{d(off)}$	Turn−Off Delay Time			40	64	ns
t_f	Fall Time			5.3	11	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 15 V, I_D = 30 A		67	94	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V; V_{DD} = 15 V, I_D = 30 A		32	45	nC
Q_{gs}	Gate to Source Charge			10		nC
Q_{gd}	Gate to Drain “Miller” Charge			9.5		nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A (Note 2)		0.6	1.2	V
		V_{GS} = 0 V, I_S = 30 A (Note 2)		0.7	1.2	
t_{rr}	Reverse Recovery Time	I_F = 30 A, di/dt = 100 A/μs		49	78	ns
Q_{rr}	Reverse Recovery Charge			29	46	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta CA}$ is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.
3. E_{AS} of 153 mJ is based on starting T_J = 25°C, L = 0.3 mH, I_{AS} = 32 A, V_{DD} = 27 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 47 A.
4. As an N−ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.
5. Pulsed Id please refer to Figure 11 SOA graph for more details.
6. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro−mechanical application board design.

TYPICAL CHARACTERISTICS

T_J = 25°C Unless Otherwise Noted

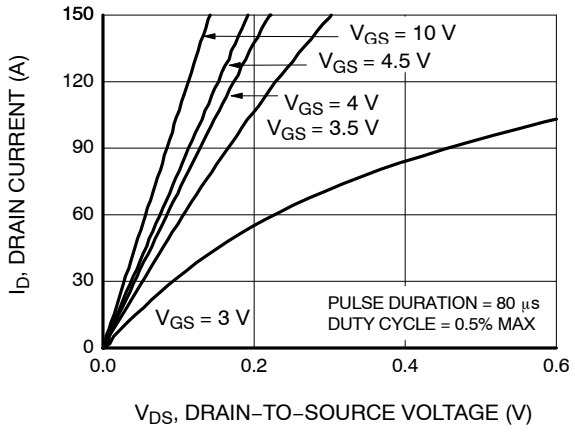


Figure 1. On−Region Characteristics

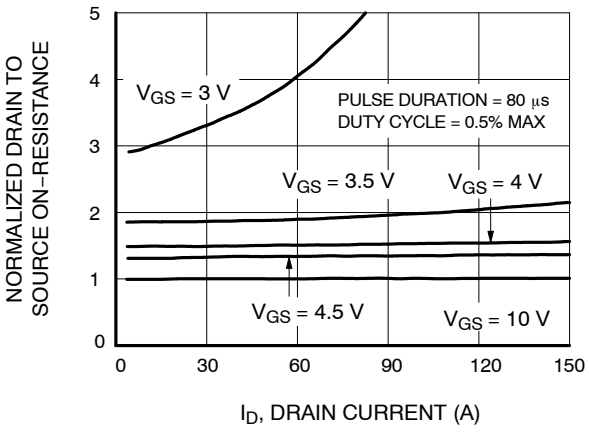


Figure 2. Normalized On−Resistance vs Drain Current and Gate Voltage

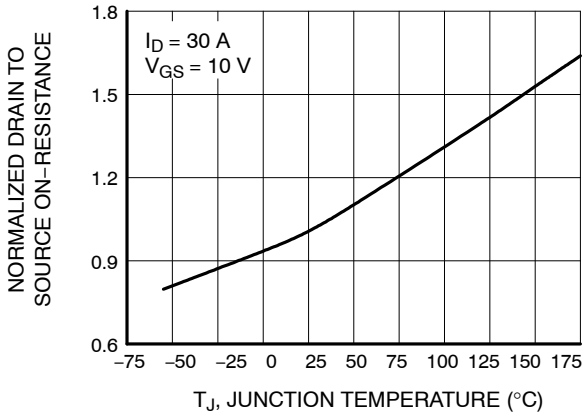


Figure 3. Normalized On Resistance vs Junction Temperature

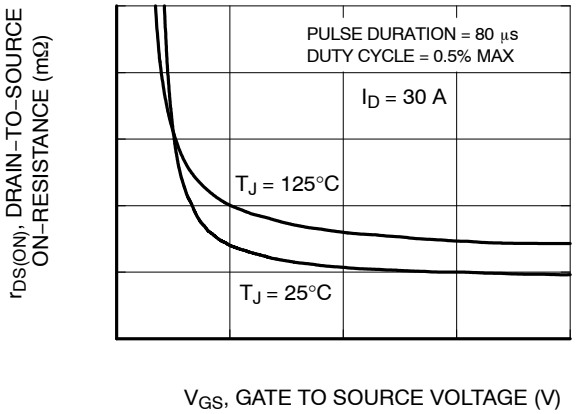


Figure 4. On−Resistance vs Gate to Source Voltage

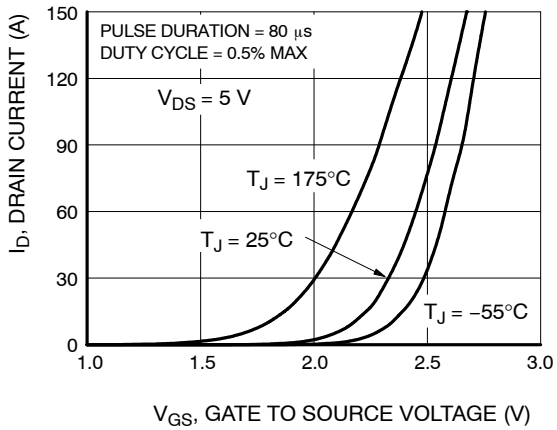


Figure 5. Transfer Characteristics

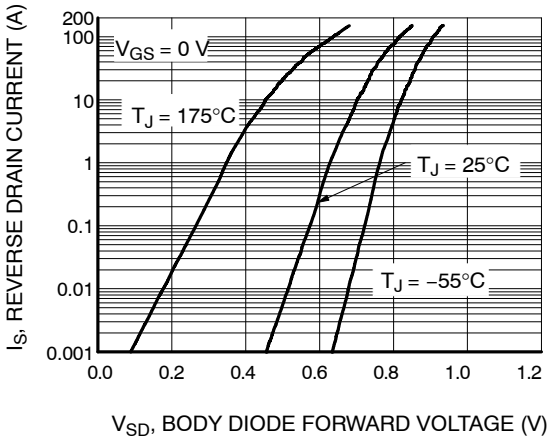


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (continued)

T_J = 25°C Unless Otherwise Noted

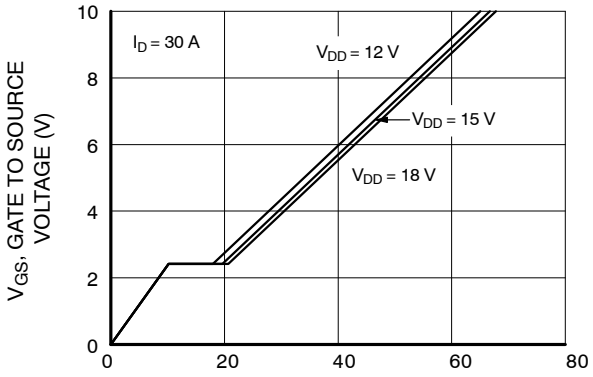


Figure 7. Gate Charge Characteristics

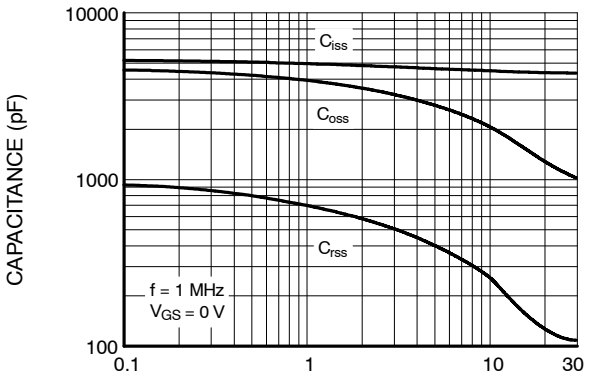


Figure 8. Capacitance vs Drain to Source Voltage

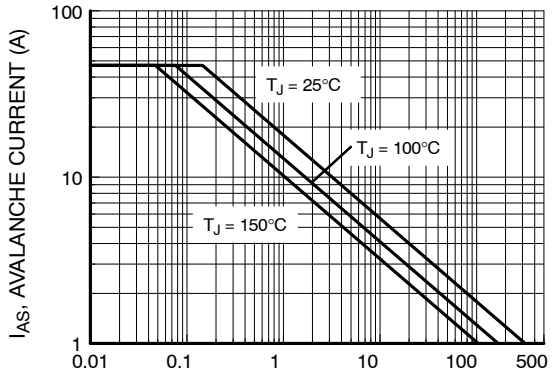


Figure 9. Unclamped Inductive Switching Capability

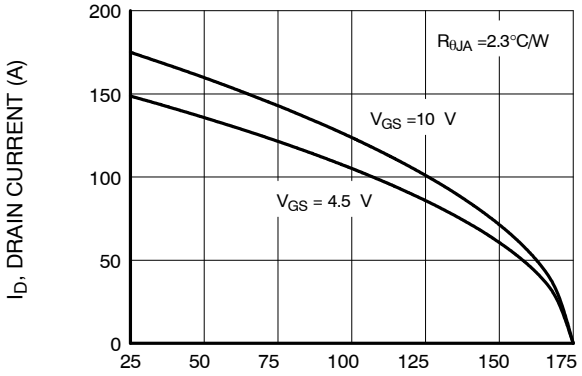


Figure 10. Maximum Continuous Drain Current vs Case Temperature

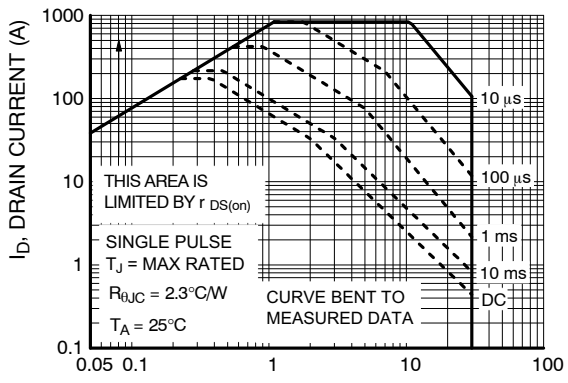


Figure 11. Forward Bias Safe Operating Area

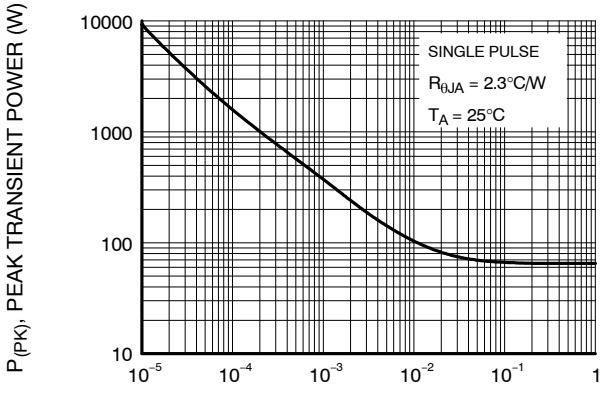


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

T_J = 25°C Unless Otherwise Noted

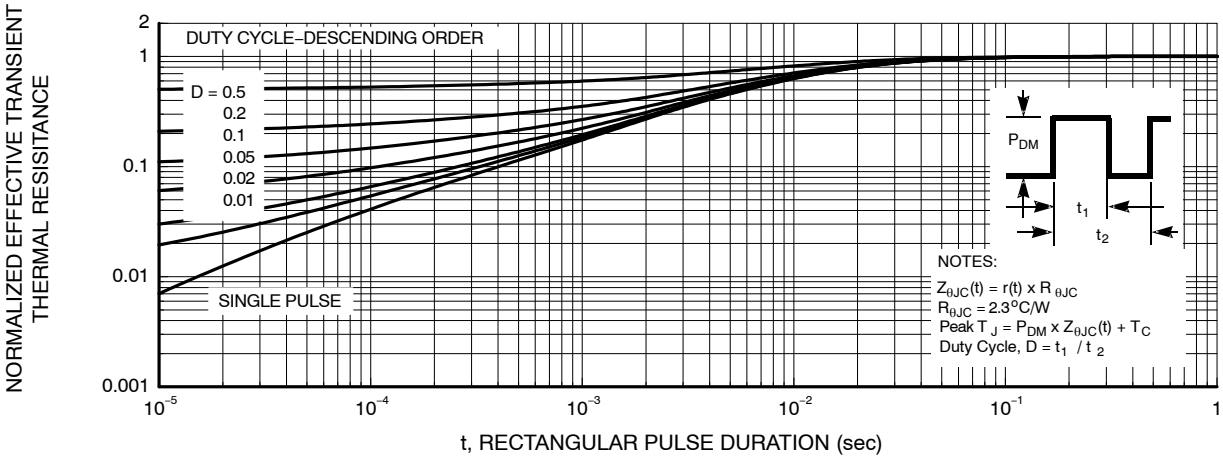
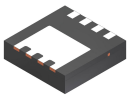


Figure 13. Junction−to−Ambient Transient Thermal Response Curve

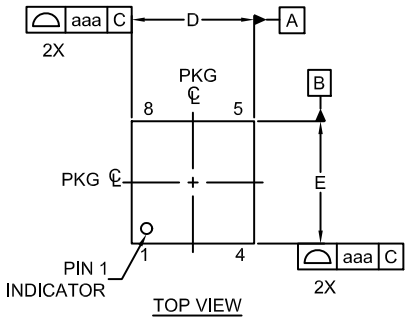
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

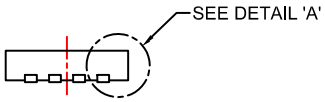


WDFN8 3.3X3.3, 0.65P
CASE 483AW
ISSUE A

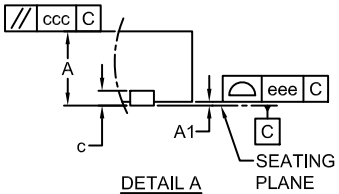
DATE 10 SEP 2019



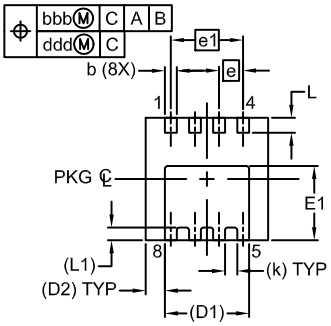
TOP VIEW



FRONT VIEW

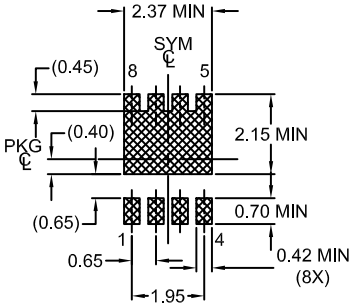


DETAIL A
SCALE: 2x



BOTTOM VIEW

LAND PATTERN RECOMMENDATION*



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS.
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	-	0.05
b	0.27	0.32	0.37
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.27 REF		
D2	0.52 REF		
E	3.20	3.30	3.40
E1	1.85	1.95	2.05
e	0.65 BSC		
e1	1.95 BSC		
k	0.33 REF		
L	0.30	0.40	0.50
L1	0.34 REF		
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.05		

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WDFN8 3.3X3.3, 0.65P**	**PAGE 1 OF 1**

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