

MOSFET - N-Channel Shielded Gate PowerTrench®



ON Semiconductor®

www.onsemi.com

FDMC86106LZ-P 100 V, 103 mΩ, 7.5 A

This N-Channel logic Level MOSFETs are produced using ON Semiconductor's advanced PowerTrench process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance. G-S zener has been added to enhance ESD voltage level.

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 103 mΩ at $V_{GS} = 10$ V, $I_D = 3.3$ A
- Max $r_{DS(on)}$ = 153 mΩ at $V_{GS} = 4.5$ V, $I_D = 2.7$ A
- HBM ESD Protection Level > 1.8 KV typical (Note 4)
- 100% UIL Tested
- RoHS Compliant

Application

- DC – DC Conversion

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	100	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $T_C = 25^\circ\text{C}$	(Package limited)	I_D 7.5	A
	(Silicon limited)	9.6	
Continuous Drain Current $T_A = 25^\circ\text{C}$	(Figure 1)	3.3	
		15	
Pulsed Drain Current		15	
Single Pulse Avalanche Energy	(Note 3)	E_{AS} 12	mJ
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D 19	W
	$T_A = 25^\circ\text{C}$ (Figure 1)	2.3	
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

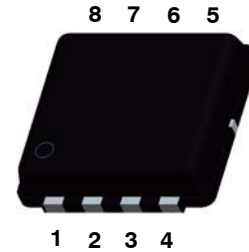
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

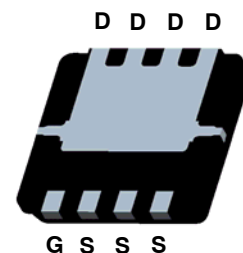
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	6.5	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient (Figure 1)	$R_{\theta JA}$	53	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Reel Size	Tape Width	Quantity
FDMC86106Z	FDMC86106LZ-P	Power 33	13"	12 mm	3000 units

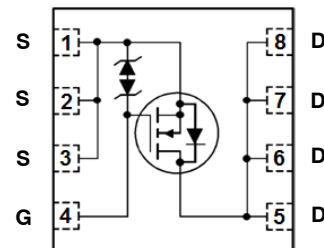


(Top View)



(Bottom View)

WDFN8
CASE 511DR



FDMC86106LZ-P

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain-to-Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	100	-	-	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	-	73	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 80 V, V _{GS} = 0 V	-	-	1	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	-	-	±10	μA

ON CHARACTERISTICS

V _{GS(th)}	Gate-to-Source Threshold Voltage	I _D = 250 μA, V _{GS} = V _{DS}	1.0	1.8	2.2	V
ΔV _{GS(th)} /ΔT _J	Gate-to-Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	-	-6	-	mV/°C
R _{DS(on)}	Static Drain-to-Source On Resistance	V _{GS} = 10 V, I _D = 3.3 A	-	79	103	mΩ
		V _{GS} = 4.5 V, I _D = 2.7 A	-	105	153	
		V _{GS} = 10 V, I _D = 3.3 A, T _J = 125°C	-	136	178	
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 3.3 A	-	11	-	S

DYNAMIC CHARACTERISTICS

C _{ISS}	Input Capacitance	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz	-	232	310	pF
C _{OSS}	Output Capacitance		-	45	60	pF
C _{RSS}	Reverse Transfer Capacitance		-	2.4	5	pF
R _g	Gate Resistance		-	0.7	-	Ω

SWITCHING CHARACTERISTICS

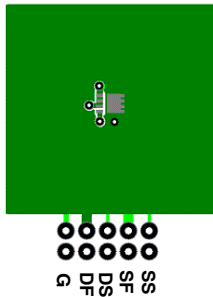
t _{d(on)}	Turn-On Delay Time	V _{DD} = 50 V, I _D = 3.3 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	-	4.5	10	ns
t _r	Rise Time		-	1.3	10	
t _{d(off)}	Turn-Off Delay Time		-	10	20	
t _f	Fall Time		-	1.4	10	
Q _{g(tot)}	Total Gate Charge	V _{GS} = 0 to 10 V, V _{DD} = 50 V, I _D = 3.3 A	-	4	6	nC
Q _{g(tot)}	Total Gate Charge	V _{GS} = 0 to 4.5 V, V _{DD} = 50 V, I _D = 3.3 A	-	2	3	
Q _{gs}	Gate-to-Source Gate Charge	V _{DD} = 50 V, I _D = 3.3 A	-	0.8	-	
Q _{gd}	Gate-to-Drain "Miller" Charge		-	0.7	-	

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source-to-Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 3.3 A (Note 2)	-	0.85	1.3	V
		V _{GS} = 0 V, I _S = 2 A (Note 2)	-	0.82	1.2	
t _{rr}	Reverse Recovery Time	I _F = 3.3 A, di/dt = 100 A/μs	-	33	54	ns
Q _{rr}	Reverse Recovery Charge		-	23	38	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- R_{θJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a. 53°C/W when mounted on a 1 in² pad of 2 oz copper

Figure 1.



b. 125°C/W when mounted on a minimum pad of 2 oz copper

Figure 2.

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- Starting T_J = 25°C; N-ch: L = 1.0 mH, I_{AS} = 5.0 A, V_{DD} = 90 V, V_{GS} = 10 V.
- The diode connected between gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

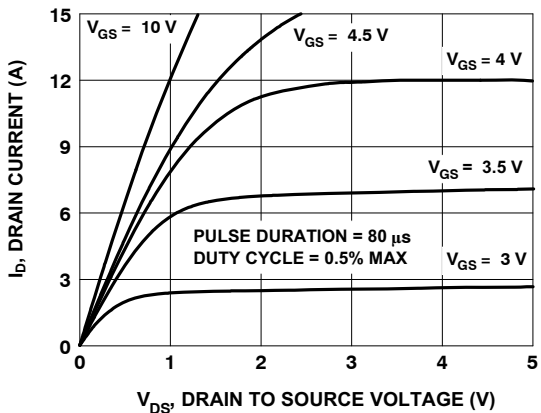


Figure 3. On Region Characteristics

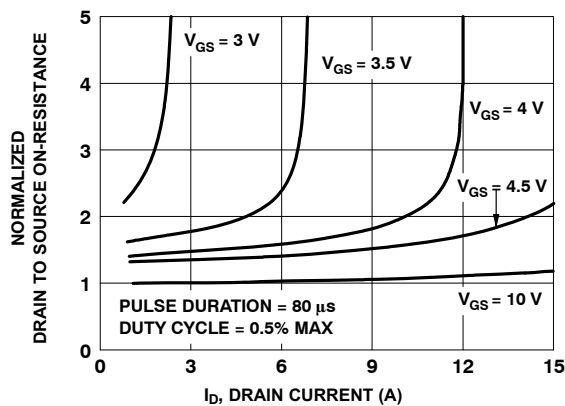


Figure 4. Normalized On-Resistance vs. Drain Current and Gate Voltage

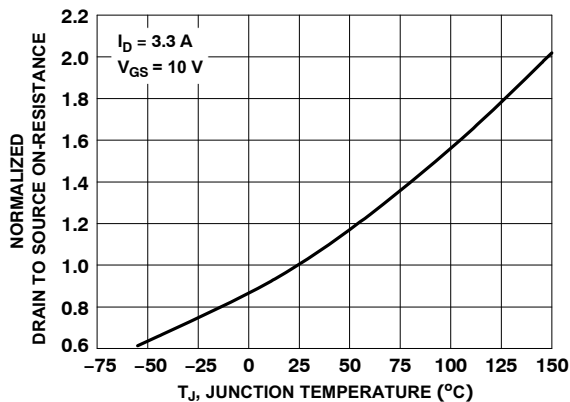


Figure 5. Normalized On Resistance vs. Junction Temperature

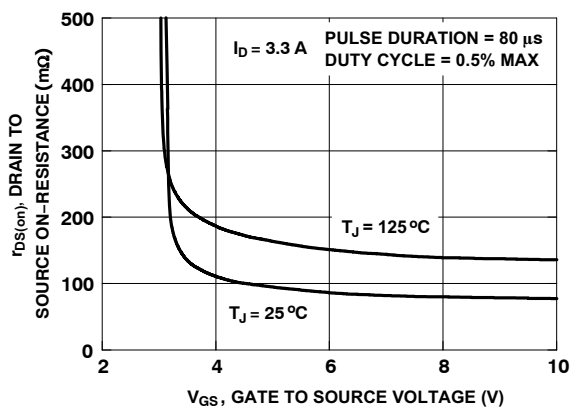


Figure 6. On-Resistance vs. Gate-to-Source Voltage

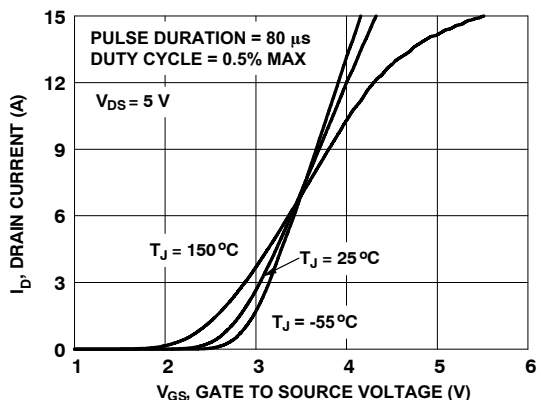


Figure 7. Transfer Characteristics

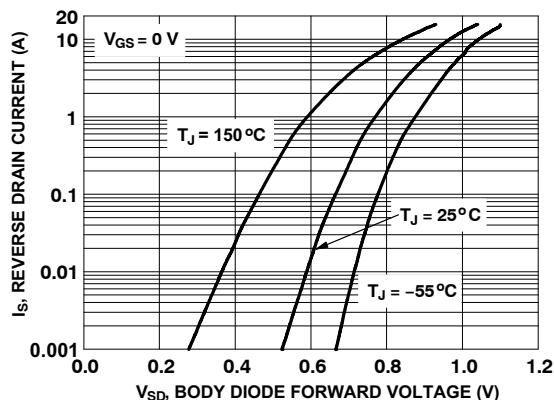


Figure 8. Source-to-Drain Diode Forward Voltage vs. Source Current

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TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

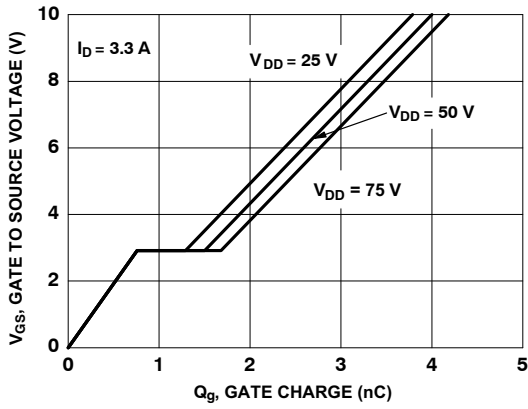


Figure 9. Gate Charge Characteristics

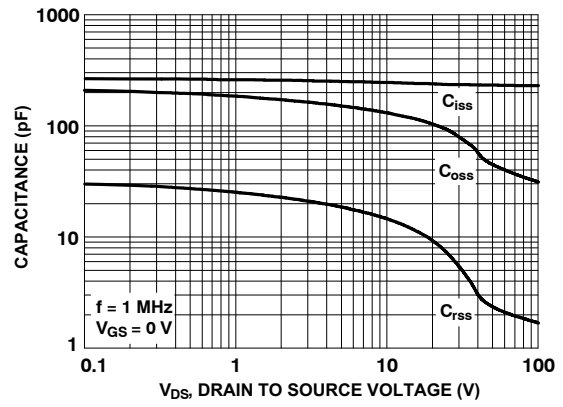


Figure 10. Capacitance vs. Drain-to-Source Voltage

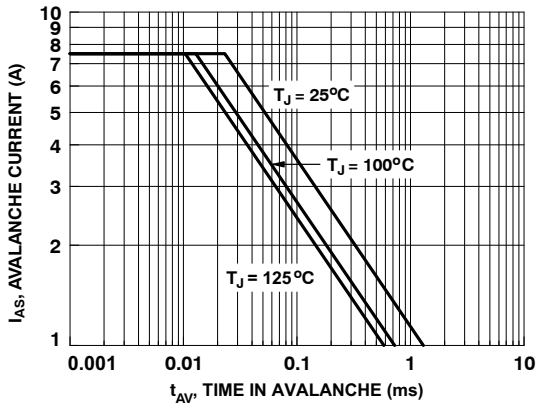


Figure 11. Unclamped Inductive Switching Capability

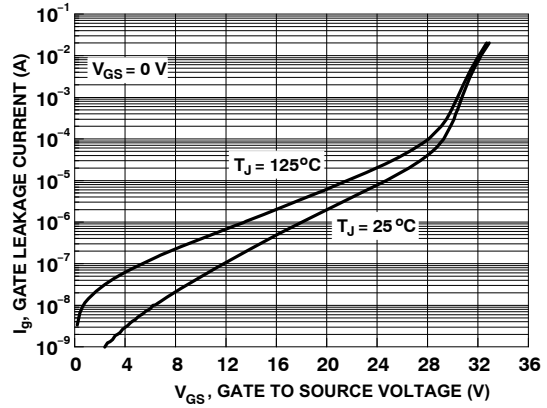


Figure 12. Gate Leakage Current vs. Gate-to-Source Voltage

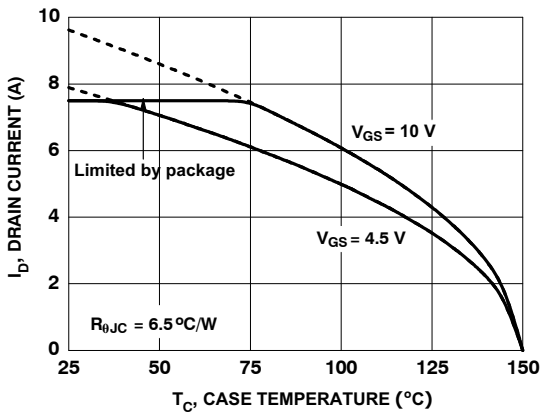


Figure 13. Maximum Continuous Drain Current vs. Case Temperature

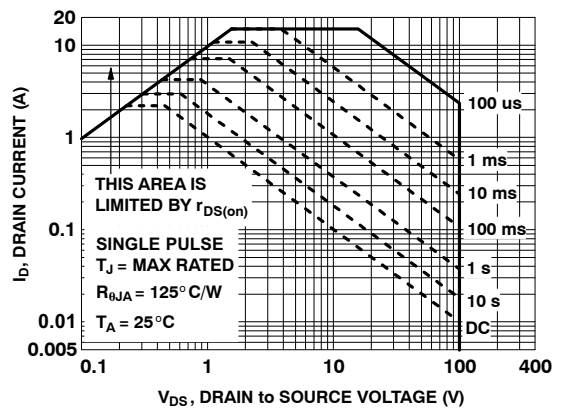


Figure 14. Forward Bias Safe Operating Area

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TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

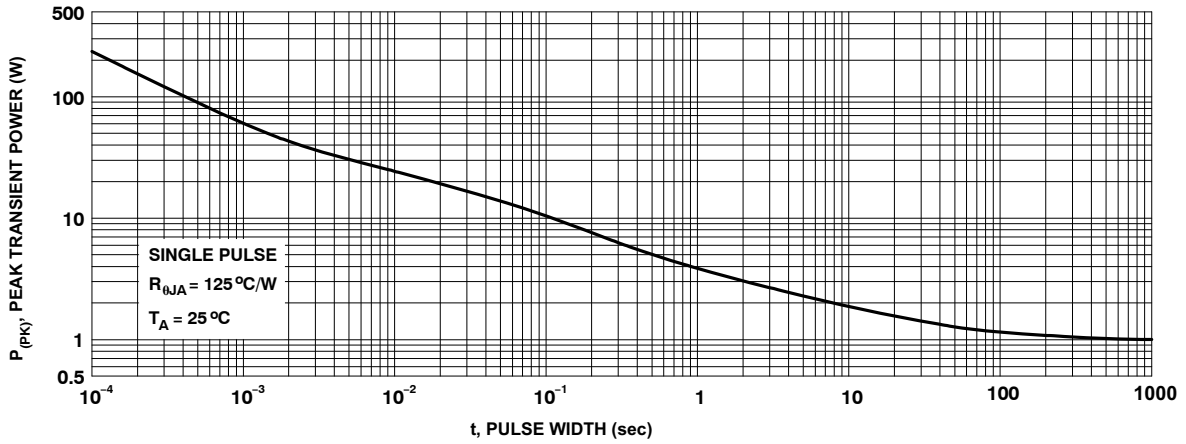


Figure 15. Single Pulse Maximum Power Dissipation

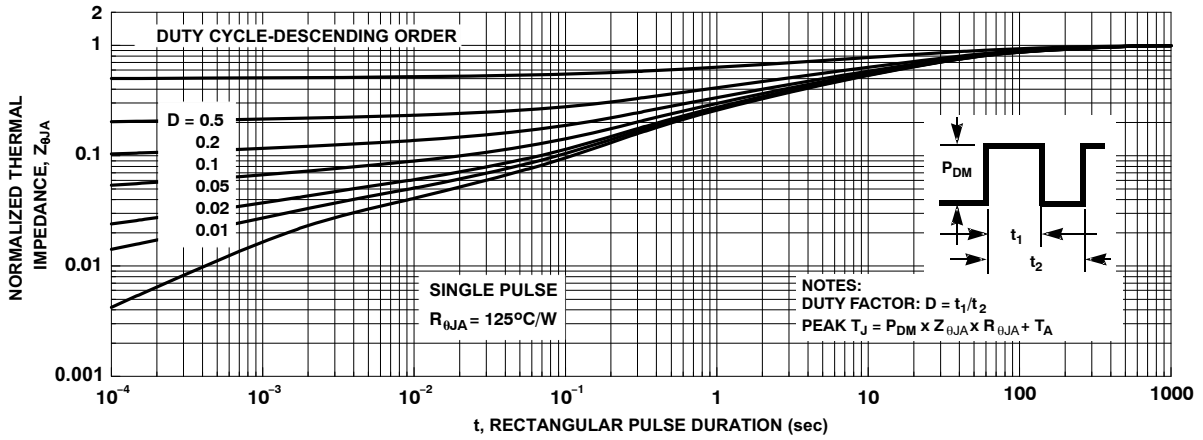
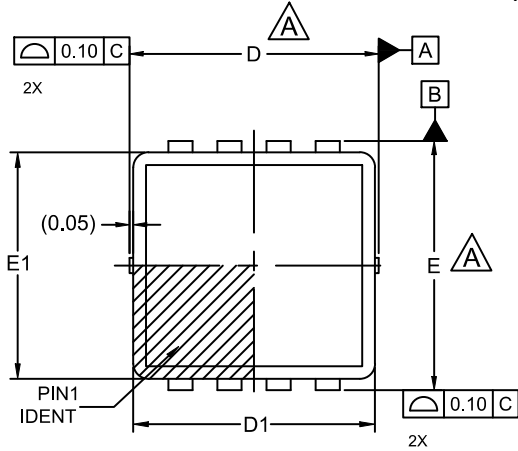


Figure 16. Junction-to-Ambient Transient Thermal Response Curve

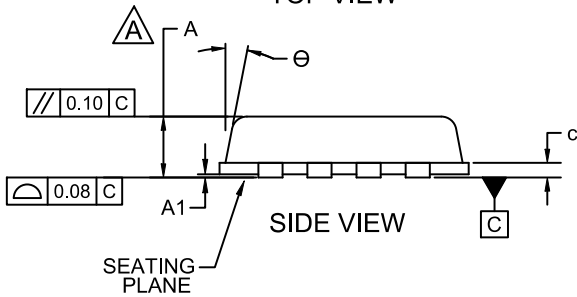
FDMC86106LZ-P

PACKAGE DIMENSIONS

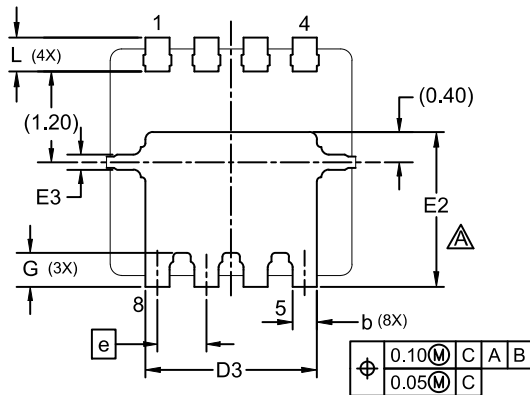
WDFN8 3.3x3.3, 0.65P
CASE 511DR
ISSUE A



TOP VIEW



SIDE VIEW

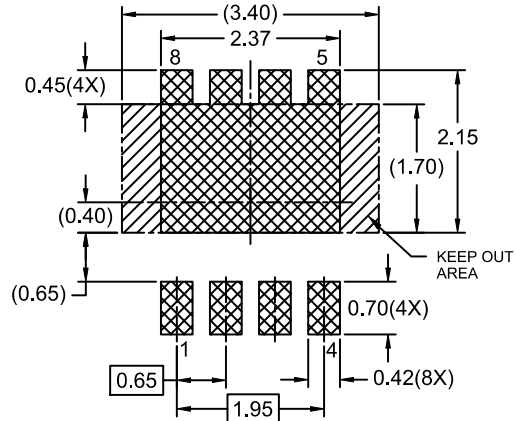


BOTTOM VIEW

NOTES:


- A. DIMENSIONS ARE IN MILLIMETERS.
- B. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- C. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY
- D. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS. MOLD FLASH PROTRUSION OR GATE BURR DOES NOT EXCEED 0.150MM.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
b	0.27	0.32	0.37
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	3.10	3.20	3.30
D3	2.17	2.27	2.37
E	3.20	3.30	3.40
E1	2.90	3.00	3.10
E2	1.95	2.05	2.15
E3	0.15	0.20	0.25
e	0.65 BSC		
G	0.40	0.45	0.50
L	0.40	0.45	0.50
Ø	0	-	12



RECOMMENDED LAND PATTERN

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