MOSFET - N-Channel Shielded Gate PowerTrench®

FDMC86106LZ-P

100 V, 103 mΩ, 7.5 A

This N−Channel logic Level MOSFETs are produced using ON Semiconductor's advanced PowerTrench process that incorporates Shielded Gate technology. This process has been optimized for the on−state resistance and yet maintain superior switching performance. G−S zener has been added to enhance ESD voltage level.

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 103 mΩ at V_{GS} = 10 V, I_D = 3.3 A
- Max $r_{DS(on)}$ = 153 mΩ at V_{GS} = 4.5 V, I_D = 2.7 A
- HBM ESD Protection Level > 1.8 KV typical (Note 4)
- 100% UIL Tested
- RoHS Compliant

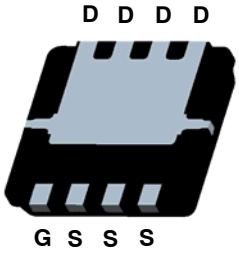
Application

- DC – DC Conversion

ON Semiconductor®

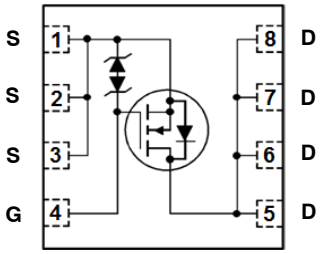
www.onsemi.com

(Top View)



(Bottom View)

WDFN8
CASE 511DR



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain−to−Source Voltage		V_{DS}	100	V
Gate−to−Source Voltage		V_{GS}	±20	V
Continuous Drain Current T_C = 25°C	(Package limited)	I_D	7.5	A
	(Silicon limited)		9.6	
Continuous Drain Current T_A = 25°C	(Figure 1)		3.3	
Pulsed Drain Current			15	
Single Pulse Avalanche Energy	(Note 3)	E_{AS}	12	mJ
Power Dissipation	T_C = 25°C	P_D	19	W
	T_A = 25°C (Figure 1)		2.3	
Operating and Storage Junction Temperature Range		T_J, T_{STG}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	6.5	°C/W
Thermal Resistance, Junction−to−Ambient (Figure 1)	$R_{\theta JA}$	53	

PACKAGE MARKING AND ORDERING INFORMATION

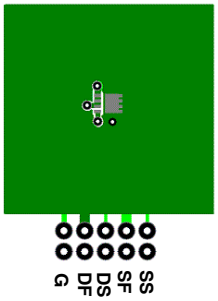
Part Number	Top Mark	Package	Reel Size	Tape Width	Quantity
FDMC86106Z	FDMC86106LZ−P	Power 33	13″	12 mm	3000 units

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−to−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	73	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate−to−Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate−to−Source Threshold Voltage	I_D = 250 μA, V_{GS} = V_{DS}	1.0	1.8	2.2	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate−to−Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	−6	–	mV/°C
$R_{DS(on)}$	Static Drain−to−Source On Resistance	V_{GS} = 10 V, I_D = 3.3 A	–	79	103	mΩ
		V_{GS} = 4.5 V, I_D = 2.7 A	–	105	153	
		V_{GS} = 10 V, I_D = 3.3 A, T_J = 125°C	–	136	178	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 3.3 A	–	11	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	–	232	310	pF
C_{oss}	Output Capacitance		–	45	60	pF
C_{rss}	Reverse Transfer Capacitance		–	2.4	5	pF
R_g	Gate Resistance		–	0.7	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 50 V, I_D = 3.3 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	4.5	10	ns
t_r	Rise Time		–	1.3	10	
$t_{d(off)}$	Turn−Off Delay Time		–	10	20	
t_f	Fall Time		–	1.4	10	
$Q_{g(tot)}$	Total Gate Charge	V_{GS} = 0 to 10 V, V_{DD} = 50 V, I_D = 3.3 A	–	4	6	nC
$Q_{g(tot)}$	Total Gate Charge	V_{GS} = 0 to 4.5 V, V_{DD} = 50 V, I_D = 3.3 A	–	2	3	
Q_{gs}	Gate−to−Source Gate Charge	V_{DD} = 50 V, I_D = 3.3 A	–	0.8	–	
Q_{gd}	Gate−to−Drain “Miller” Charge		–	0.7	–	
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source−to−Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 3.3 A (Note 2)	–	0.85	1.3	V
		V_{GS} = 0 V, I_S = 2 A (Note 2)	–	0.82	1.2	
t_{rr}	Reverse Recovery Time	I_F = 3.3 A, di/dt = 100 A/μs	–	33	54	ns
Q_{rr}	Reverse Recovery Charge		–	23	38	nC

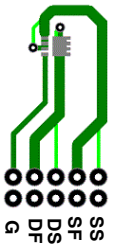
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a. 53°C/W when mounted on a 1 in^2 pad of 2 oz copper

Figure 1.



b. 125°C/W when mounted on a minimum pad of 2 oz copper

Figure 2.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting T_J = 25°C; N−ch: L = 1.0 mH, I_{AS} = 5.0 A, V_{DD} = 90 V, V_{GS} = 10 V.
4. The diode connected between gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

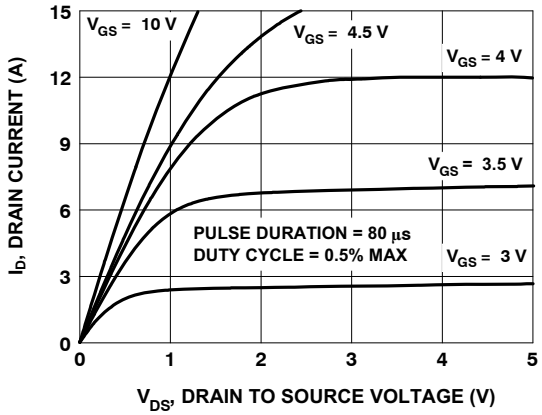


Figure 3. On Region Characteristics

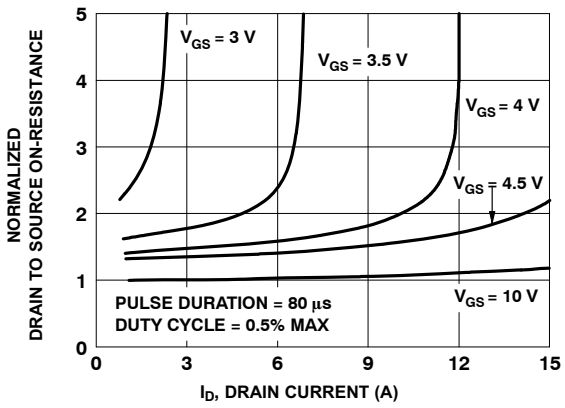


Figure 4. Normalized On−Resistance vs. Drain Current and Gate Voltage

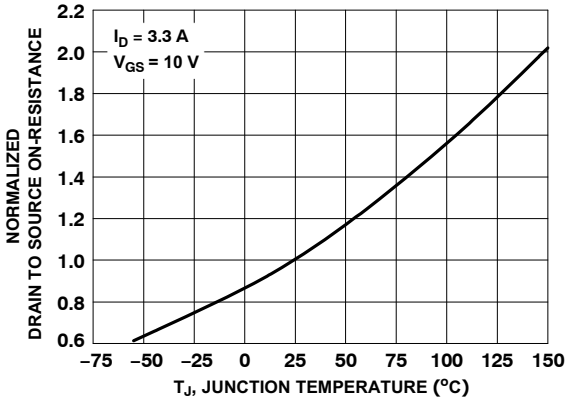


Figure 5. Normalized On Resistance vs. Junction Temperature

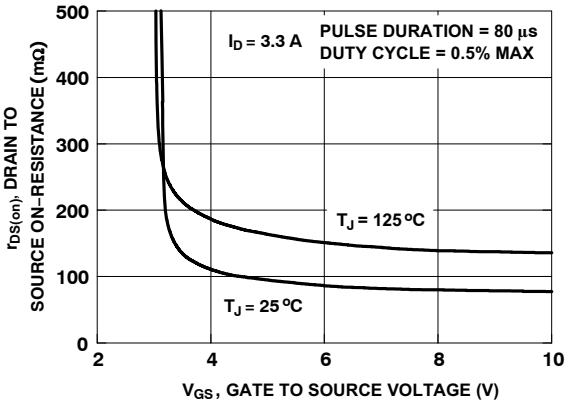


Figure 6. On−Resistance vs. Gate−to−Source Voltage

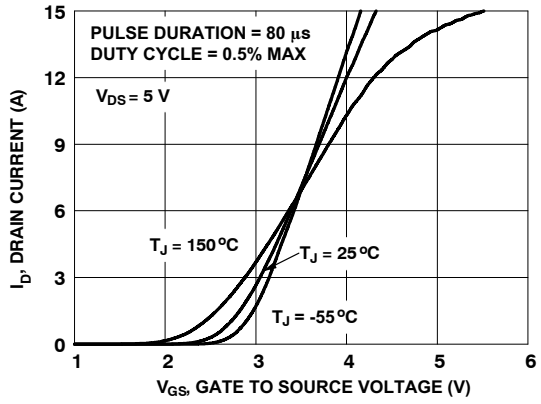


Figure 7. Transfer Characteristics

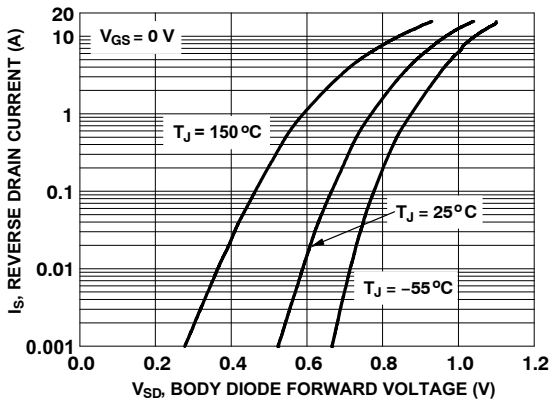


Figure 8. Source−to−Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

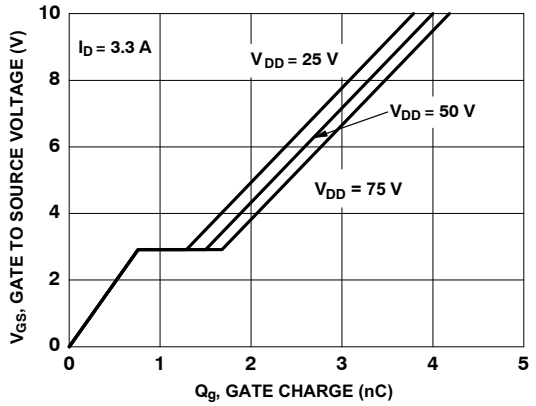


Figure 9. Gate Charge Characteristics

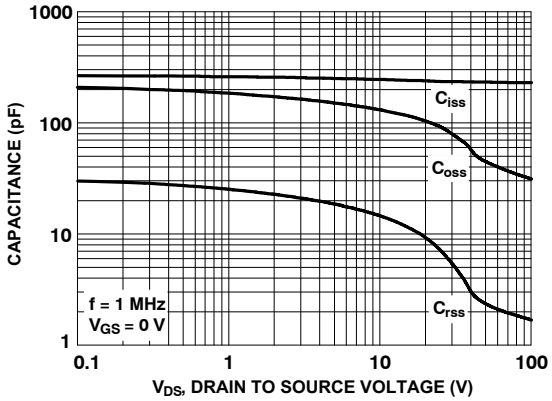


Figure 10. Capacitance vs. Drain−to−Source Voltage

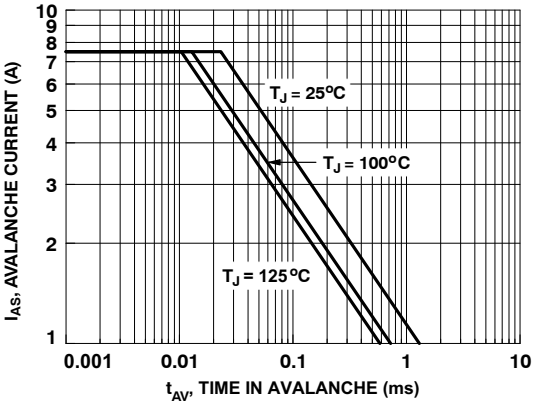


Figure 11. Unclamped Inductive Switching Capability

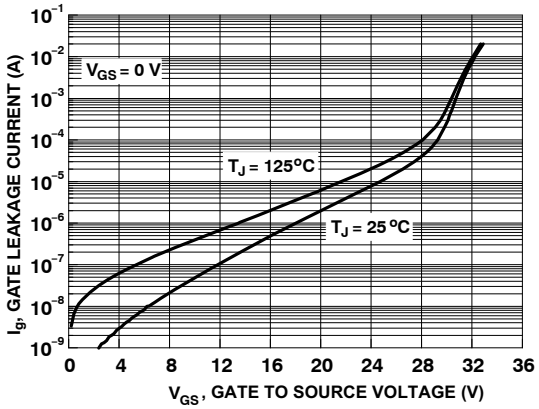


Figure 12. Gate Leakage Current vs. Gate−to−Source Voltage

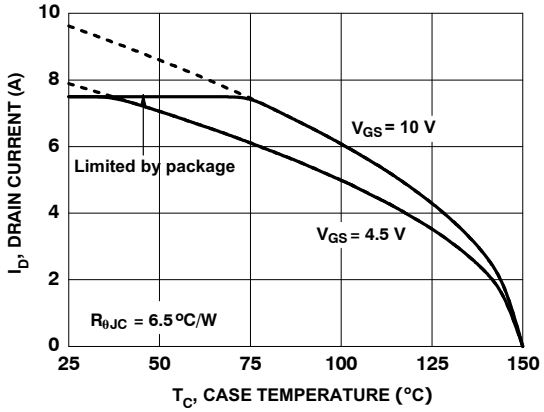


Figure 13. Maximum Continuous Drain Current vs. Case Temperature

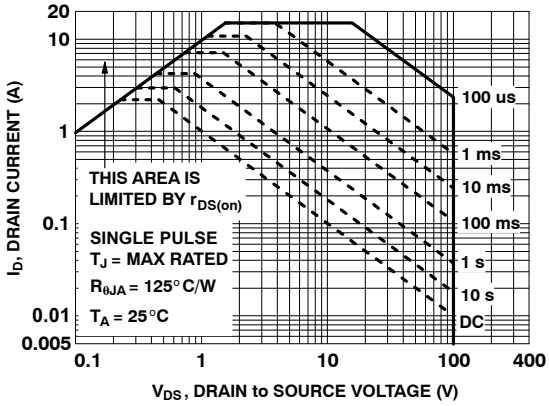


Figure 14. Forward Bias Safe Operating Area

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

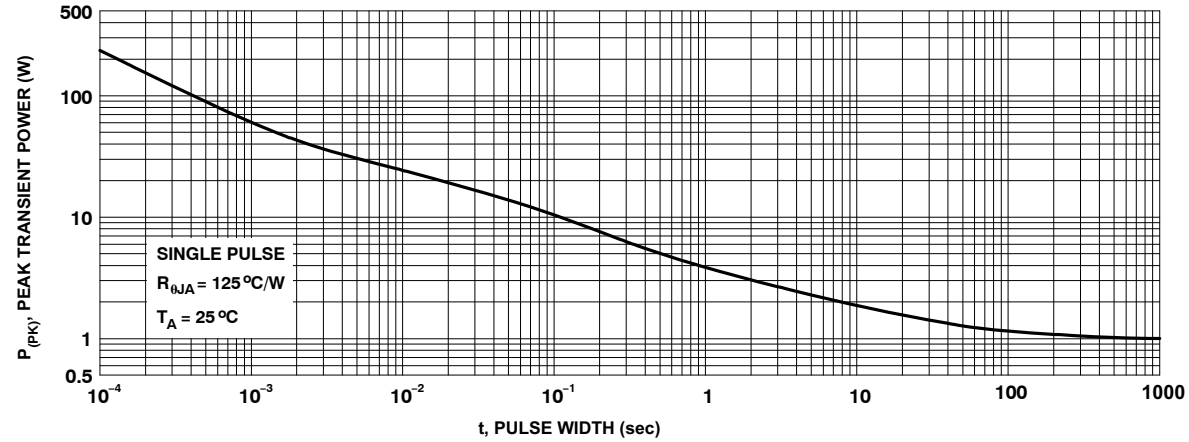


Figure 15. Single Pulse Maximum Power Dissipation

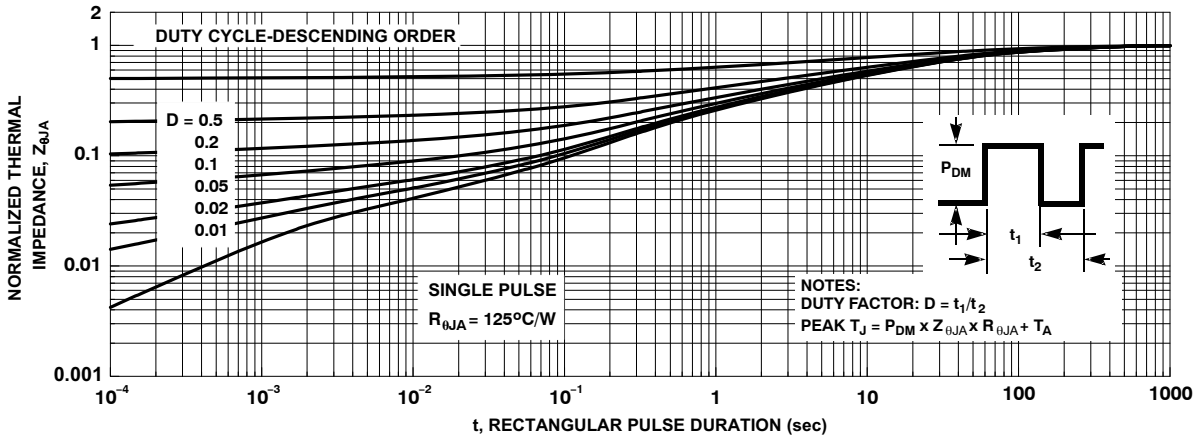
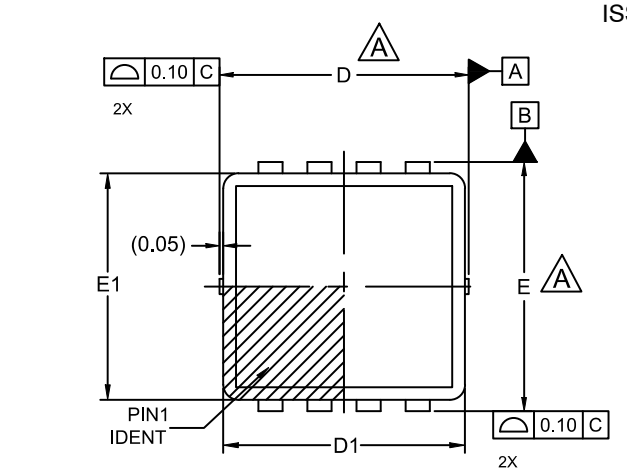


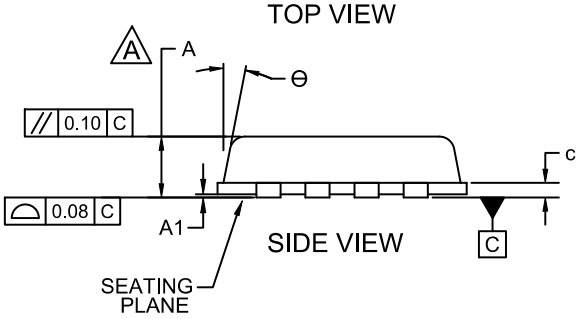
Figure 16. Junction−to−Ambient Transient Thermal Response Curve

PACKAGE DIMENSIONS

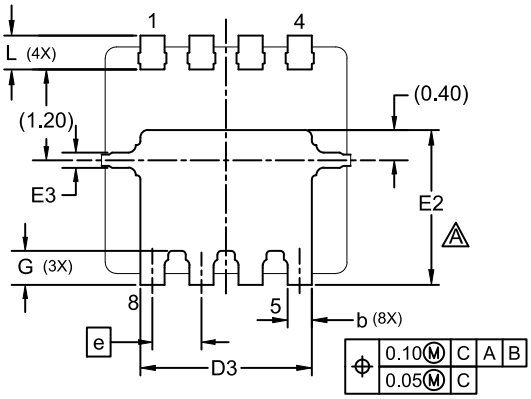
WDFN8 3.3x3.3, 0.65P
CASE 511DR
ISSUE A



TOP VIEW



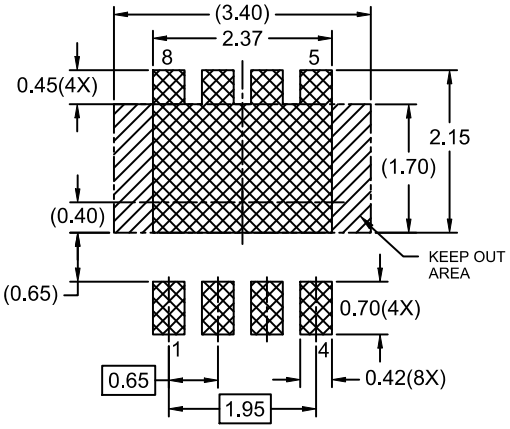
SIDE VIEW



BOTTOM VIEW

NOTES:
A. DIMENSIONS ARE IN MILLIMETERS.
B. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
C. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY
D. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS. MOLD FLASH PROTRUSION OR GATE BURR DOES NOT EXCEED 0.150MM.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
b	0.27	0.32	0.37
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	3.10	3.20	3.30
D3	2.17	2.27	2.37
E	3.20	3.30	3.40
E1	2.90	3.00	3.10
E2	1.95	2.05	2.15
E3	0.15	0.20	0.25
e	0.65 BSC		
G	0.40	0.45	0.50
L	0.40	0.45	0.50
Θ	0	-	12



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