

FDMS4D5N08LC

MOSFET, N-Channel Shielded Gate, POWERTRENCH®

80 V, 116 A, 4.2 mΩ

General Description

This N-Channel MV MOSFET is produced using ON Semiconductor's advanced POWERTRENCH® process that incorporates Shielded Gate technology. This process has been optimized to minimise on-state resistance and yet maintain superior switching performance with best in class soft body diode.

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 4.2 mΩ at $V_{GS} = 10$ V, $I_D = 37$ A
- Max $r_{DS(on)}$ = 6.1 mΩ at $V_{GS} = 4.5$ V, $I_D = 29$ A
- 50% Lower Q_{rr} than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant

Typical Applications

- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive
- Solar

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	80	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current - Continuous $T_C = 25^\circ\text{C}$ (Note 5)	116	A
	- Continuous $T_C = 100^\circ\text{C}$ (Note 5)	73	
	- Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	17	
	- Pulsed (Note 4)	633	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	384	mJ
P_D	Power dissipation $T_C = 25^\circ\text{C}$	113.6	W
	Power dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.5	
T_J , T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

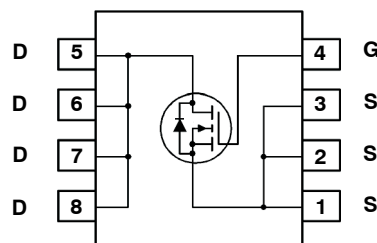
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



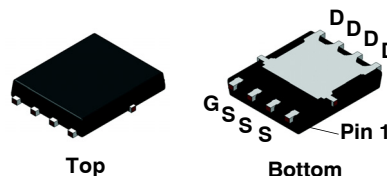
ON Semiconductor®

www.onsemi.com

ELECTRICAL CONNECTION

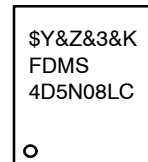


N-Channel MOSFET



Power 56
(PGFN8 5x6)
CASE 483AE

MARKING DIAGRAM



\$Y = ON Semiconductor Logo
&Z = Assembly Plant Code
&3 = Numeric Date Code
&K = Lot Code
FDMS4D5N08LC = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDMS4D5N08LC

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Shipping [†]
FDMS4D5N08LC	FDMS4D5N08LC	PQFN8 5×6 (Pb-Free/Halogen Free)	3000 Units/ Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
--------	-----------	----------------	-----	-----	-----	------

OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C		66		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 64 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
I_{GSS}	Gate-to-Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 210 \mu\text{A}$	1.0	1.4	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 210 \mu\text{A}$, referenced to 25°C		-5.1		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 37 \text{ A}$		3.2	4.2	m Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 29 \text{ A}$		4.5	6.1	
		$V_{GS} = 10 \text{ V}, I_D = 37 \text{ A}, T_J = 125^\circ\text{C}$		5.7	7.5	
g_{FS}	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_D = 37 \text{ A}$		135		S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		3640	5100	pF
C_{oss}	Output Capacitance			834	1170	
C_{rSS}	Reverse Transfer Capacitance			39	65	
R_g	Gate Resistance		0.1	0.6	1.1	

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn – On Delay Time	$V_{DD} = 40 \text{ V}, I_D = 37 \text{ A}, V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$		13	23	ns
t_r	Rise Time			19	34	
$t_{D(off)}$	Turn – Off Delay Time			59	94	
t_f	Fall Time			17	30	
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ V to } 10 \text{ V}$	$V_{DD} = 40 \text{ V}, I_D = 37 \text{ A}$	51	71	nC
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ V to } 4.5 \text{ V}$		24	34	
Q_{gs}	Gate to Source Charge			8		
Q_{gd}	Gate to Drain “Miller” Charge			6		
Q_{oss}	Output Charge	$V_{DD} = 40 \text{ V}, V_{GS} = 0 \text{ V}$		51		nC
Q_{sync}	Total Gate Charge Sync.	$V_{DS} = 0 \text{ V}, I_D = 37 \text{ A}$		46		

FDMS4D5N08LC

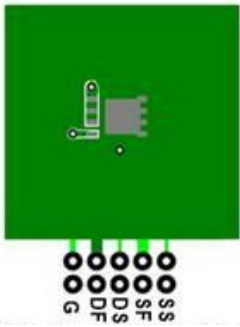
ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.1\text{ A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 37\text{ A}$ (Note 2)		0.8	1.3	
t_{rr}	Reverse Recovery Time	$I_F = 18\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		22	36	ns
Q_{rr}	Reverse Recovery Charge			38	61	
t_{rr}	Reverse Recovery Time	$I_F = 18\text{ A}, di/dt = 1000\text{ A}/\mu\text{s}$		17	27	ns
Q_{rr}	Reverse Recovery Charge			82	132	

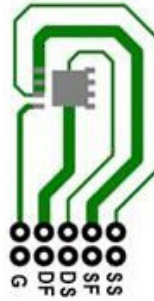
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



a) $50^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.



b) $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.
- E_{AS} of 384 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: $L = 3\text{ mH}, I_{AS} = 16\text{ A}, V_{DD} = 72\text{ V}, V_{GS} = 10\text{ V}$. 100% tested at $L = 0.1\text{ mH}, I_{AS} = 41\text{ A}, V_{GS} = 10\text{ V}$.
- Pulsed I_D please refer to Figure 11 SOA graph for more details.
- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted

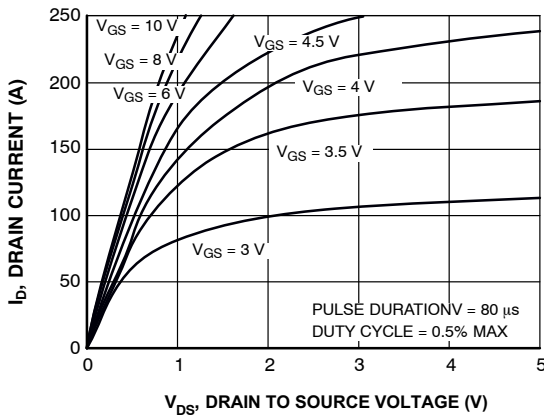


Figure 1. On Region Characteristics

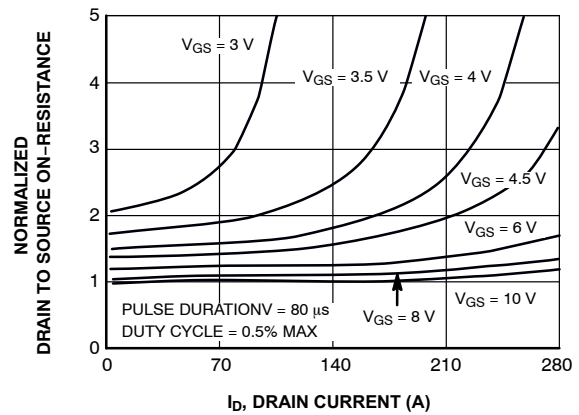


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

FDMS4D5N08LC

TYPICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted (continued)

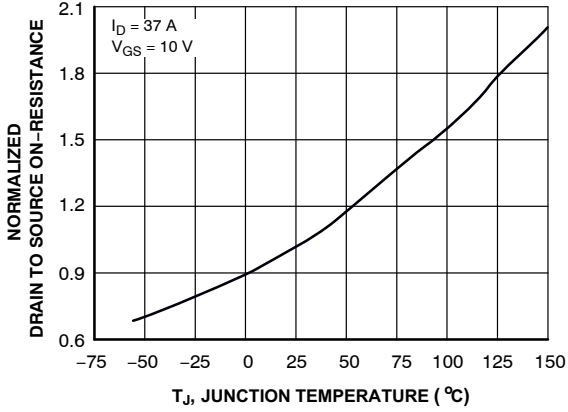


Figure 3. Normalized On Resistance vs. Junction Temperature

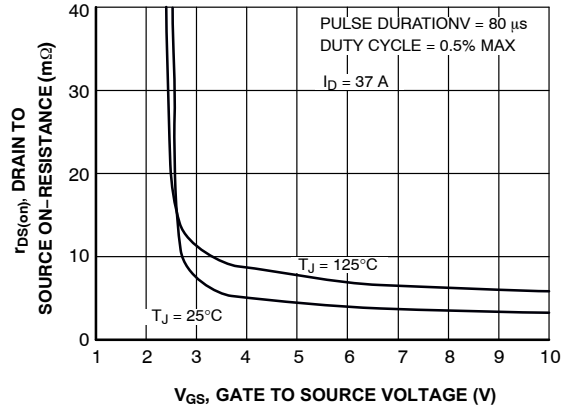


Figure 4. On-Resistance vs. Gate to Source Voltage

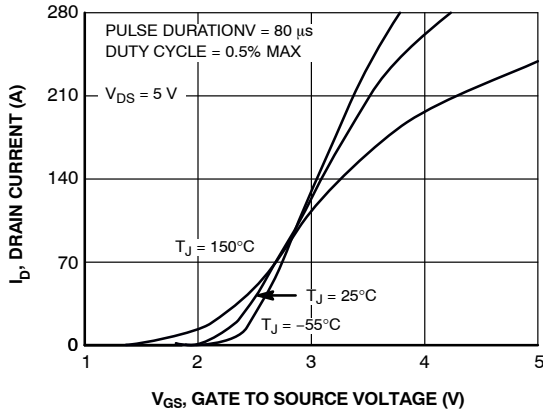


Figure 5. Transfer Characteristics

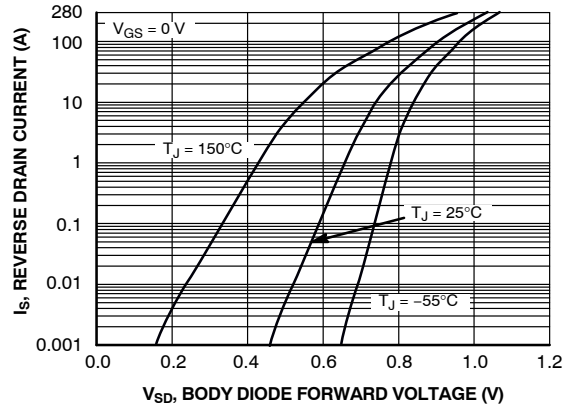


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

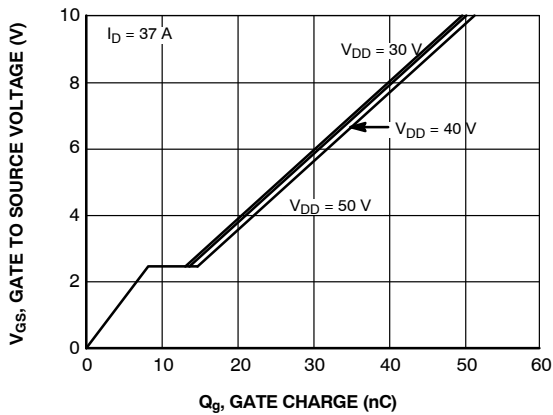


Figure 7. Gate Charge Characteristics

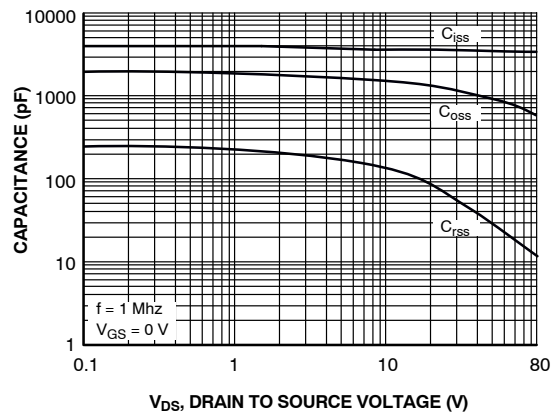


Figure 8. Capacitance vs. Drain to Source Voltage

FDMS4D5N08LC

TYPICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted (continued)

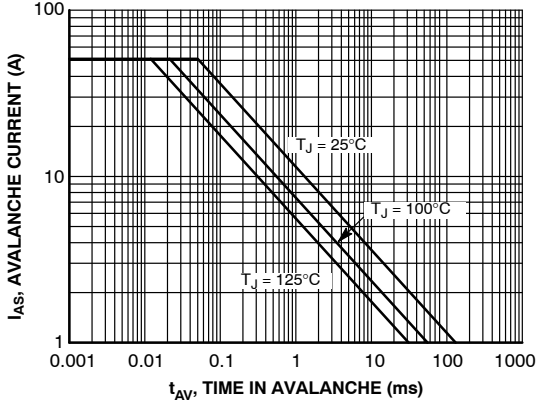


Figure 9. Unclamped Inductive Switching Capability

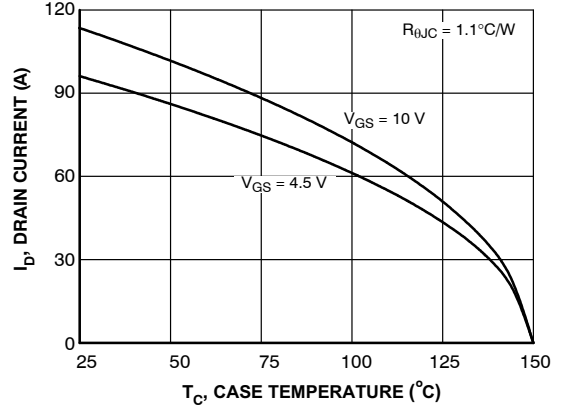


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

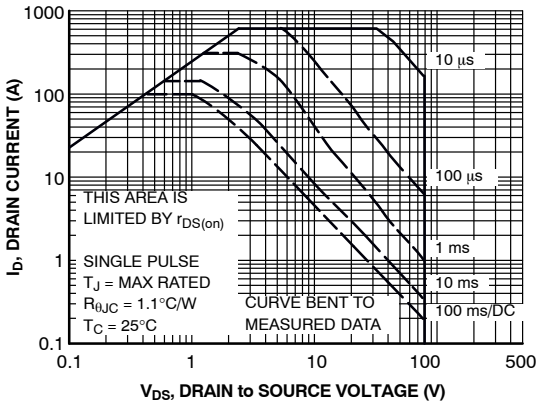


Figure 11. Unclamped Inductive Switching Capability

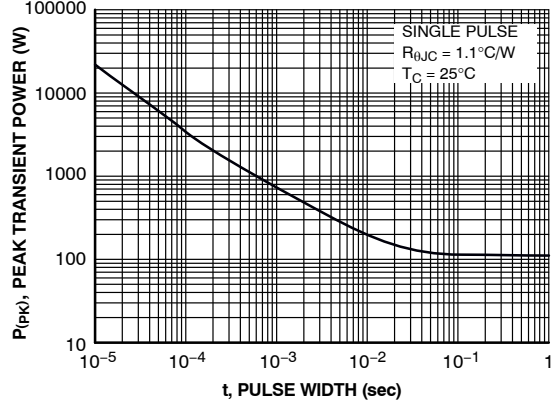


Figure 12. Maximum Continuous Drain Current vs. Case Temperature

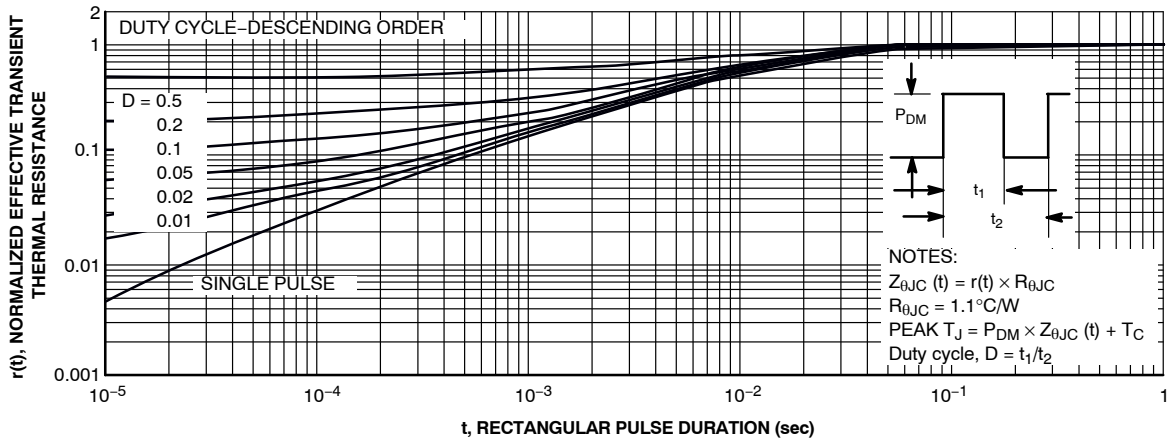
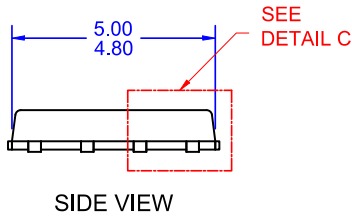
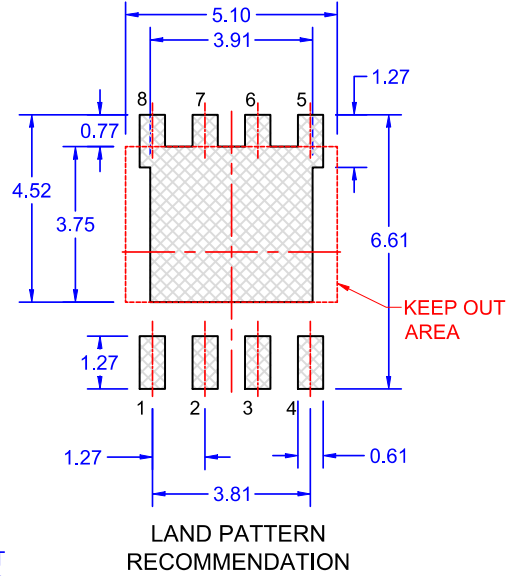
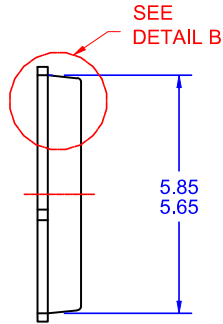
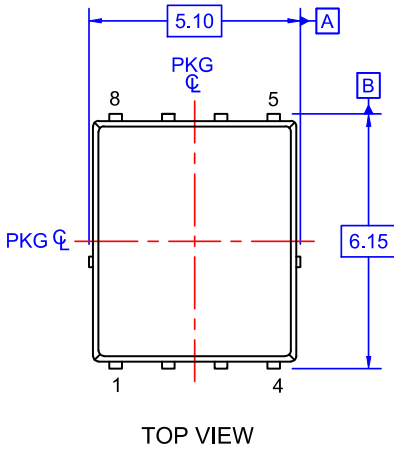


Figure 13. Junction-to-Case Transient Thermal Response Curve

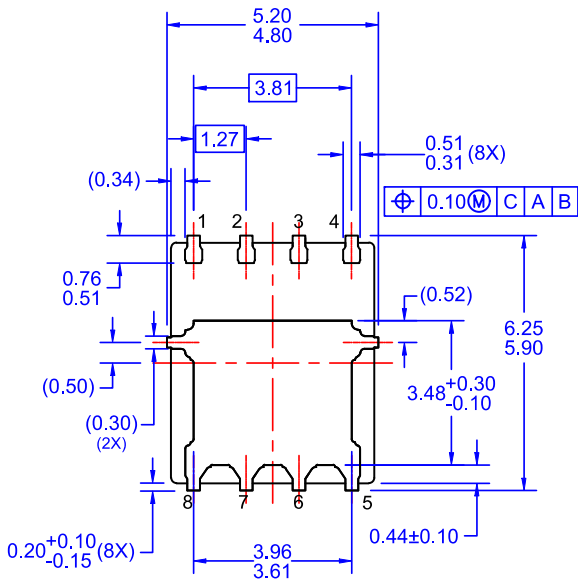
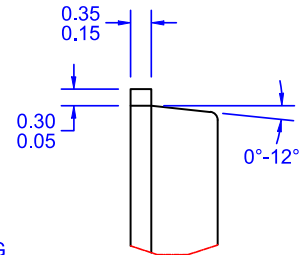
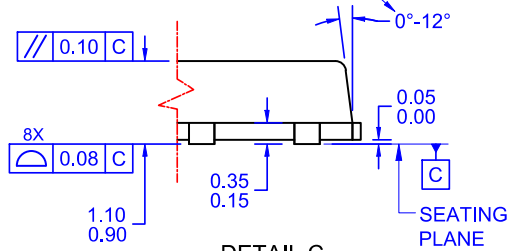
FDMS4D5N08LC

PACKAGE DIMENSIONS

PQFN8 5X6, 1.27P
CASE 483AE
ISSUE A




OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



- NOTES: UNLESS OTHERWISE SPECIFIED
- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA..
 - B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
 - C. ALL DIMENSIONS ARE IN MILLIMETERS.
 - D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
 - E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

POWERTRENCH is registered trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative