FDMS86569

MOSFET – N-Channel, POWERTRENCH®

60 V, 65 A, 5.6 mΩ

Features

- Typical $R_{DS(on)}$ = 4.3 mΩ at V_{GS} = 10 V, I_D = 65 A
- Typical $Q_{g(tot)}$ = 36 nC at V_{GS} = 10 V, I_D = 65 A
- UIS Capability
- This Device is Pb−Free and is RoHS Compliant

Applications

- Primary Switch for 12 V Systems

MOSFET MAXIMUM RATINGS (T_J = 25°C Unless Otherwise Noted)

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain−to−Source Voltage	60	V
V_{GS}	Gate−to−Source Voltage	±20	V
I_D	Drain Current - Continuous (V_{GS} = 10) (Note 1) T_C = 25°C	65	A
	Pulsed Drain Current T_C = 25°C	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	41	mJ
P_D	Power Dissipation	100	W
	Derate Above 25°C	0.67	W/°C
T_J, T_{STG}	Operating and Storage Temperature	−55 to +175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.5	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	50	°C/W

1. Current is limited by bondwire configuration.
2. Starting T_J = 25°C, L = 30 μH, I_{AS} = 52 A, V_{DD} = 60 V during inductor charging and V_{DD} = 0 V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2oz copper.

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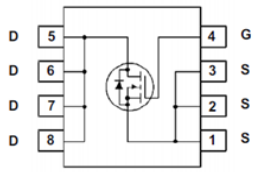
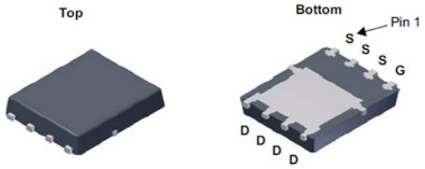
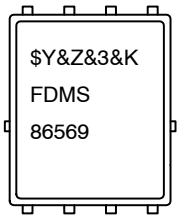




PQFN8 5x6, 1.27P
CASE 483BJ
Power 56

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDMS86569	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86569	FDMS86569	Power 56	13”	12 mm	3000 Units

ELECTRICAL CHARACTERISTICS T_J = 25°C Unless Otherwise Noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
B_{VDSS}	Drain−to−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V		60	–	–	V
I_{DSS}	Drain−to−Source Leakage Current	V_{DS} = 60 V, V_{GS} = 0 V	T_J = 25°C	–	–	1	μA
			T_J = 175°C (Note 4)	–	–	1	mA
I_{GSS}	Gate−to−Source Leakage Current	V_{GS} = ±20 V		–	–	±100	nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		2.0	2.8	4.0	V
$R_{DS(on)}$	Drain to Source On Resistance	I_D = 65 A, V_{GS}= 10 V	T_J = 25°C	–	4.3	5.6	mΩ
			T_J = 175°C (Note 4)	–	8.3	10.8	mΩ
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 30 V, V_{GS} = 0 V, f = 1 MHz		–	2560	–	pF
C_{oss}	Output Capacitance			–	740	–	pF
C_{rss}	Reverse Transfer Capacitance			–	40	–	pF
R_g	Gate Resistance	V_{GS} = 0.5 V, f = 1 MHz		–	2.0	–	Ω
$Q_{g(ToT)}$	Total Gate Charge	V_{GS} = 0 to 10 V	V_{DD} = 30 V, I_D = 65 A	–	36	54	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 to 2 V		–	4.8	–	nC
Q_{gs}	Gate−to−Source Gate Charge			–	14	–	nC
Q_{gd}	Gate−to−Drain “Miller” Charge			–	7	–	nC
SWITCHING CHARACTERISTICS							
t_{on}	Turn−On Time	V_{DD} = 30 V, I_D = 65 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		–	–	36	ns
$t_{d(on)}$	Turn−On Delay			–	16	–	ns
t_r	Rise Time			–	11	–	ns
$t_{d(off)}$	Turn−Off Delay			–	23	–	ns
t_f	Fall Time			–	8	–	ns
t_{off}	Turn−Off Time			–	–	41	ns
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source−to−Drain Diode Voltage	I_{SD} = 65 A, V_{GS} = 0 V		–	–	1.25	V
		I_{SD} = 32.5 A, V_{GS} = 0 V		–	–	1.2	V
t_{rr}	Reverse−Recovery Time	V_{DD} = 48 V, I_F = 65 A, dI_{SD}/dt = 100 A/μs		–	55	72	ns
Q_{rr}	Reverse−Recovery Charge			–	45	59	nC

4. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

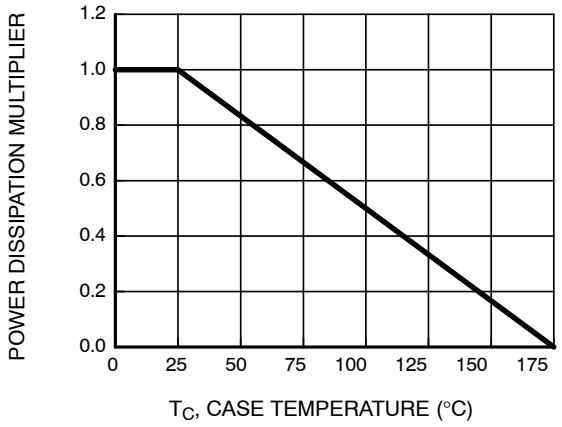


Figure 1. Normalized Power Dissipation vs. Case Temperature

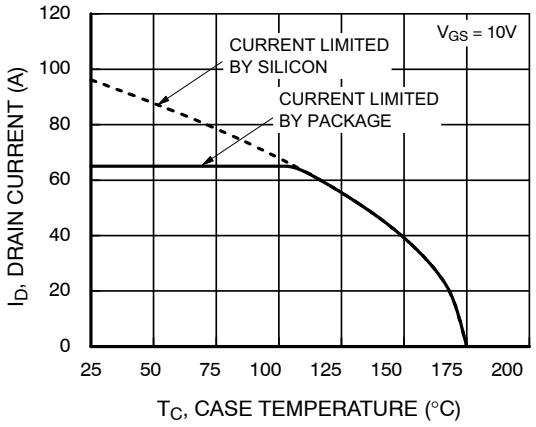


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

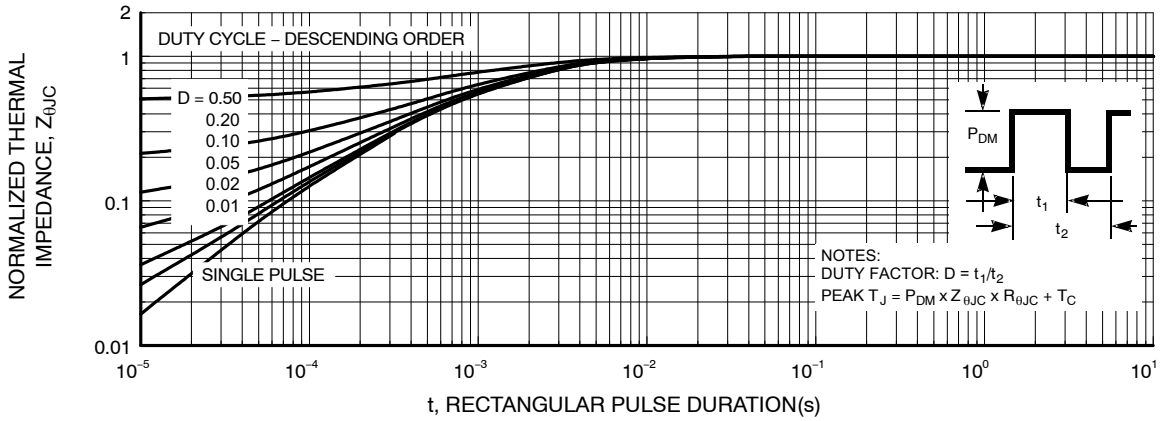


Figure 3. Normalized Maximum Transient Thermal Impedance

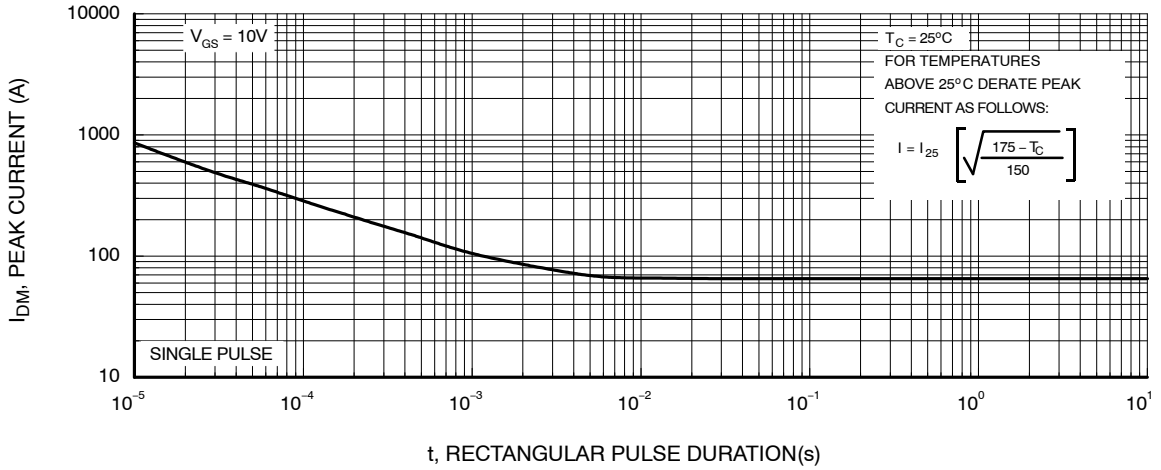


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

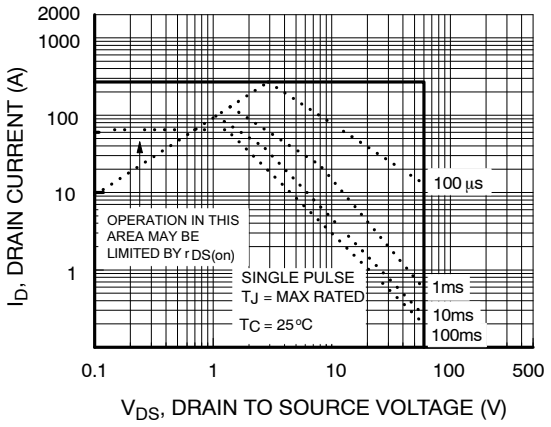
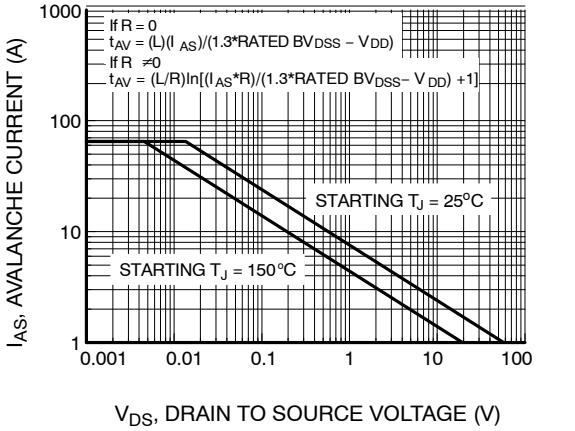


Figure 5. Forward Bias Safe Operating Area



NOTE:
Refer to ON Semiconductor Application Notes AN7514 and AN7515.

Figure 6. Unclamped Inductive Switching Capability

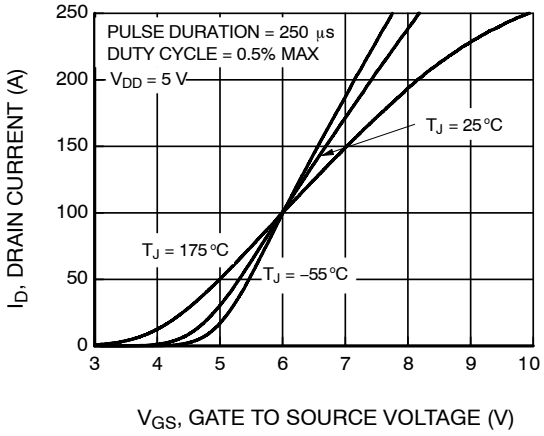


Figure 7. Transfer Characteristics

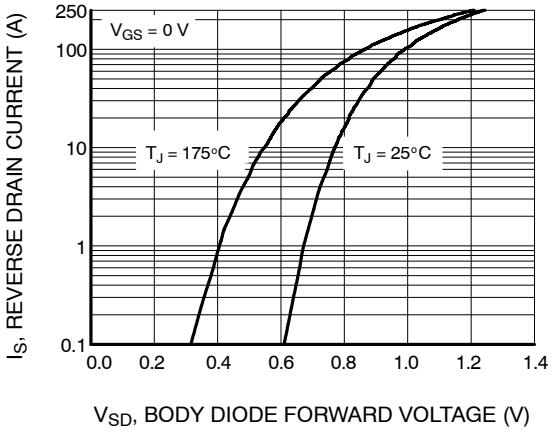


Figure 8. Forward Diode Characteristics

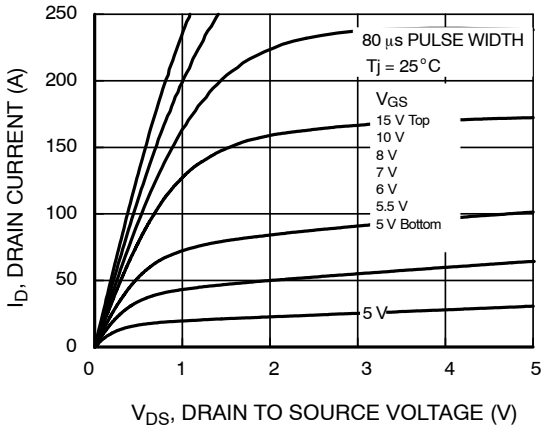


Figure 9. Saturation Characteristics

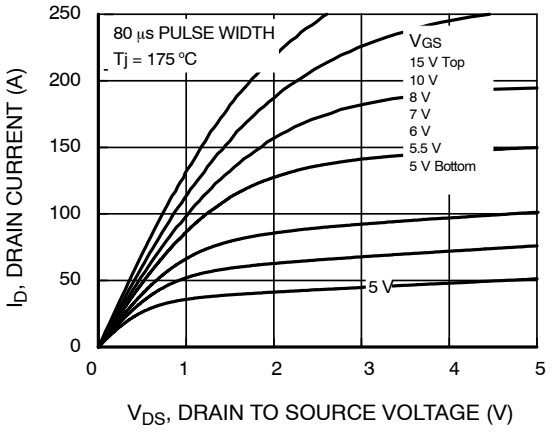


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (continued)

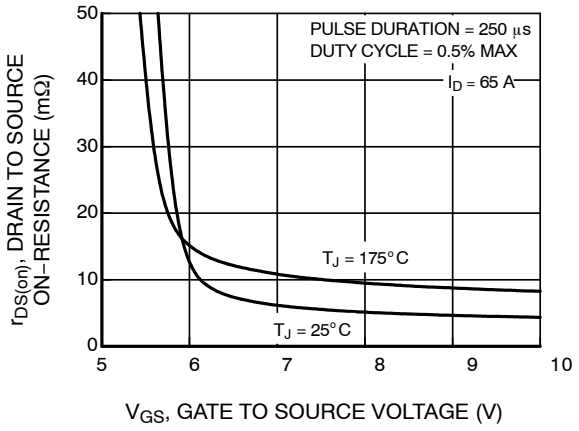


Figure 11. R_{DSON} vs. Gate Voltage

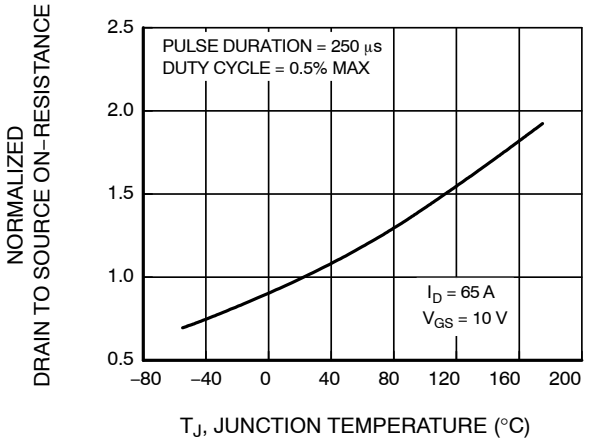


Figure 12. Normalized R_{DSON} vs. Junction Temperature

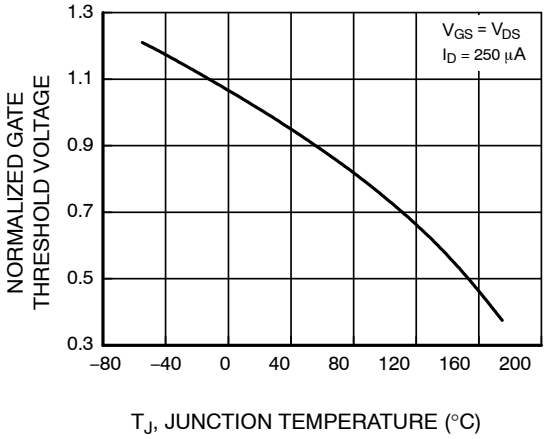


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

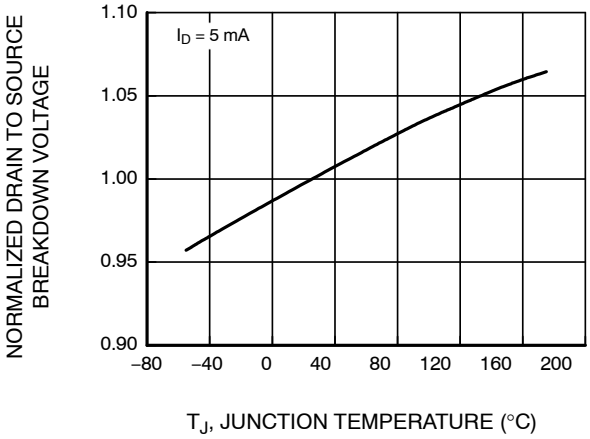


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

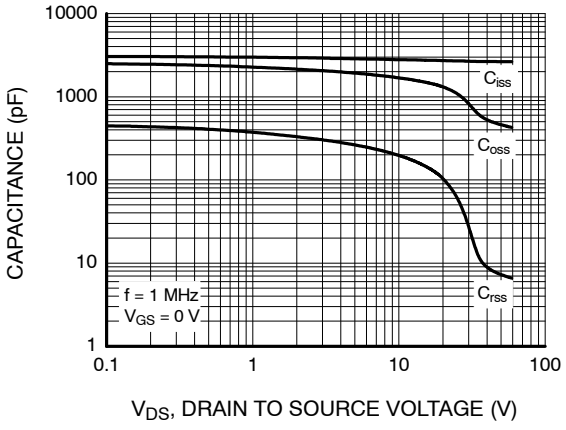


Figure 15. Capacitance vs. Drain to Source Voltage

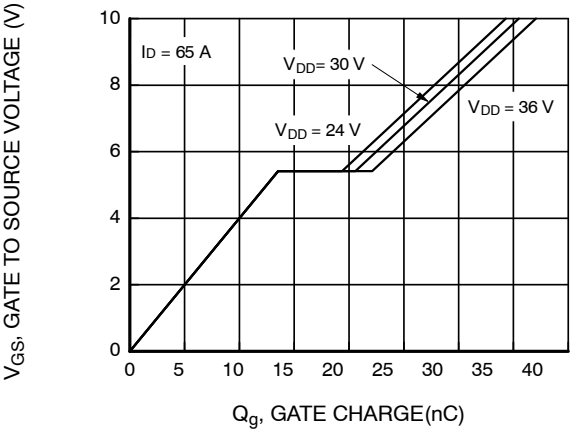
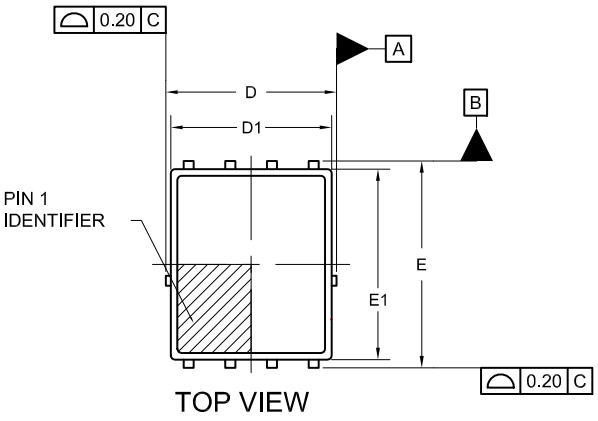


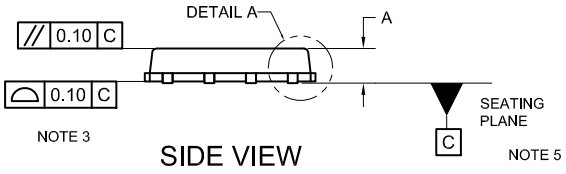
Figure 16. Gate Charge vs. Gate to Source Voltage

PACKAGE DIMENSIONS

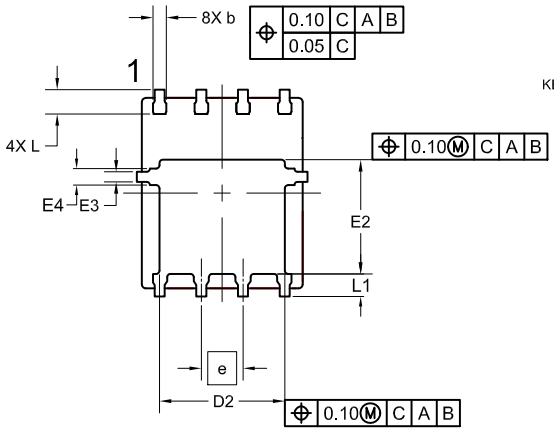
PQFN8 5X6, 1.27P
CASE 483BJ
ISSUE C



TOP VIEW



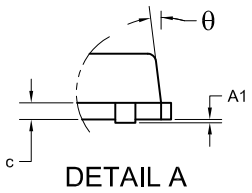
SIDE VIEW



BOTTOM VIEW

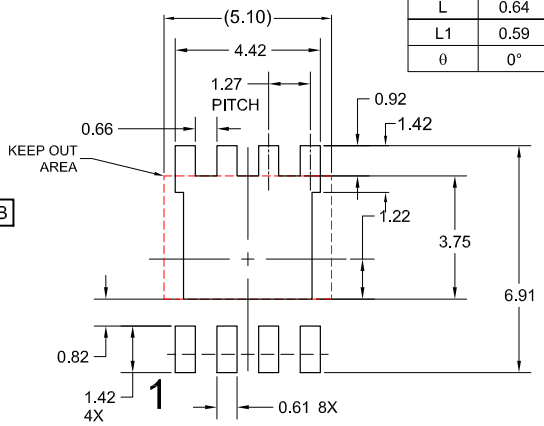
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



DETAIL A

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.025	0.05
b	0.31	0.41	0.51
c	0.23	0.28	0.33
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.72	3.82	3.92
E	6.20	6.30	6.40
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	0.30		
E4	0.50		
e	1.27 BSC		
L	0.64	0.74	0.84
L1	0.59	0.69	0.79
θ	0°	—	12°



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