

FDMS86581-F085

MOSFET – POWERTRENCH[®], N-Channel

60 V, 30 A, 15 mΩ

Features

- Typical $R_{DS(on)}$ = 12.5 mΩ at $V_{GS} = 10$ V, $I_D = 30$ A
- Typical $Q_{G(tot)}$ = 13 nC at $V_{GS} = 10$ V, $I_D = 25$ A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Electronic Steering
- Integrated Started/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12 V Systems

MOSFET MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Drain Current – Continuous ($V_{GS} = 10$) $T_C = 25^\circ\text{C}$ (Note 1)	30	A
	Pulsed Drain Current, $T_C = 25^\circ\text{C}$	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	13.5	mJ
P_D	Power Dissipation	50	W
	Derate Above 25°C	0.33	
T_J, T_{STG}	Operating and Storage Temperature	-55 to +175	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	50	$^\circ\text{C}/\text{W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

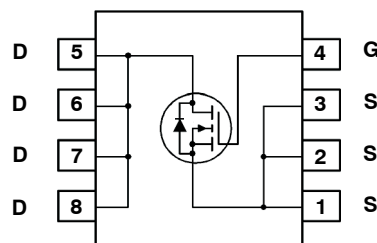
1. Current is limited by bondwire configuration.
2. Starting $T_J = 25^\circ\text{C}$, $L = 40\mu\text{H}$, $I_{AS} = 26$ A, $V_{DD} = 60$ V during inductor charging and $V_{DD} = 0$ V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2 oz copper.



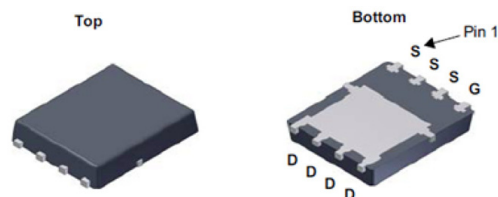
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ELECTRICAL CONNECTION

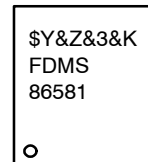


N-Channel MOSFET



Power 56
(PGFN8 5x6)
CASE 483BJ

MARKING DIAGRAM



\$Y = ON Semiconductor Logo
 &Z = Assembly Plant Code
 &3 = Numeric Date Code
 &K = Lot Code
 FDMS86581 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDMS86581–F085

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Shipping [†]
FDMS86581	FDMS86581–F085	Power 56	3000 Units/ Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max.	Units
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OFF CHARACTERISTICS

B _{VDS}	Drain-to-Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	60	–	–	V
I _{DSS}	Drain-to-Source Leakage Current	V _{DS} = 60 V, T _J = 25°C	–	–	1	A
		V _{GS} = 0 V, T _J = 175°C (Note 4)	–	–	1	mA
I _{GSS}	Gate-to-Source Leakage Current	V _{GS} = ±20 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	2.0	2.7	4.0	V
R _{DS(on)}	Drain to Source On Resistance	I _D = 30 A, T _J = 25°C	–	12.5	15.0	mΩ
		V _{GS} = 10 V, T _J = 175°C (Note 4)	–	25.1	30.1	mΩ

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 30 V, V _{GS} = 0 V, f = 1 MHz	–	881	–	pF
C _{oss}	Output Capacitance		–	281	–	pF
C _{rss}	Reverse Transfer Capacitance		–	15	–	pF
R _G	Gate Resistance	f = 1 MHz	–	3.1	–	Ω
Q _{g(ToT)}	Total Gate Charge	V _{GS} = 0 to 10 V	–	13	19	nC
Q _{g(th)}	Threshold Gate Charge	V _{GS} = 0 to 2 V V _{DD} = 30 V I _D = 25 A	–	2	–	nC
Q _{gs}	Gate-to-Source Gate Charge		–	4	–	nC
Q _{gd}	Gate-to-Drain "Miller" Charge		–	3	–	nC

SWITCHING CHARACTERISTICS

t _{on}	Turn-On Time	V _{DD} = 30 V, I _D = 30 A V _{GS} = 10 V, R _{GEN} = 6 Ω	–	–	20	ns
t _{d(on)}	Turn-On Delay		–	9	–	ns
t _r	Rise Time		–	5	–	ns
t _{d(off)}	Turn-Off Delay		–	15	–	ns
t _f	Fall Time		–	4	–	ns
t _{off}	Turn-Off Time		–	–	28	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source-to-Drain Diode Voltage	I _{SD} = 30 A, V _{GS} = 0 V	–	–	1.25	V
		I _{SD} = 15 A, V _{GS} = 0 V	–	–	1.2	V
t _{rr}	Reverse-Recovery Time	I _F = 30 A, dI _{SD} /dt = 100 A/μs, V _{DD} = 48 V	–	37	55	ns
Q _{rr}	Reverse Recovery Charge		–	22	33	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

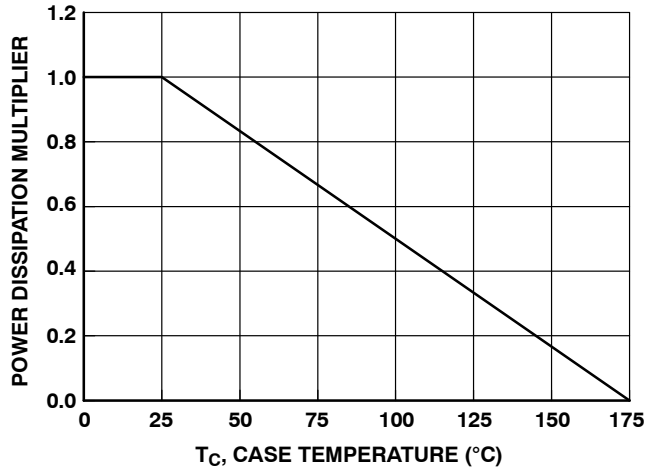


Figure 1. Normalized Power Dissipation vs. Case Temperature

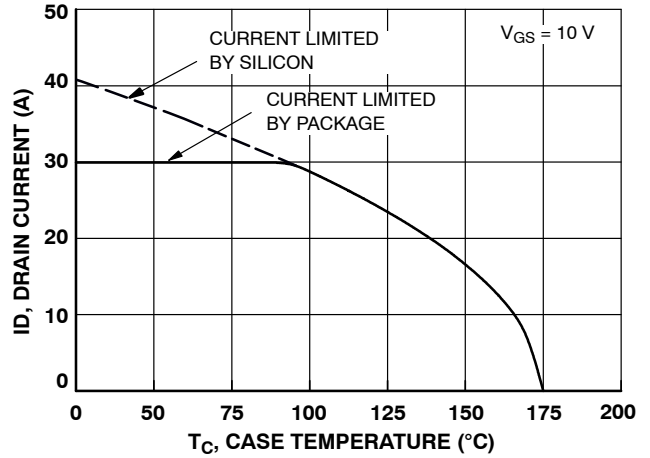


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

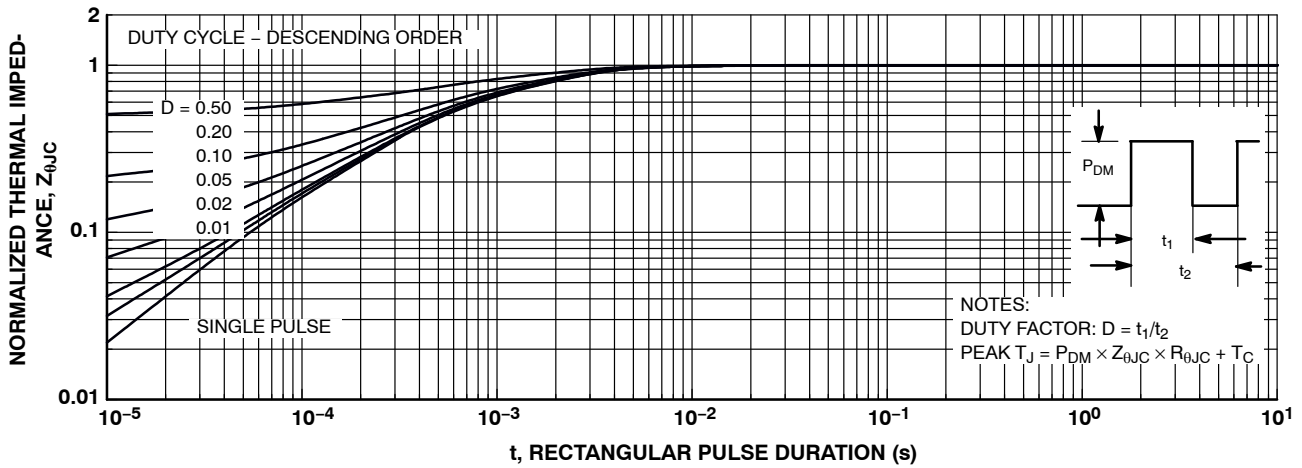


Figure 3. Normalized Maximum Transient Thermal Impedance

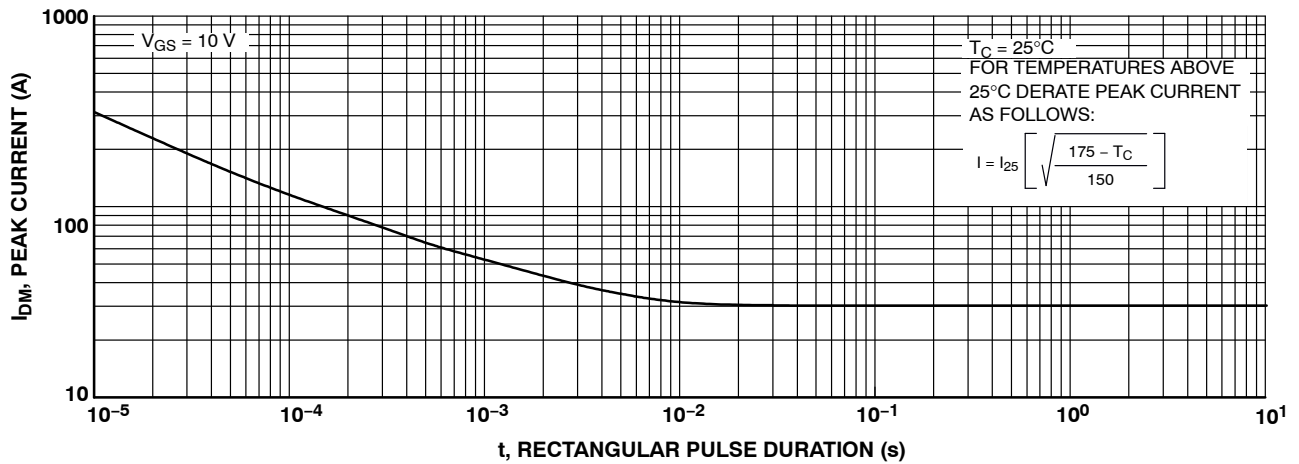


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

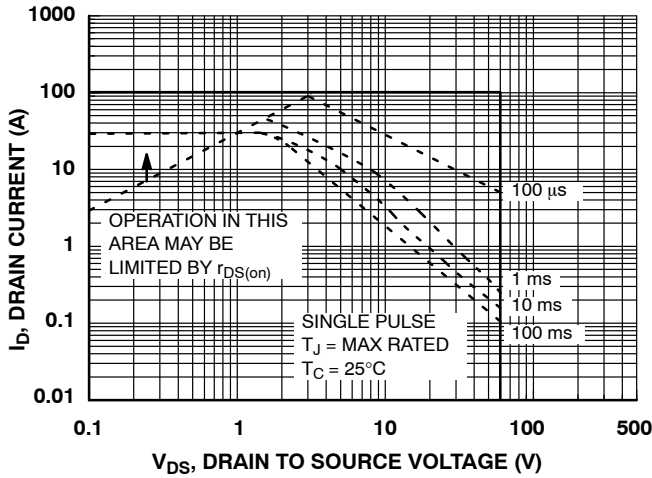
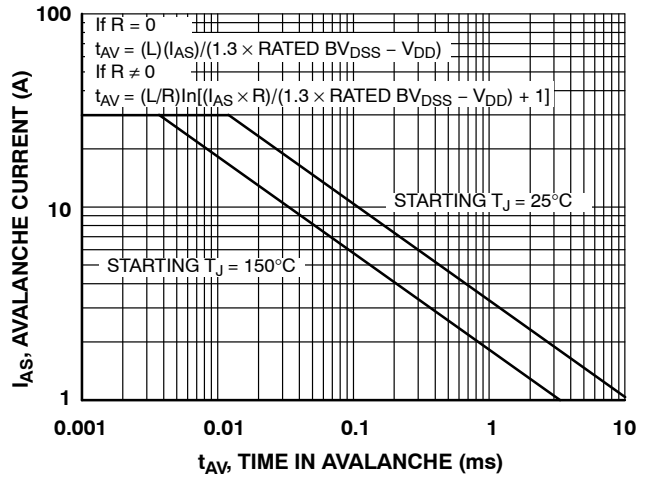


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to ON Semiconductor Application Notes [AN7514](#) and [AN7515](#).

Figure 6. Unclamped Inductive Switching Capability

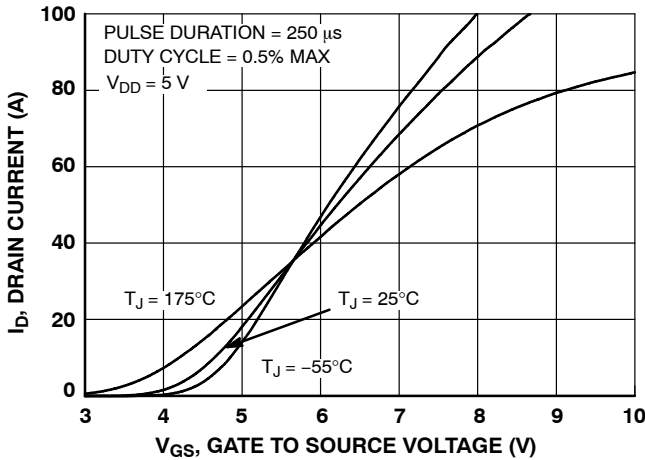


Figure 7. Transfer Characteristics

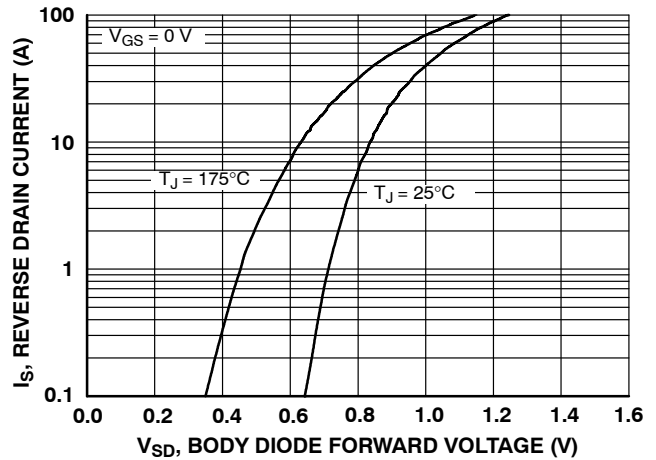


Figure 8. Forward Diode Characteristics

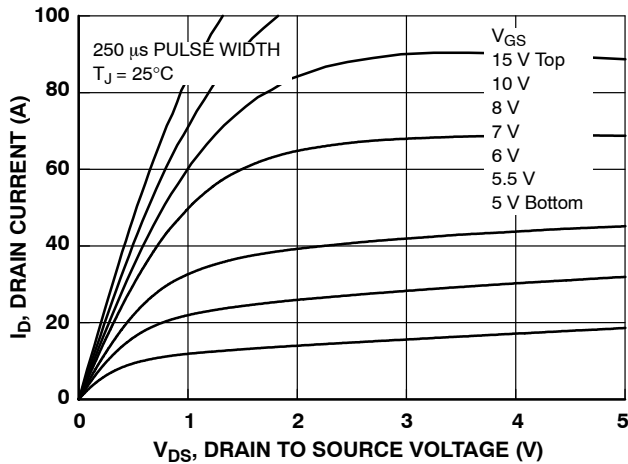


Figure 9. Saturation Characteristics

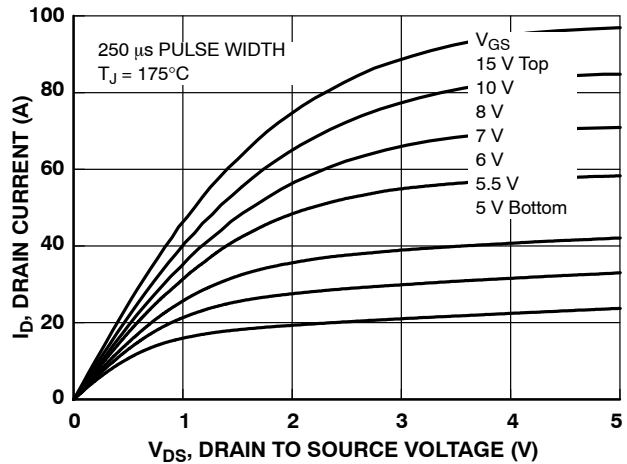


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (continued)

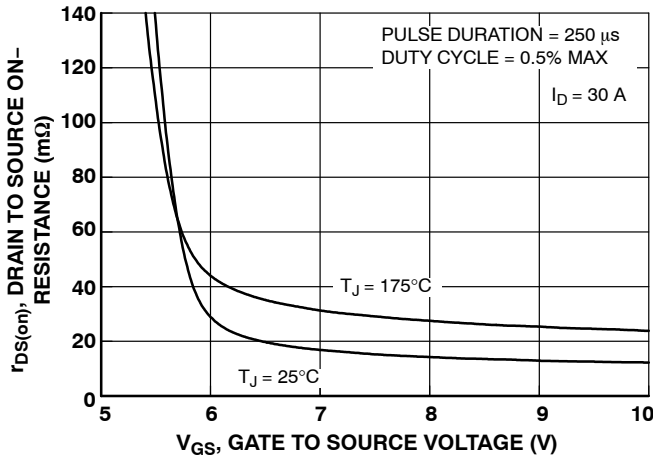


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

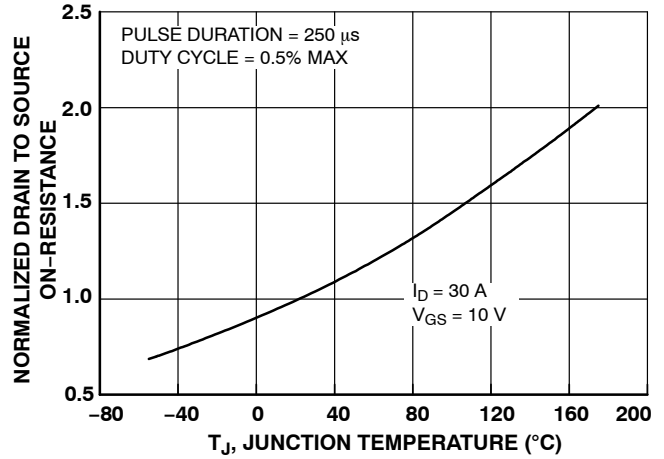


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

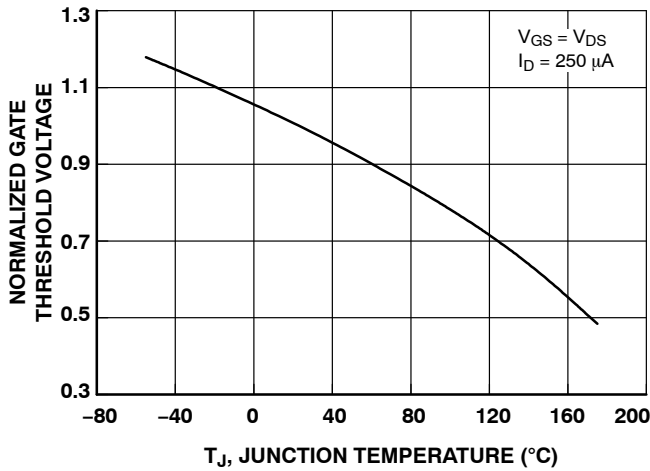


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

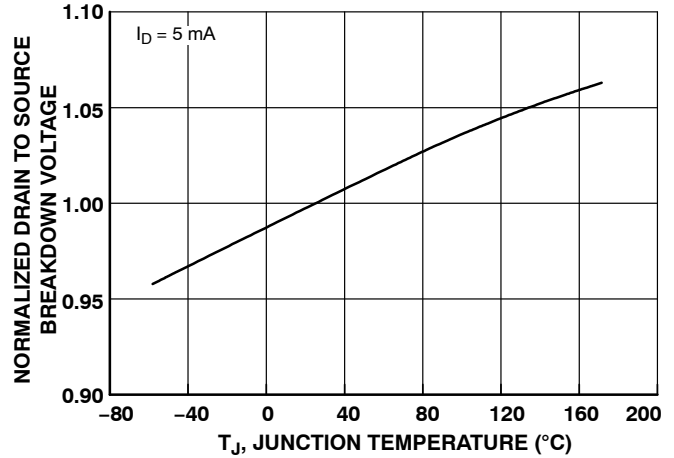


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

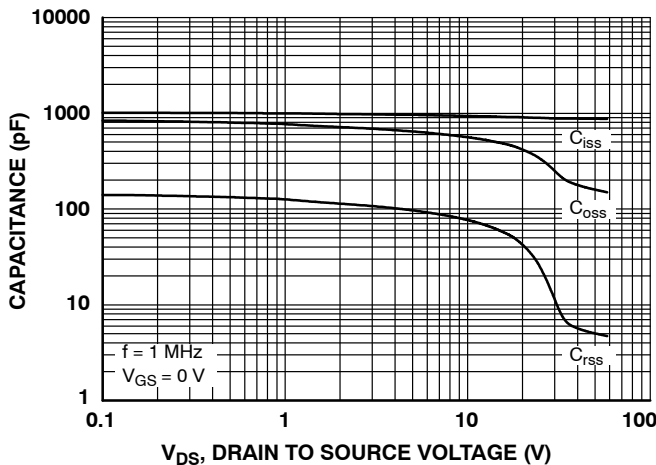


Figure 15. Capacitance vs. Drain to Source Voltage

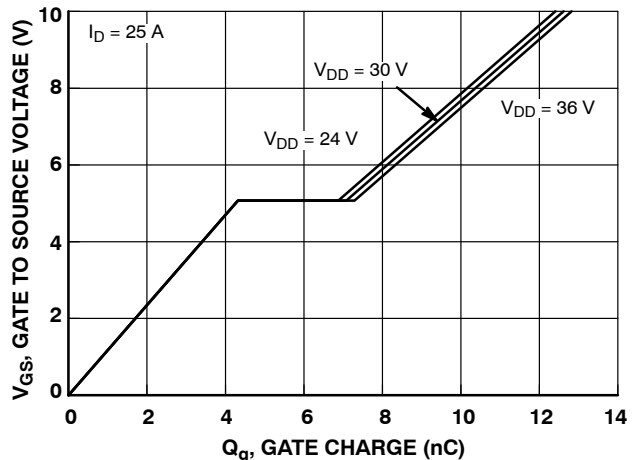


Figure 16. Gate Charge vs. Gate to Source Voltage

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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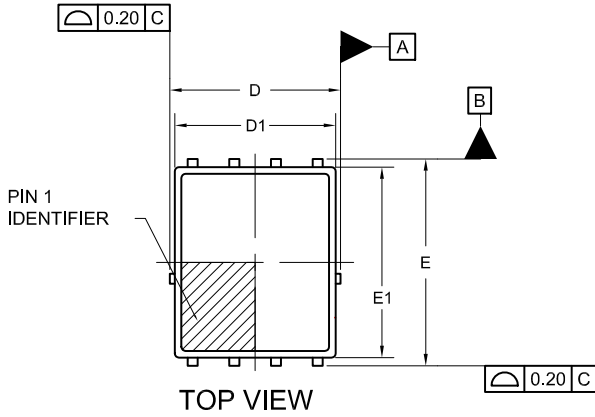


PQFN8 5X6, 1.27P

CASE 483BJ

ISSUE C

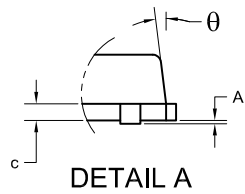
DATE 13 DEC 2017



TOP VIEW

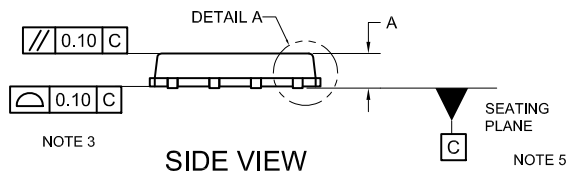
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

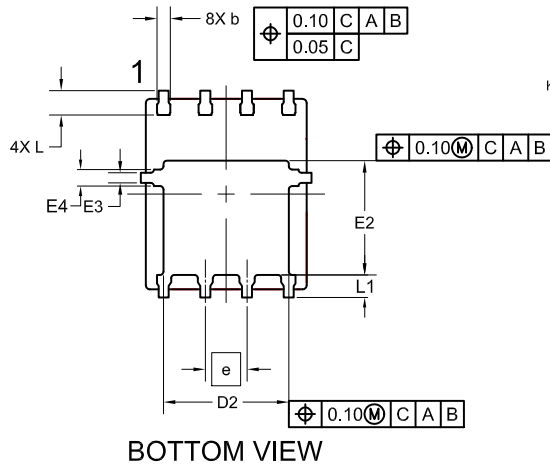


DETAIL A

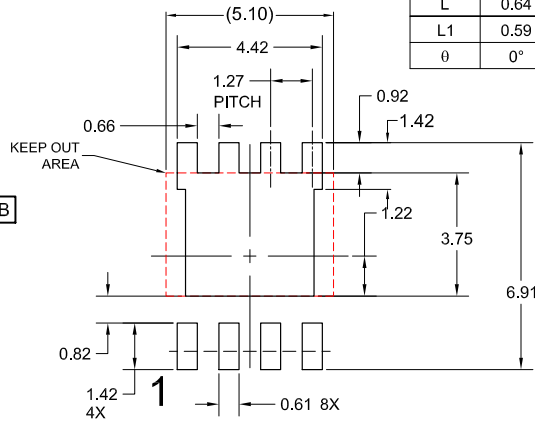
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.025	0.05
b	0.31	0.41	0.51
c	0.23	0.28	0.33
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.72	3.82	3.92
E	6.20	6.30	6.40
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	0.30		
E4	0.50		
e	1.27 BSC		
L	0.64	0.74	0.84
L1	0.59	0.69	0.79
theta	0°	—	12°



SIDE VIEW



BOTTOM VIEW




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ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION FROM FAIRCHILD PQFN08M TO ON SEMICONDUCTOR. REQ. BY I. CAMBALIZA.	30 SEP 2016
A	MODIFIED DRAWING TO ADD PIN NUMBERING AND TOP OF PACKAGE DIMENSIONS. REQ. BY J. COMPARATIVO.	02 JUN 2017
B	ROTATED CASE OUTLINE TO CORRECT PIN NUMBERING. REQ. BY H. ALLEN.	14 JUN 2017
C	REDRAWN TO ON SEMI JEDEC STANDARDS. MODIFIED DIMENSIONS FOR A, D & E. REQ. BY J. COMPARATIVO.	13 DEC 2017

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