



ON Semiconductor®

FDP038AN06A0 / FDI038AN06A0

N-Channel PowerTrench® MOSFET

60 V, 80 A, 3.8 mΩ

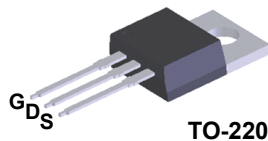
Features

- $R_{DS(on)} = 3.5 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 80 \text{ A}$
- $Q_{G(tot)} = 96 \text{ nC}$ (Typ.) @ $V_{GS} = 10 \text{ V}$
- Low Miller Charge
- Low Q_{rr} Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)

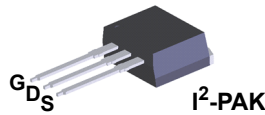
Formerly developmental type 82584

Applications

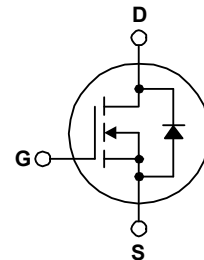
- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor drives and Uninterruptible Power Supplies



TO-220



I²-PAK



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDP038AN06A0 FDI038AN06A0	Unit
V_{DSS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current		
	Continuous ($T_C < 151^\circ\text{C}$, $V_{GS} = 10\text{V}$)	80	A
	Continuous ($T_{amb} = 25^\circ\text{C}$, $V_{GS} = 10\text{V}$, with $R_{\theta JA} = 62^\circ\text{C/W}$)	17	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	625	mJ
P_D	Power dissipation	310	W
	Derate above 25°C	2.07	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.48	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. (Note 2)	62	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP038AN06A0	FDP038AN06A0	TO-220	Tube	N/A	50 units
FDI038AN06A0	FDI038AN06A0	I ² -PAK	Tube	N/A	50 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 50\text{V}$ $V_{GS} = 0\text{V}$ $T_C = 150^\circ\text{C}$	-	-	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 80\text{A}$, $V_{GS} = 10\text{V}$	-	0.0035	0.0038	Ω
		$I_D = 40\text{A}$, $V_{GS} = 6\text{V}$	-	0.0049	0.0074	
		$I_D = 80\text{A}$, $V_{GS} = 10\text{V}$, $T_J = 175^\circ\text{C}$	-	0.0071	0.0078	

Dynamic Characteristics

C_{ISS}	Input Capacitance	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	-	6400	-	pF	
C_{OSS}	Output Capacitance		-	1123	-	pF	
C_{RSS}	Reverse Transfer Capacitance		-	367	-	pF	
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V}$ to 10V	$V_{DD} = 30\text{V}$ $I_D = 80\text{A}$ $I_g = 1.0\text{mA}$	96	124	nC	
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\text{V}$ to 2V		-	12	15	nC
Q_{gs}	Gate to Source Gate Charge			-	26	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau			-	15	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			-	27	-	nC

Switching Characteristics ($V_{GS} = 10\text{V}$)

t_{ON}	Turn-On Time	$V_{DD} = 30\text{V}$, $I_D = 80\text{A}$ $V_{GS} = 10\text{V}$, $R_{GS} = 2.4\Omega$	-	-	175	ns
$t_{d(ON)}$	Turn-On Delay Time		-	17	-	ns
t_r	Rise Time		-	144	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	34	-	ns
t_f	Fall Time		-	60	-	ns
t_{OFF}	Turn-Off Time		-	-	115	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 80\text{A}$	-	-	1.25	V
		$I_{SD} = 40\text{A}$	-	-	1.0	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 75\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	38	ns
Q_{RR}	Reverse Recovered Charge	$I_{SD} = 75\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	39	nC

Notes:

- Starting $T_J = 25^\circ\text{C}$, $L = 0.255\text{mH}$, $I_{AS} = 70\text{A}$.
- Pulse Width = 100s

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

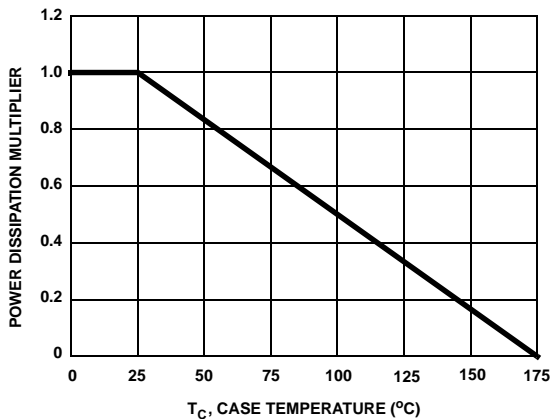


Figure 1. Normalized Power Dissipation vs Ambient Temperature

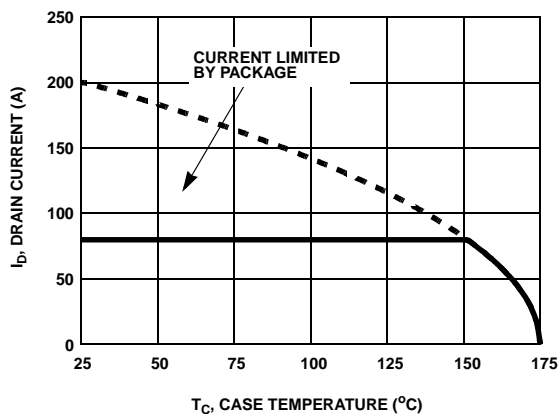


Figure 2. Maximum Continuous Drain Current vs Case Temperature

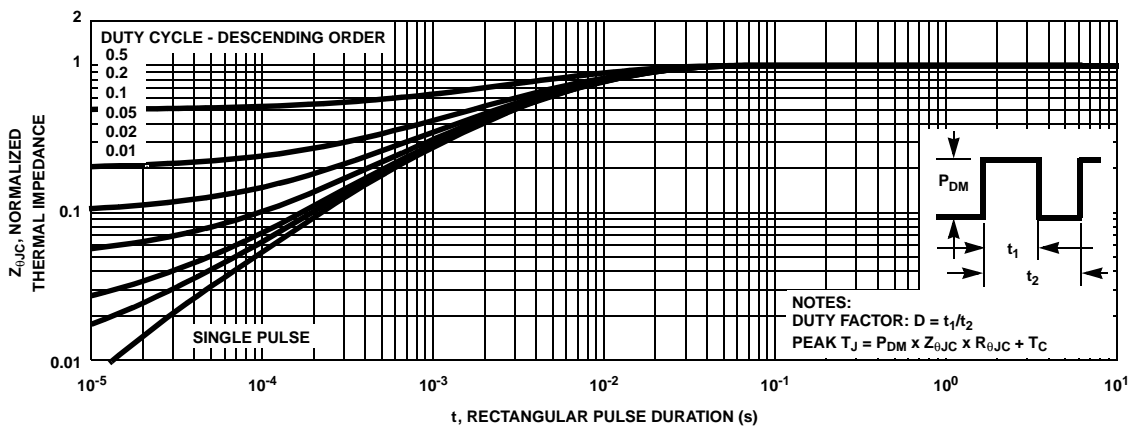


Figure 3. Normalized Maximum Transient Thermal Impedance

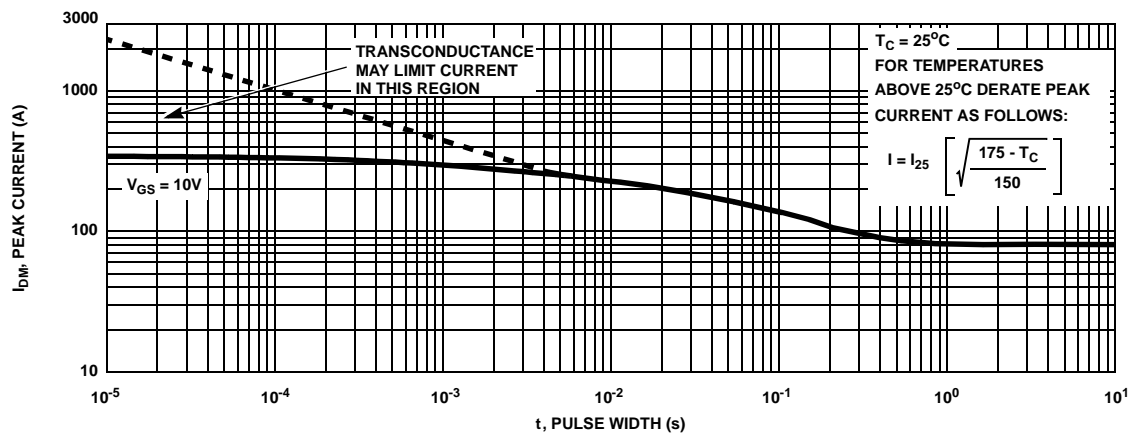


Figure 4. Peak Current Capability

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

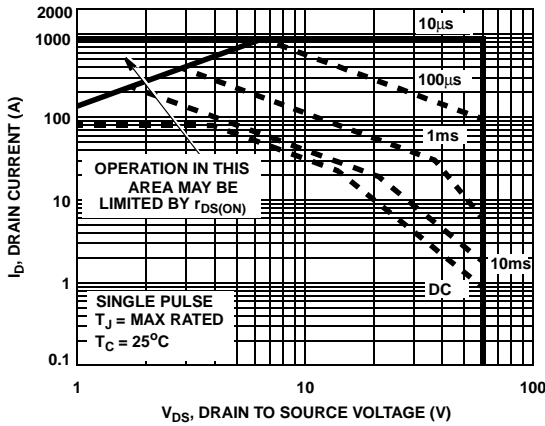
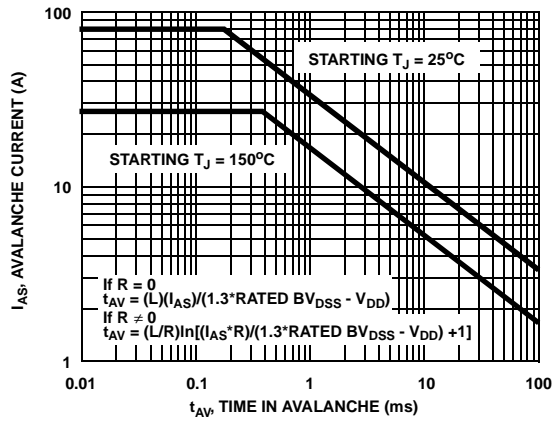


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

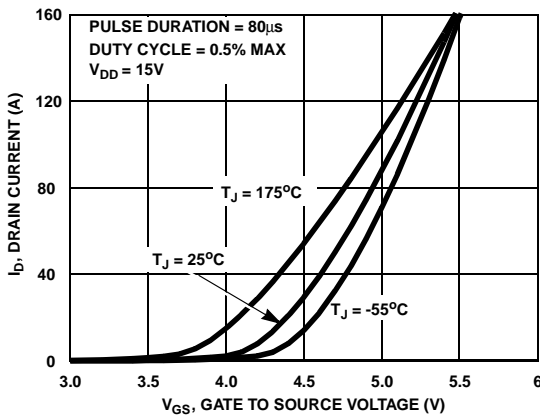


Figure 7. Transfer Characteristics

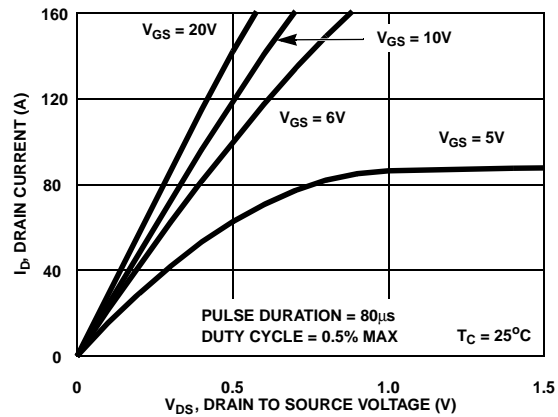


Figure 8. Saturation Characteristics

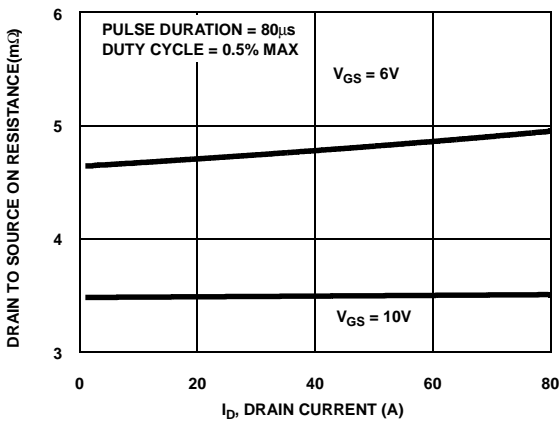


Figure 9. Drain to Source On Resistance vs Drain Current

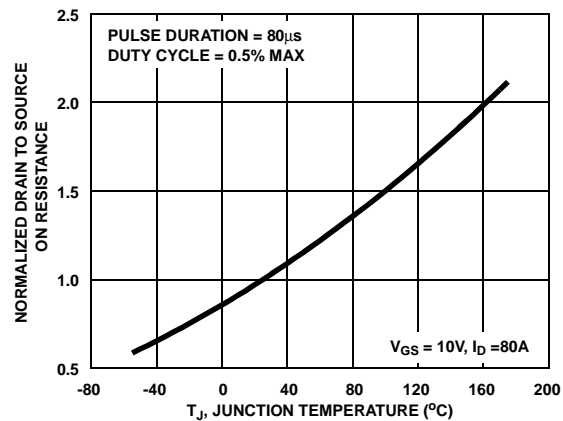


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

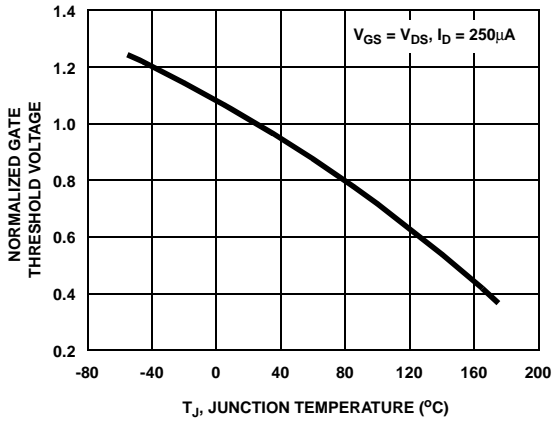


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

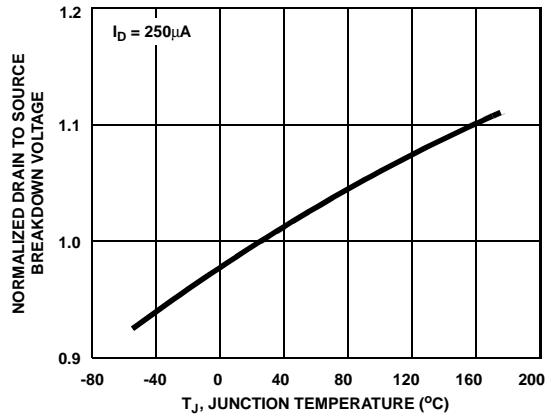


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

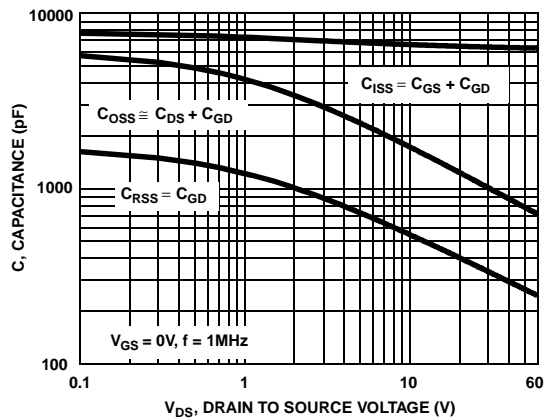


Figure 13. Capacitance vs Drain to Source Voltage

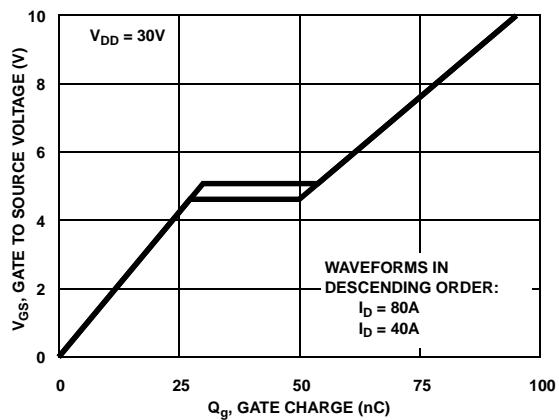


Figure 14. Gate Charge Waveforms for Constant Gate Current

Test Circuits and Waveforms

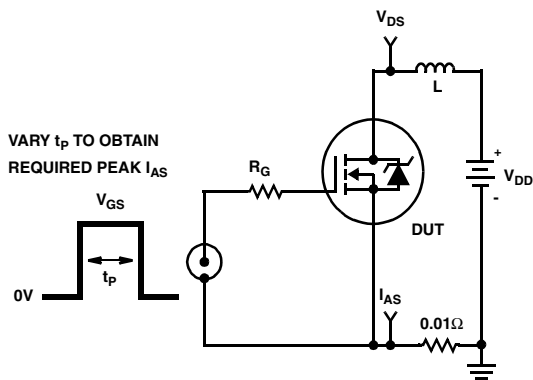


Figure 15. Unclamped Energy Test Circuit

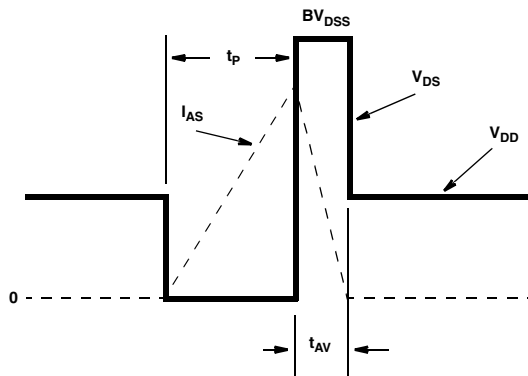


Figure 16. Unclamped Energy Waveforms

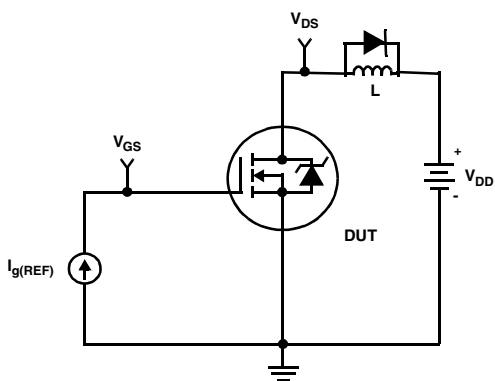


Figure 17. Gate Charge Test Circuit

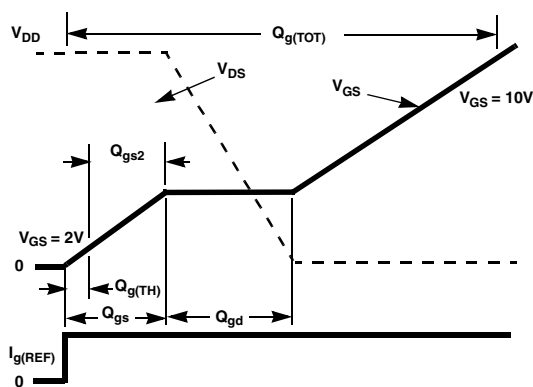


Figure 18. Gate Charge Waveforms

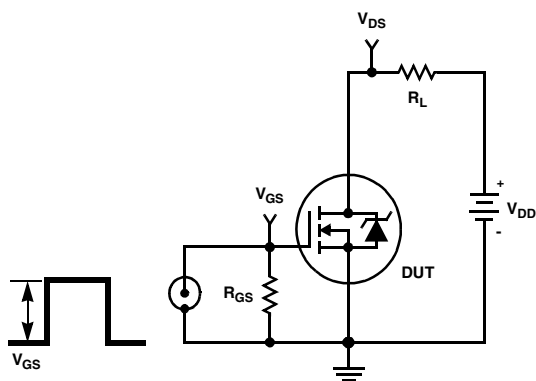


Figure 19. Switching Time Test Circuit

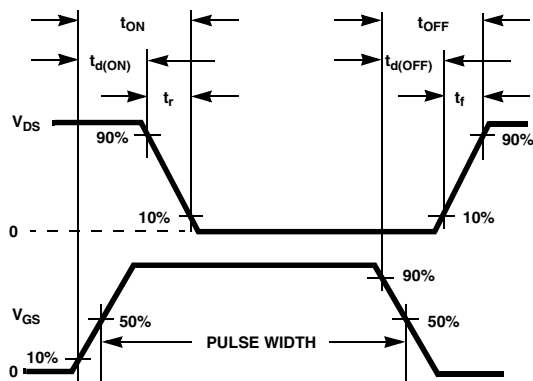


Figure 20. Switching Time Waveforms

PSPICE Electrical Model

.SUBCKT FDP038AN06A0 2 1 3 ; rev July 04, 2002
 Ca 12 8 1.5e-9
 Cb 15 14 1.5e-9
 Cin 6 8 6.1e-9

Dbody 7 5 DbodyMOD
 Dbreak 5 11 DbreakMOD
 Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 69.3
 Eds 14 8 5 8 1
 Egs 13 8 6 8 1
 Esg 6 10 6 8 1
 Evthres 6 21 19 8 1
 Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 4.81e-9
 Ldrain 2 5 1.0e-9
 Lsource 3 7 4.63e-9

RLgate 1 9 48.1
 RLdrain 2 5 10
 RLsource 3 7 46.3

Mmed 16 6 8 8 MmedMOD
 Mstro 16 6 8 8 MstroMOD
 Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
 Rdrain 50 16 RdrainMOD 1e-4
 Rgate 9 20 1.36
 RSLC1 5 51 RSLCMOD 1e-6
 RSLC2 5 50 1e3
 Rsource 8 7 RsourceMOD 2.8e-3
 Rvthres 22 8 RvthresMOD 1
 Rvtemp 18 19 RvtempMOD 1
 S1a 6 12 13 8 S1AMOD
 S1b 13 12 13 8 S1BMOD
 S2a 6 15 14 13 S2AMOD
 S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE={ (V(5,51)/ABS(V(5,51))) * (PWR(V(5,51))/(1e-6*250), 10) }

.MODEL DbodyMOD D (IS=2.4E-11 N=1.04 RS=1.65e-3 TRS1=2.7e-3 TRS2=2e-7 + CJO=4.35e-9 M=5.4e-1 TT=1e-9 XTI=3.9)

.MODEL DbreakMOD D (RS=1.5e-1 TRS1=1e-3 TRS2=-8.9e-6)

.MODEL DplcapMOD D (CJO=1.7e-9 IS=1e-30 N=10 M=0.47)

.MODEL MmedMOD NMOS (VTO=3.3 KP=9 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=1.36 T_abs=25)

.MODEL MstroMOD NMOS (VTO=4.00 KP=275 IS=1e-30 N=10 TOX=1 L=1u W=1u T_abs=25)

.MODEL MweakMOD NMOS (VTO=2.72 KP=0.03 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=13.6 RS=0.1 T_abs=25)

.MODEL RbreakMOD RES (TC1=9e-4 TC2=-9e-7)

.MODEL RdrainMOD RES (TC1=4e-2 TC2=3e-4)

.MODEL RSLCMOD RES (TC1=1e-3 TC2=1e-5)

.MODEL RsourceMOD RES (TC1=5e-3 TC2=1e-6)

.MODEL RvthresMOD RES (TC1=-6.7e-3 TC2=-1.5e-5)

.MODEL RvtempMOD RES (TC1=-2.5e-3 TC2=1e-6)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4 VOFF=-1.5)

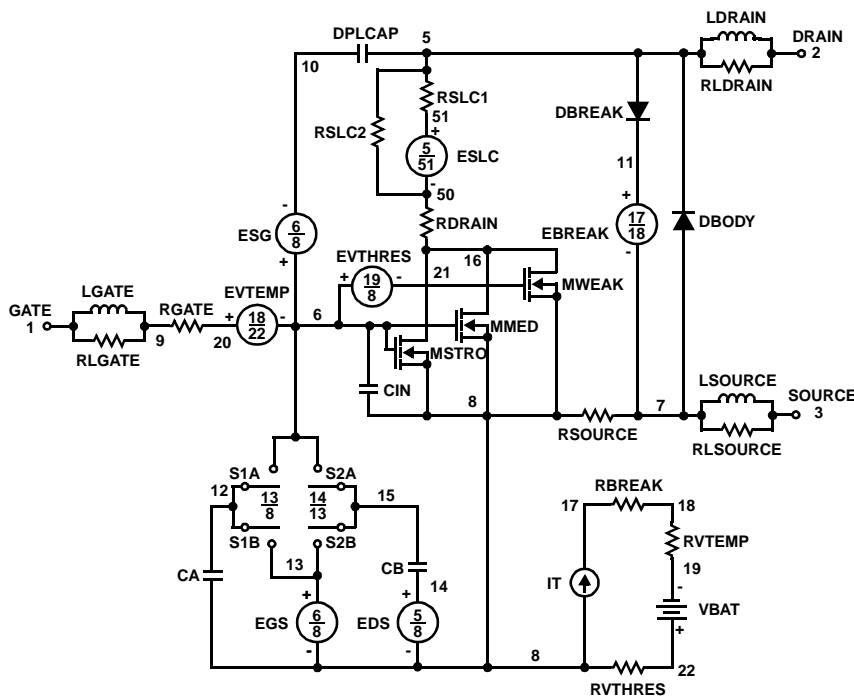
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.5 VOFF=-4)

.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1 VOFF=0.5)

.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.5 VOFF=-1)

.ENDS

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



SABER Electrical Model

rev July 4, 2002
 template FDP038AN06A0 n2,n1,n3 = m_temp
 electrical n2,n1,n3
 number m_temp=25

```
{
var i iscl
dp..model dbodymod = (isl=2.4e-11,nl=1.04,rs=1.65e-3,trs1=2.7e-3,trs2=2e-7,cjo=4.35e-9,m=5.4e-1,tt=1e-9,xti=3.9)
dp..model dbreakmod = (rs=1.5e-1,trs1=1e-3,trs2=-8.9e-6)
dp..model dplcapmod = (cjo=1.7e-9,isl=10e-30,nl=10,m=0.47)
m..model mmedmod = (type=_n,vto=3.3,kp=9,rs=1e-30,tox=1)
m..model mstrongmod = (type=_n,vto=4.00,kp=275,rs=1e-30,tox=1)
m..model mweakmod = (type=_n,vto=2.72,kp=0.03,rs=1e-30,tox=1,rs=0.1)
sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-4,voff=-1.5)
sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-1.5,voff=-4)
sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-1,voff=0.5)
sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=0.5,voff=-1)
c.ca n12 n8 = 1.5e-9
c.cb n15 n14 = 1.5e-9
c.cin n6 n8 = 6.1e-9
```

```
dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 69.3
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
```

i.it n8 n17 = 1

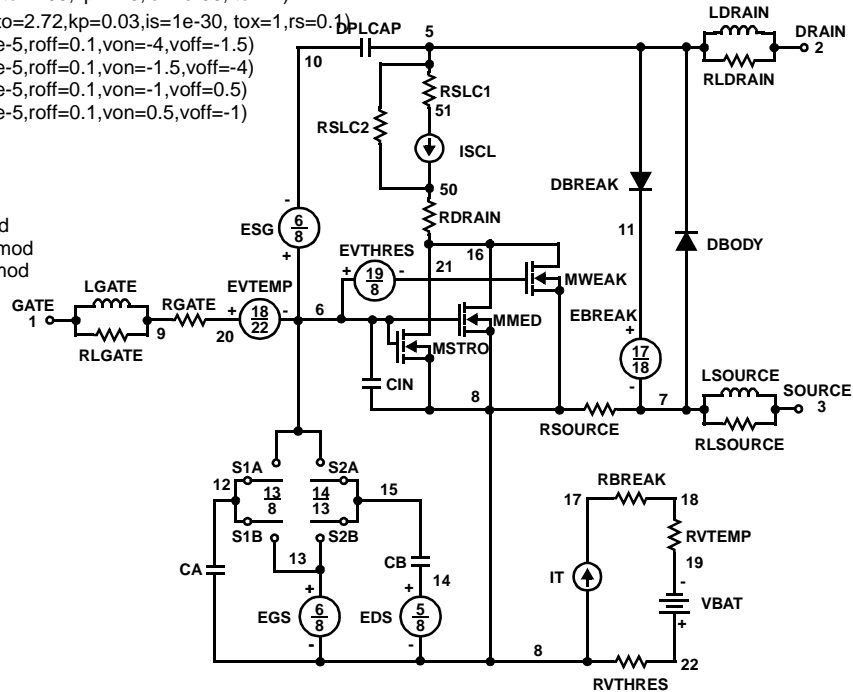
```
l.lgate n1 n9 = 4.81e-9
l.l drain n2 n5 = 1.0e-9
l.l source n3 n7 = 4.63e-9
```

```
res.rlgate n1 n9 = 48.1
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 46.3
```

```
m.mmed n16 n6 n8 n8 = model=mmedmod, temp=m_temp, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, temp=m_temp, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, temp=m_temp, l=1u, w=1u
```

```
res.rbreak n17 n18 = 1, tc1=9e-4,tc2=-9e-7
res.rdrain n50 n16 = 1e-4, tc1=4e-2,tc2=3e-4
res.rgate n9 n20 = 1.36
res.rslc1 n5 n51 = 1e-6, tc1=1e-3,tc2=1e-5
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 2.8e-3, tc1=5e-3,tc2=1e-6
res.rvthres n22 n8 = 1, tc1=-6.7e-3,tc2=-1.5e-5
res.rvtemp n18 n19 = 1, tc1=-2.5e-3,tc2=1e-6
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod
```

```
v.vbat n22 n19 = dc=1
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51)))))*((abs(v(n5,n51))*1e6/250)** 10)
}
```



FDP038AN06A0 / FDI038AN06A0 — N-Channel PowerTrench® MOSFET

SPICE Thermal Model

REV 23 July 4, 2002

FDP038AN06A0T

CTHERM1 TH 6 6.45e-3
 CTHERM2 6 5 3e-2
 CTHERM3 5 4 1.4e-2
 CTHERM4 4 3 1.65e-2
 CTHERM5 3 2 4.85e-2
 CTHERM6 2 TL 1e-1

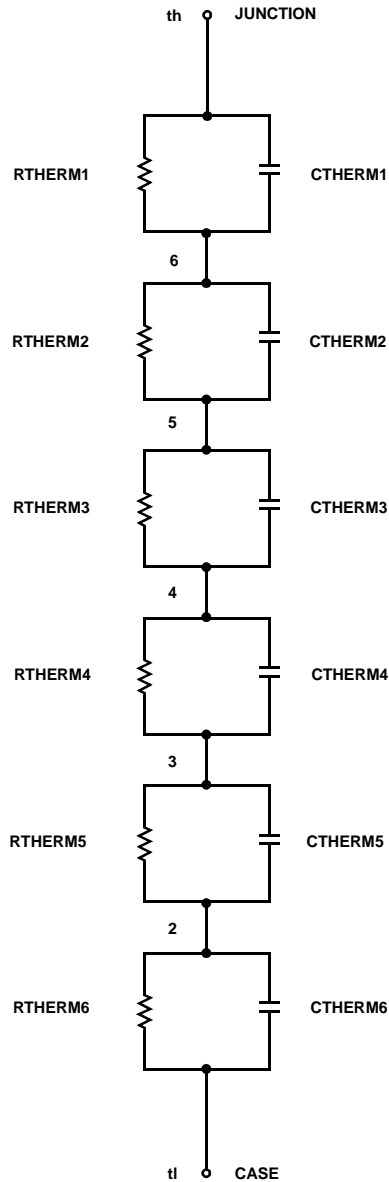
RTHERM1 TH 6 3.24e-3
 RTHERM2 6 5 8.08e-3
 RTHERM3 5 4 2.28e-2
 RTHERM4 4 3 1e-1
 RTHERM5 3 2 1.1e-1
 RTHERM6 2 TL 1.4e-1

SABER Thermal Model

SABER thermal model FDP035AN06A0T
 template thermal_model th tl
 thermal_c th, tl

```
{
    ctherm.ctherm1 th 6 =6.45e-3
    ctherm.ctherm2 6 5 =3e-2
    ctherm.ctherm3 5 4 =1.4e-2
    ctherm.ctherm4 4 3 =1.65e-2
    ctherm.ctherm5 3 2 =4.85e-2
    ctherm.ctherm6 2 tl =1e-1
```

```
rtherm.rtherm1 th 6 =3.24e-3
rtherm.rtherm2 6 5 =8.08e-3
rtherm.rtherm3 5 4 =2.28e-2
rtherm.rtherm4 4 3 =1e-1
rtherm.rtherm5 3 2 =1.1e-1
rtherm.rtherm6 2 tl =1.4e-1
}
```



Mechanical Dimensions

TO-220 3L

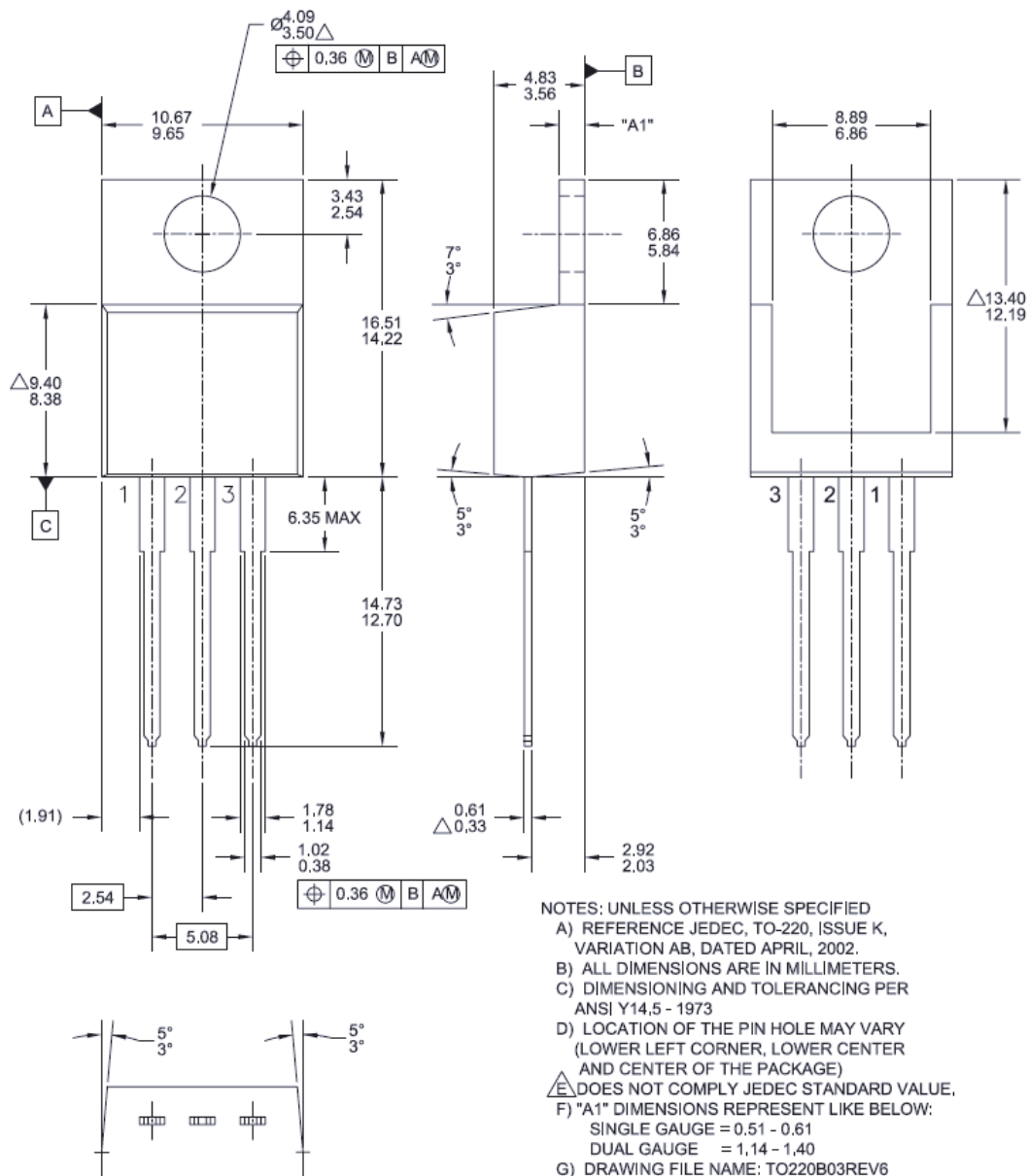


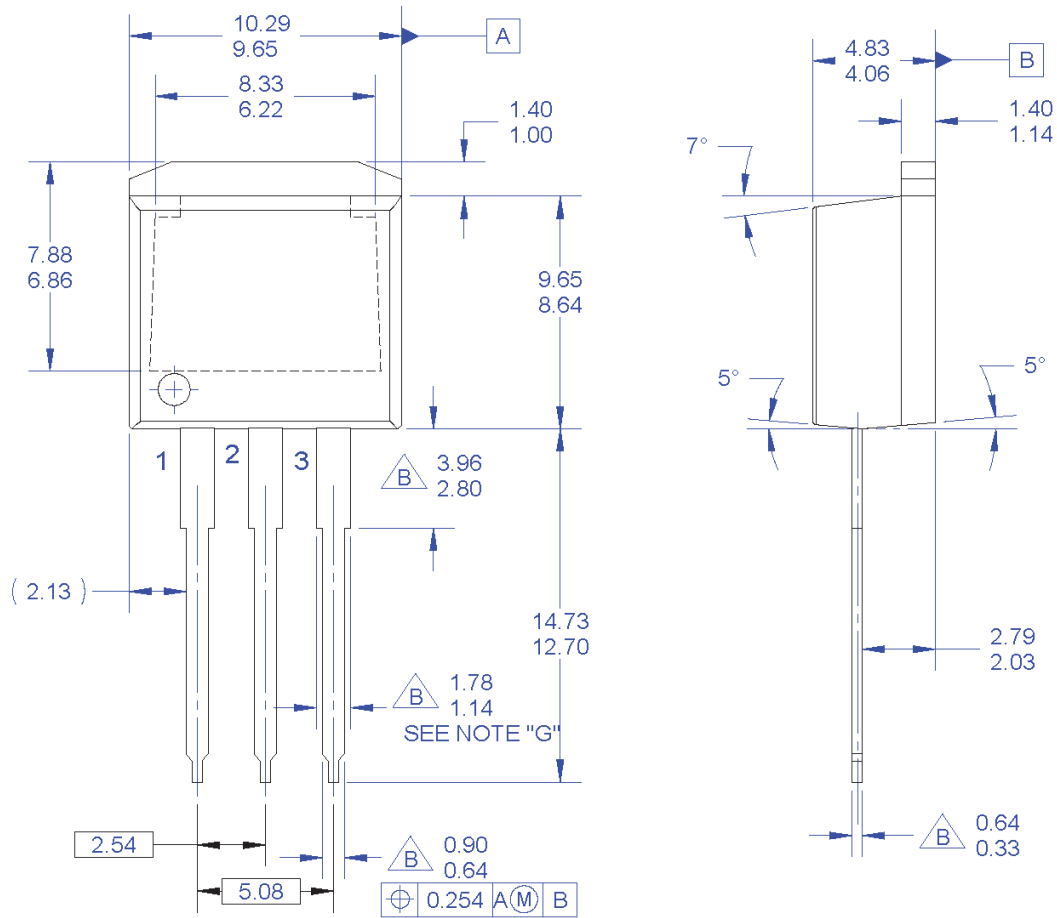
Figure 21. TO-220, Molded, 3Lead, Jedec Variation AB

Package drawings are provided as a service to customers considering ON Semiconductor components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a ON Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of ON Semiconductor's worldwide terms and conditions, specifically the warranty therein, which covers ON Semiconductor products.

Dimension in Millimeters

Mechanical Dimensions

TO-262 3L (I²PAK)



NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO TO262 JEDEC VARIATION AA.
- B. DOES NOT COMPLY JEDEC STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.
- F. LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)
- G. MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.
- H. DRAWING FILE NAME: TO262A03REV5

Figure 22. 3LD, TO262, Jedec Variation AA (I²PAK)

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Dimension in Millimeters

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