FDP045N10A / FDI045N10A

MOSFET – N-Channel, POWERTRENCH®

100 V, 164 A, 4.5 mΩ

Description

This N−Channel MOSFET is produced using ON Semiconductor's advance POWERTRENCH process that has been tailored to minimize the on−state resistance while maintaining superior switching performance.

Features

- $R_{DS(on)}$ = 3.8 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 100 A
- Fast Switching Speed
- Low Gate Charge, Q_G = 54 nC (Typ.)
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- This Device is Pb−Free and is RoHS Compliant

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

ON Semiconductor®

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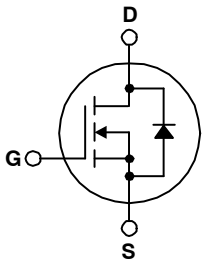
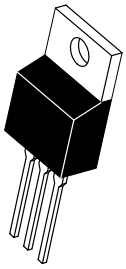
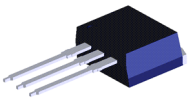


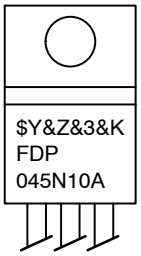


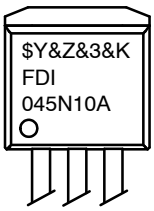


TO−220
CASE 221A−09

I²PAK
CASE 418AV

MARKING DIAGRAM





$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDP/FDI045N10A	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

MOSFET MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

Symbol	Parameter		FDP045N10A_F102 FDI045N10A_F102	Unit
V_{DSS}	Drain to Source Voltage		100	V
V_{GSS}	Gate to Source Voltage		±20	V
I_D	Drain Current	– Continuous (T_C = 25°C, Silicon Limited)	164*	A
		– Continuous (T_C = 100°C, Silicon LImited)	116	
		– Continuous (T_C = 25°C, Package Limited)	120	
I_{DM}	Drain Current	– Pulsed (Note 1)	656	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		637	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		6.0	V/ns
P_D	Power Dissipation	(T_C = 25°C)	263	W
		– Derate Above 25°C	1.75	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		–55 to +175	°C
T_L	Maximum Lead Temperature for Soldering, 1/8” from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120 A.

THERMAL CHARACTERISTICS

Symbol	Parameter	FDP045N10A_F102 FDI045N10A_F102	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.57	°C
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP045N10A_F102	FDP045N10A	TO–220	Tube	N/A	N/A	50 Units
FDI045N10A_F102	FDI045N10A	I^2–PAK	Tube	N/A	N/A	50 Units

ELECTRICAL CHARACTERISTICS (T_C = 25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 mA, V_{GS} = 0 V	100	–	–	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 mA, Referenced to 25°C	–	0.07	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 80 V, T_C = 150°C	–	–	500	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 mA	2.0	–	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 100 A	–	3.8	4.5	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 100 A	–	132	–	S

ELECTRICAL CHARACTERISTICS (T_C = 25°C Unless Otherwise Noted) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	–	3960	5270	pF
C_{oss}	Output Capacitance		–	925	1230	pF
C_{rss}	Reverse Transfer Capacitance		–	34	–	pF
$C_{oss(er)}$	Engry Releted Output Capacitance	V_{DS} = 50 V, V_{GS} = 0 V	–	1520	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{GS} = 10 V, V_{DS} = 50 V, I_D = 100 A (Note 4)	–	54	74	nC
Q_{gs}	Gate to Source Gate Charge		–	17	–	nC
Q_{gs2}	Gate Charge Threshold to Plateau		–	8	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	13	–	nC
ESR	Equivalent Series Resistance (G−S)	f = 1 MHz	–	1.9	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 50 V, I_D = 100 A, V_{GS} = 10 V, R_G = 4.7 Ω (Note 4)	–	23	56	ns
t_r	Turn−On Rise Time		–	26	62	ns
$t_{d(off)}$	Turn−Off Delay Time		–	50	110	ns
t_f	Turn−Off Fall Time		–	15	40	ns
DRAIN−SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	164*	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	656	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 100 A	–	–	1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, V_{DD} = 50 V, I_{SD} = 100 A, dI_F/dt = 100 A/ms	–	75	–	ns
Q_{rr}	Reverse Recovery Charge		–	120	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. L = 3 mH, I_{AS} = 20.6 A, R_G = 25 Ω, starting T_J = 25°C.
3. $I_{SD} \le$ 100 A, di/dt $\le$ 200 A/μs, $V_{DD} \le BV_{DSS}$, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

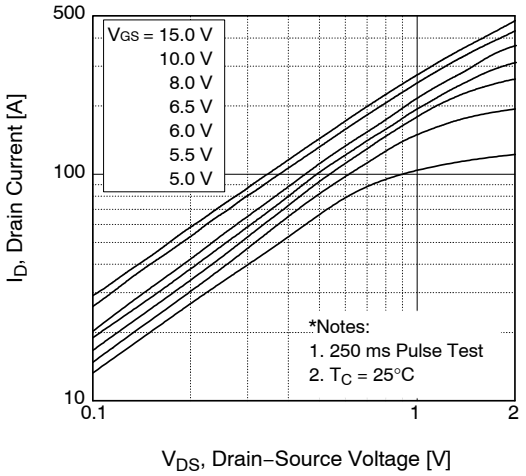


Figure 1. On−Region Characteristics

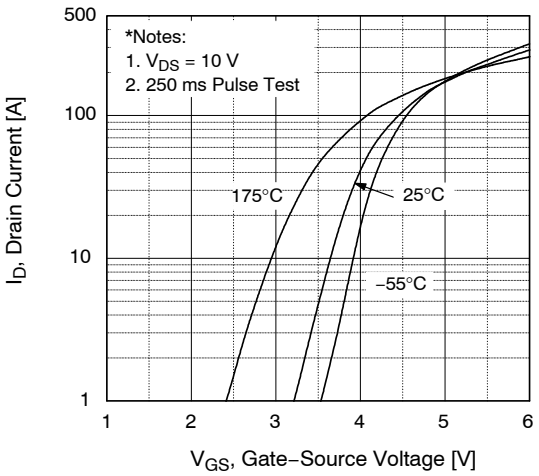


Figure 2. Transfer Characteristics

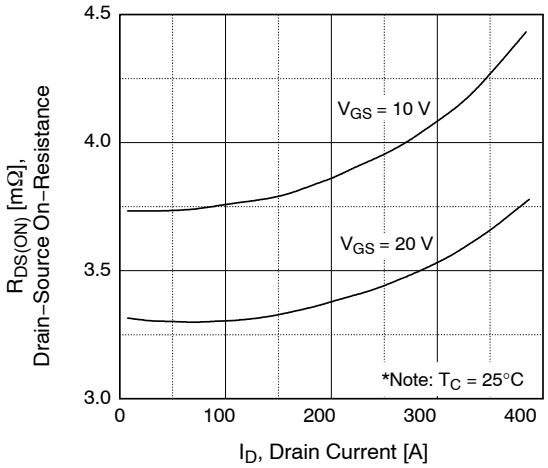


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

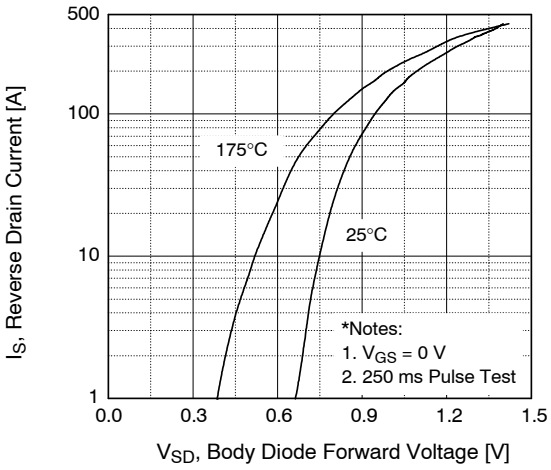


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

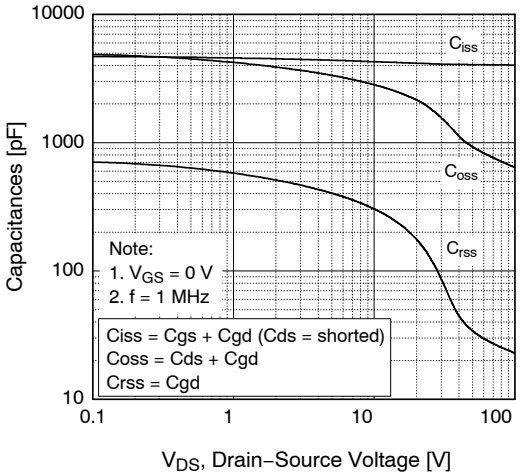


Figure 5. Capacitance Characteristics

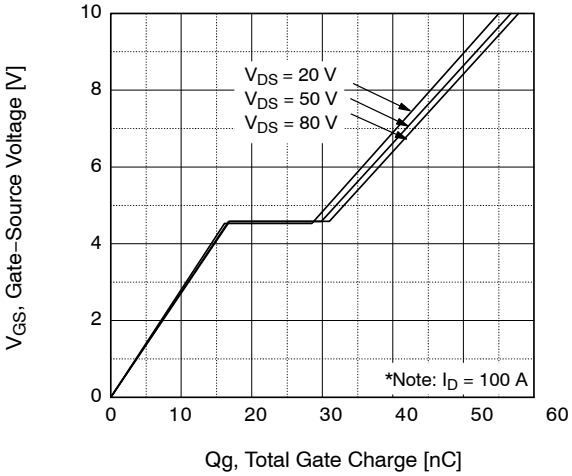


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

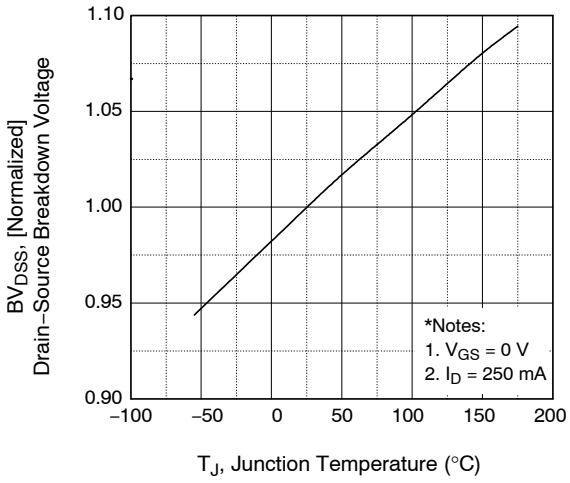


Figure 7. Maximum Safe Operating Area

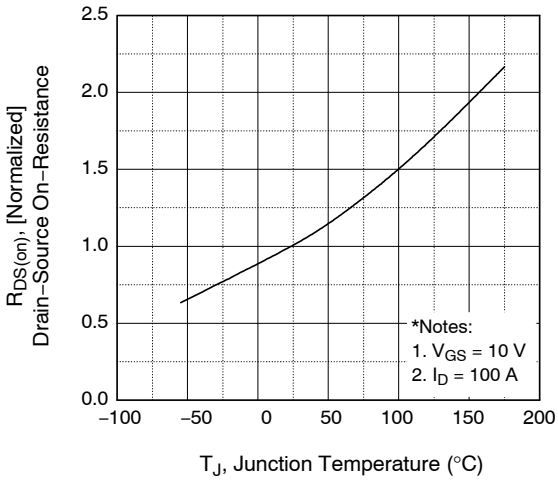


Figure 8. On−Resistance Variation vs. Temperature

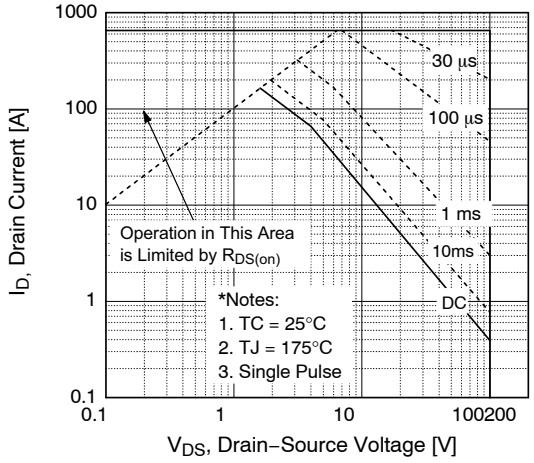


Figure 9. Maximum Safe Operating Area

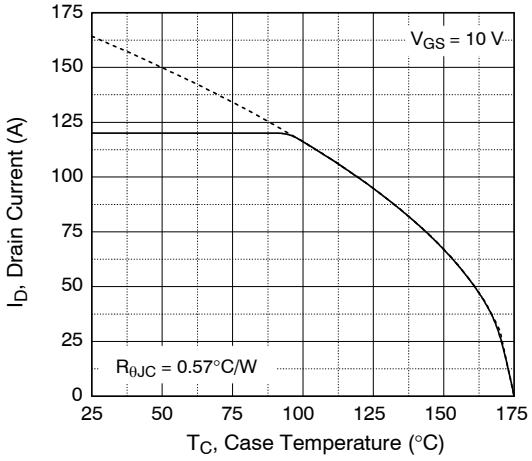


Figure 10. Maximum Drain Current vs. Case Temperature

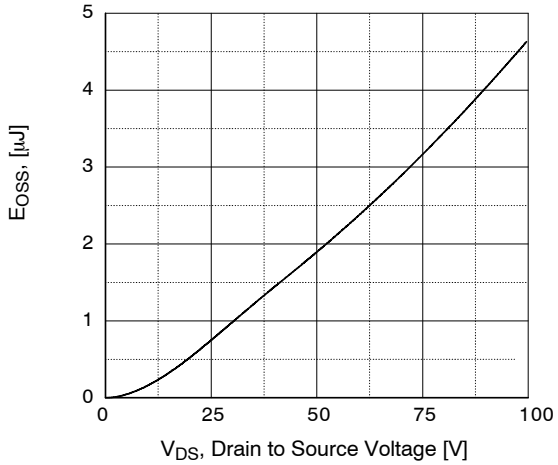


Figure 11. Eoss vs. Drain to Source Voltage

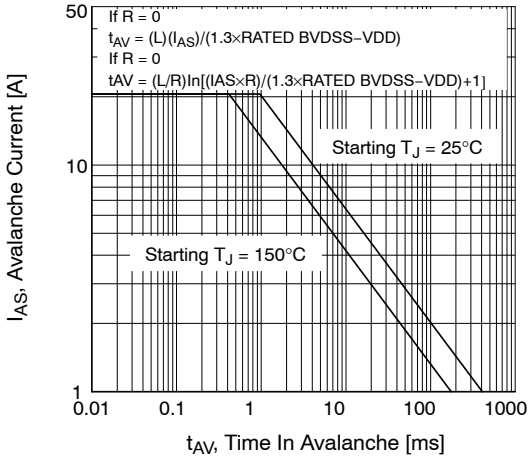


Figure 12. Unclamped Inductive Switching Capability

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

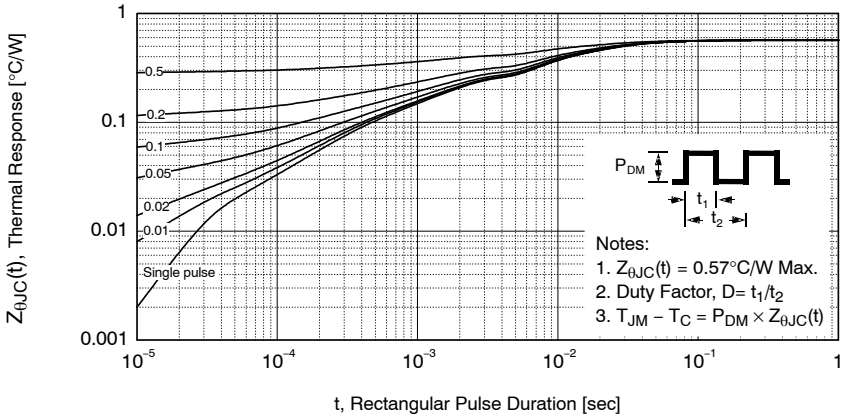


Figure 13. Transient Thermal Response Curve

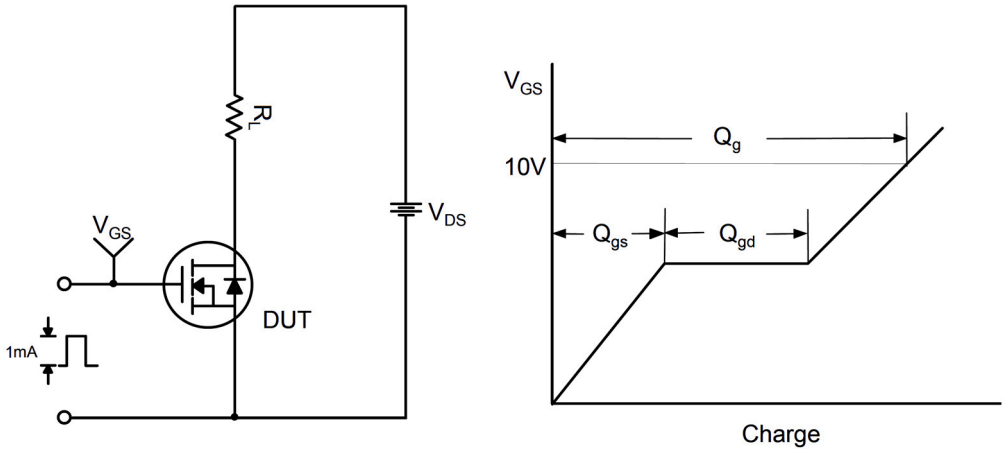


Figure 14. Gate Charge Test Circuit & Waveform

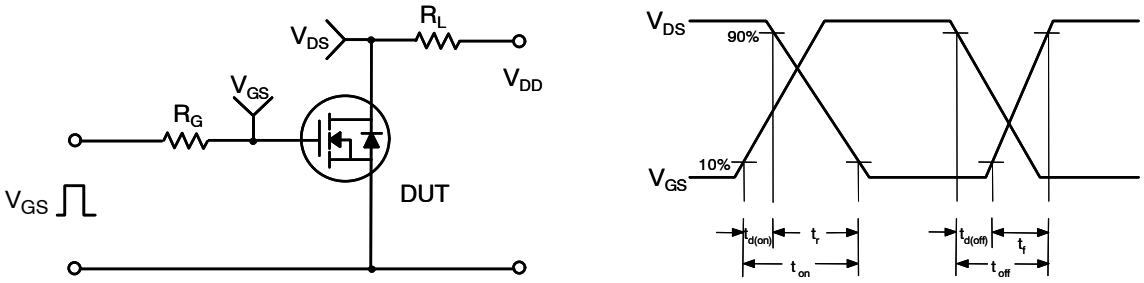


Figure 15. Resistive Switching Test Circuit & Waveforms

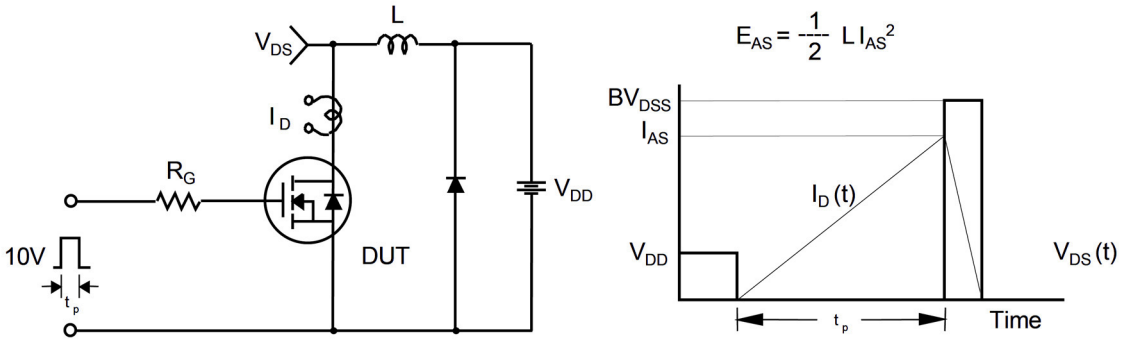


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

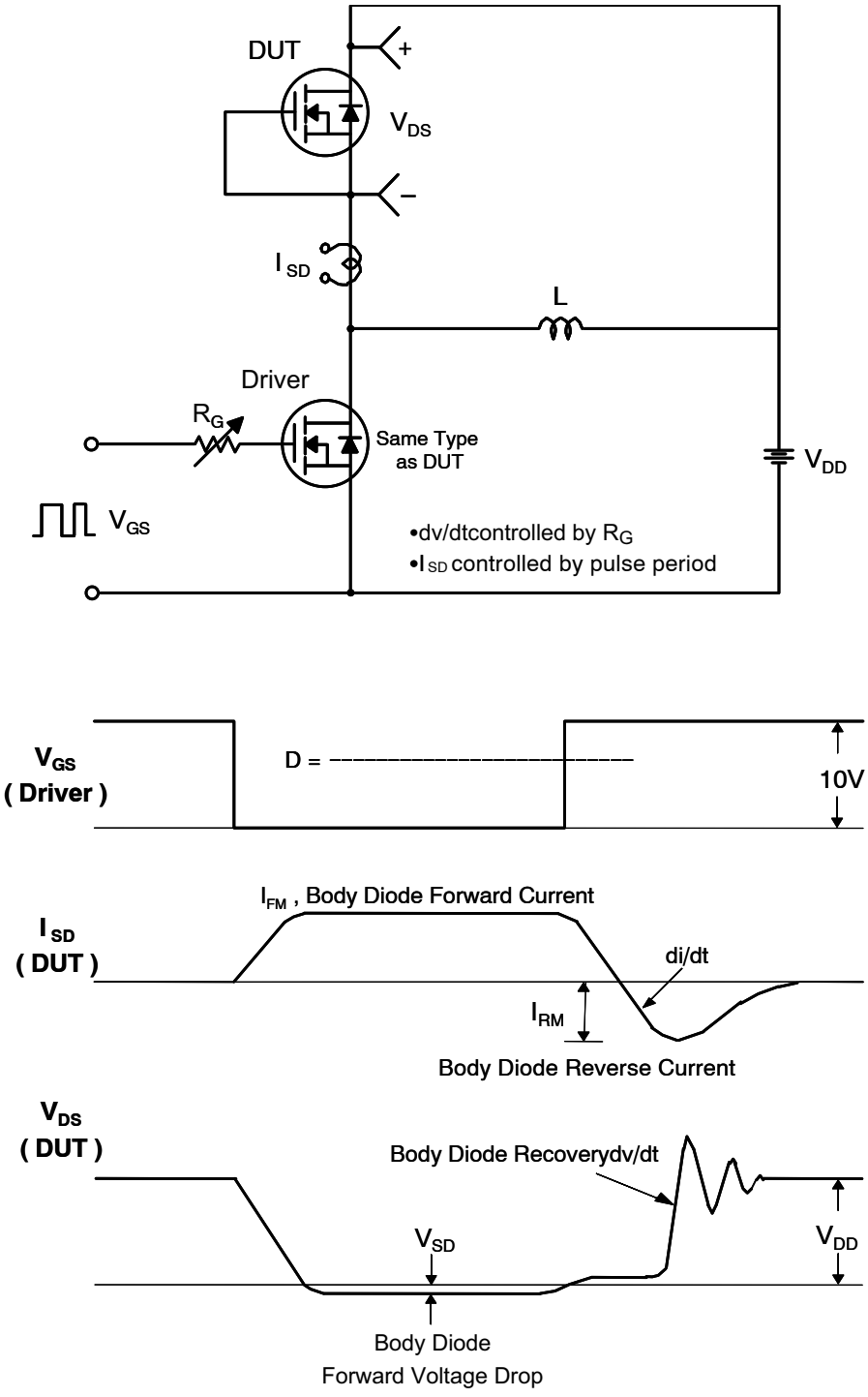


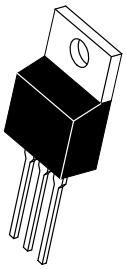
Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

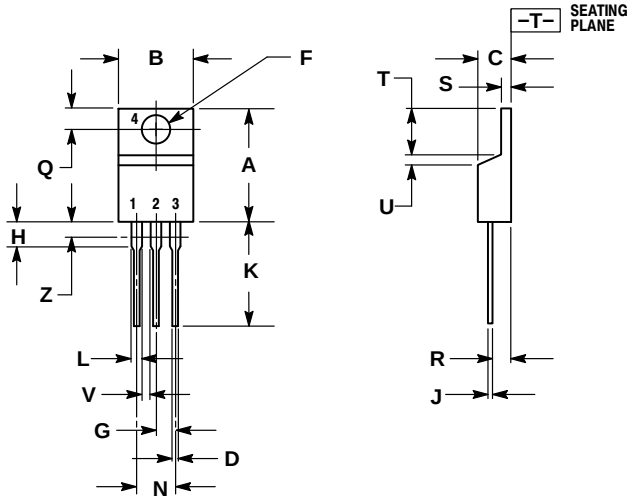
ON Semiconductor®

TO−220
CASE 221A−09
ISSUE AH

DATE 28 AUG 2014



SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

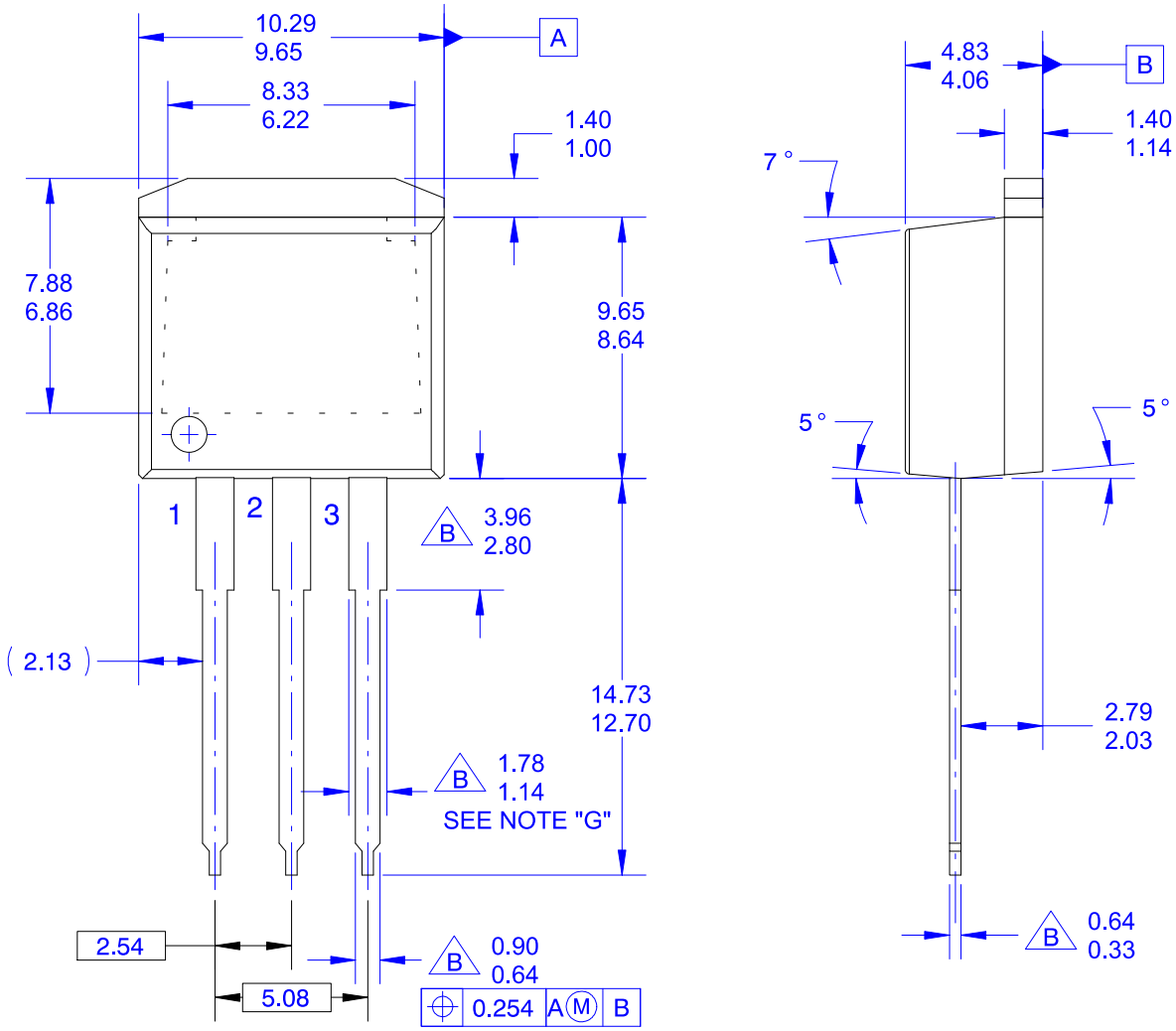
STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

ISSUE	REVISION	DATE
AB	CHANGED MINIMUM DIMENSION FOR S FROM 0.045 (1.15) TO 0.020 (0.508). REQ. BY W. LOW.	04 MAY 2006
AC	INTERNAL REVISION IN DDCM	30 MAY 2006
AD	REVERSED CHANGES FROM REVISION AB. RETURNED DIMENSION S TO DUAL GAUGE VALUES. REQ. BY M. SCHAGER.	17 JUL 2006
AE	CHANGED MAXIMUM DIMENSION F FROM 0.147 INCH (3.73MM) TO 0.16 1INCH (4.09MM) AND MINIMUM DIMENSION FOR J FROM 0.018 INCH (0.46MM) TO 0.014 INCH (0.36MM). REQ. BY M. SCHAGER.	13 APR 2007
AF	ADDED STYLE 12. REQ. BY A. ANGUS.	26 NOV 2007
AG	CHANGED DIMENSIONS D AND H MAX LIMITS TO 0.036 (0.91) AND 0.161 (4.10) RESPECTIVELY. REQ. BY J. RAMIREZ.	16 SEP 2011
AH	MODIFIED MAXIMUM VALUES OF DIMENSIONS B TO 0.415 (10.53), C TO 0.190 (4.83), D TO 0.038 (0.96), & J TO 0.024 (0.61) TO MATCH SUB−CONTRACTORS SPECS. REQ. BY J. MORRIS.	28 AUG 2014

I2PAK (TO−262 3 LD)
CASE 418AV
ISSUE O

DATE 30 SEP 2016



NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO TO262 JEDEC VARIATION AA.
B. DOES NOT COMPLY JEDEC STD. VALUE.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.
F. LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)
G. MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION FROM FAIRCHILD TO262A03 TO ON SEMICONDUCTOR. REQ. BY I. CAMBALIZA.	30 SEP 2016

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
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