

# MOSFET - N-Channel PowerTrench®



ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)

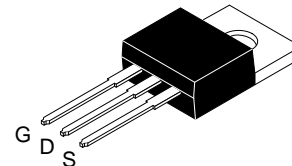
## FDP42AN15A0 150 V, 35 A, 42 mΩ

### Features

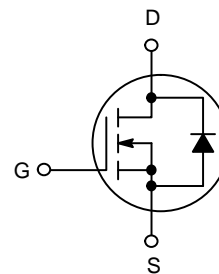
- $R_{DS(on)} = 36 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 12 \text{ A}$
- $Q_{G(tot)} = 33 \text{ nC}$  (Typ.) @  $V_{GS} = 10 \text{ V}$
- Low Miller Charge
- Low  $Q_{rr}$  Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- These Devices are Pb-Free and are RoHS Compliant

### Applications

- Consumer Appliances
- Synchronous Rectification
- Uninterruptible Power Supply
- Micro Solar Inverter



TO-220  
CASE 340AT



### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain to Source Voltage	$V_{DSS}$	150	V
Gate to Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current – Continuous ( $V_{GS} = 10 \text{ V}$ , $T_C = 25^\circ\text{C}$ )	$I_D$	35	A
Continuous ( $V_{GS} = 10 \text{ V}$ , $T_C = 100^\circ\text{C}$ )		24	A
Continuous ( $T_{amb} = 25^\circ\text{C}$ , $V_{GS} = 10 \text{ V}$ , with $R_{\theta JA} = 43^\circ\text{C/W}$ )		5	A
Pulsed		Figure 4	A
Single Pulse Avalanche Energy	$E_{AS}$	90	mJ
Power Dissipation	$P_D$	150	W
Derate above $25^\circ\text{C}$		1.0	W/ $^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{STG}$	-55 to +175	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Thermal Resistance (Junction to Case)	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$
Maximum Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	62	$^\circ\text{C/W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Quantity
FDP42AN15A0	FDP42AN15A0	TO-220	Tube	N/A	50 Units

# FDP42AN15A0

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
--------	-----------	-----------------	-----	-----	-----	------

### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	150	–	–	V	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 120 V, V <sub>GS</sub> = 0 V	T <sub>C</sub> = 25°C	–	–	1	μA
			T <sub>C</sub> = 150°C	–	–	250	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V	–	–	±100	nA	

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	2	–	4	V
R <sub>DS(on)</sub>	Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 12 A	–	0.036	0.042	Ω
		V <sub>GS</sub> = 6 V, I <sub>D</sub> = 6 A	–	0.040	0.060	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 12 A, T <sub>J</sub> = 175°C	–	0.090	0.107	Ω

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	2150	–	pF	
C <sub>oss</sub>	Output Capacitance		–	225	–	pF	
C <sub>rss</sub>	Reverse Transfer Capacitance		–	45	–	pF	
Q <sub>g(tot)</sub>	Total Gate Charge at 10 V	V <sub>DD</sub> = 75 V, I <sub>D</sub> = 12 A, I <sub>g</sub> = 1.0 mA	V <sub>GS</sub> = 0 V to 10 V	–	30	39	nC
Q <sub>g(th)</sub>	Threshold Gate Charge		V <sub>GS</sub> = 0 V to 2 V	–	4.2	5.4	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	V <sub>DD</sub> = 75 V, I <sub>D</sub> = 12 A, I <sub>g</sub> = 1.0 mA	–	9.5	–	nC	
Q <sub>gs2</sub>	Gate Charge Threshold to Plateau		–	5.3	–	nC	
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		–	6.9	–	nC	

### SWITCHING CHARACTERISTICS (V<sub>GS</sub> = 10 V)

t <sub>on</sub>	Turn-On Time	V <sub>DD</sub> = 75 V, I <sub>D</sub> = 12 A, V <sub>GS</sub> = 10 V, R <sub>GS</sub> = 7.5 Ω	–	–	46	ns
t <sub>d(on)</sub>	Turn-On Delay Time		–	11	–	ns
t <sub>r</sub>	Rise Time		–	19	–	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		–	27	–	ns
t <sub>f</sub>	Fall Time		–	23	–	ns
t <sub>off</sub>	Turn-Off Time		–	–	74	ns

### DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Source to Drain Diode Voltage	I <sub>SD</sub> = 12 A	–	–	1.25	V
		I <sub>SD</sub> = 6 A	–	–	1.0	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>SD</sub> = 12 A, dI <sub>SD</sub> /dt = 100 A/μs	–	–	82	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	–	204	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Starting T<sub>J</sub> = 25°C, L = 0.2 mH, I<sub>AS</sub> = 30 A.

# FDP42AN15A0

## TYPICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

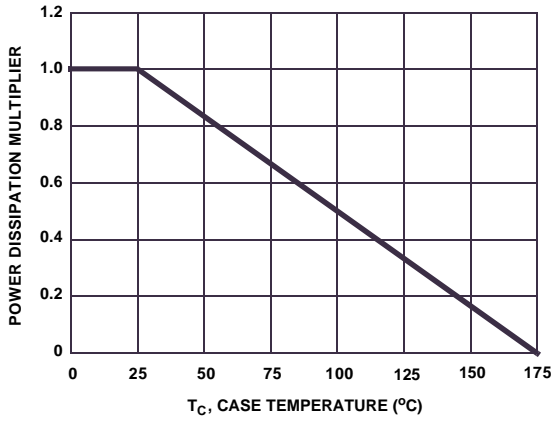


Figure 1. Normalized Power Dissipation vs. Ambient Temperature

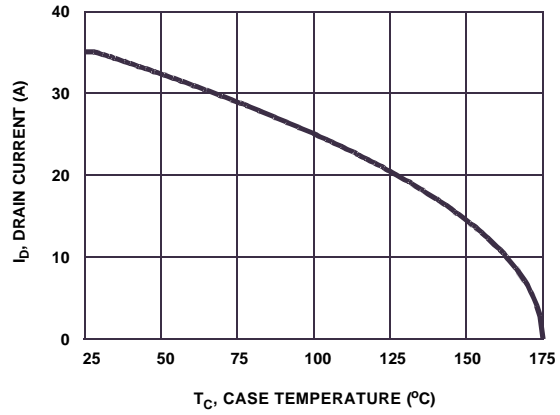


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

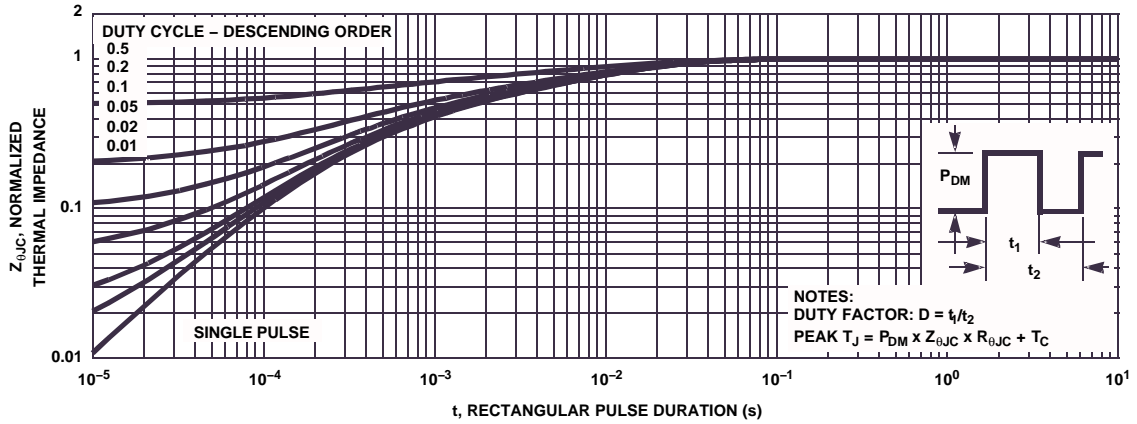


Figure 3. Normalized Maximum Transient Thermal Impedance

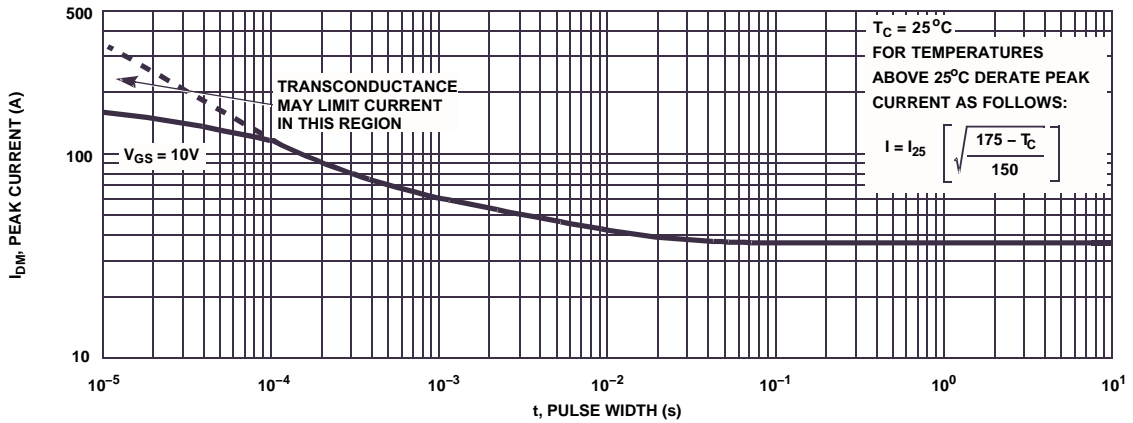


Figure 4. Peak Current Capability

# FDP42AN15A0

## TYPICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

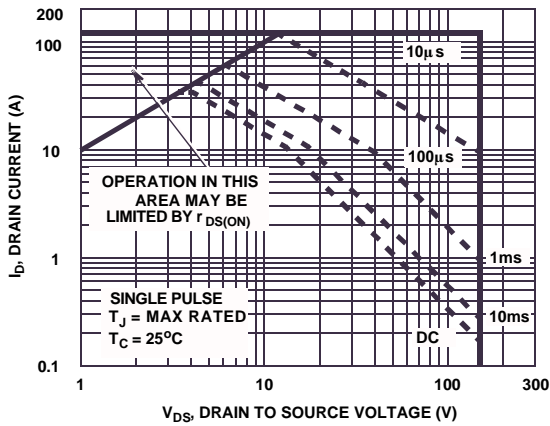
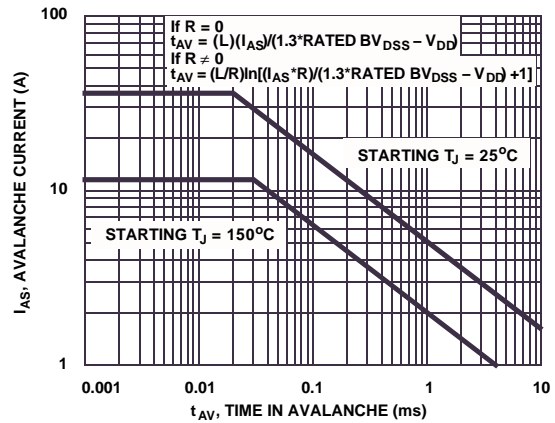


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

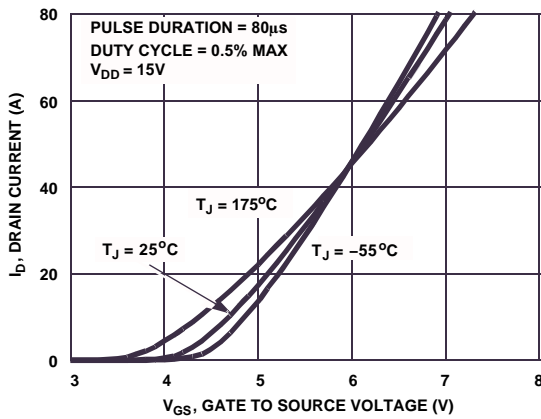


Figure 7. Transfer Characteristics

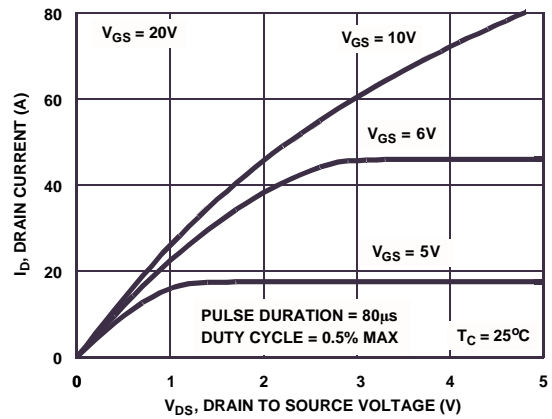


Figure 8. Saturation Characteristics

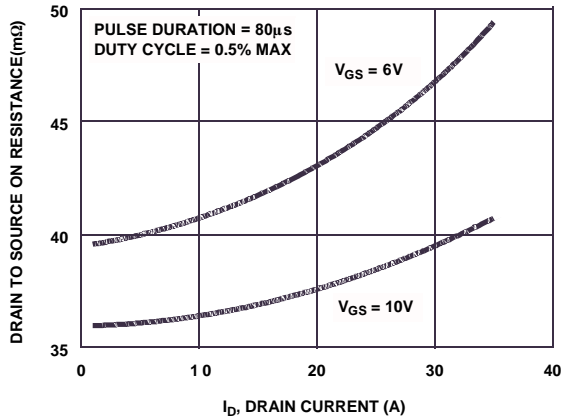


Figure 9. Drain to Source On Resistance vs. Drain Current

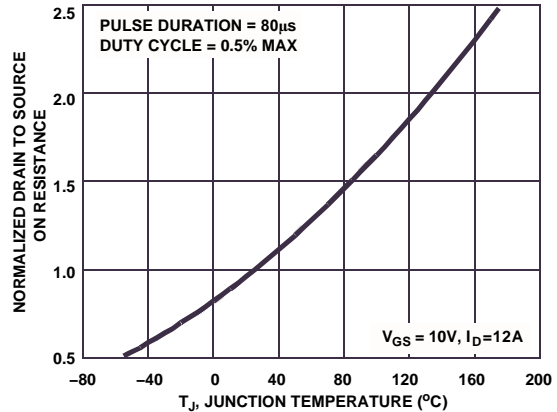


Figure 10. Normalized Drain to Source On Resistance vs. Junction Temperature

# FDP42AN15A0

## TYPICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

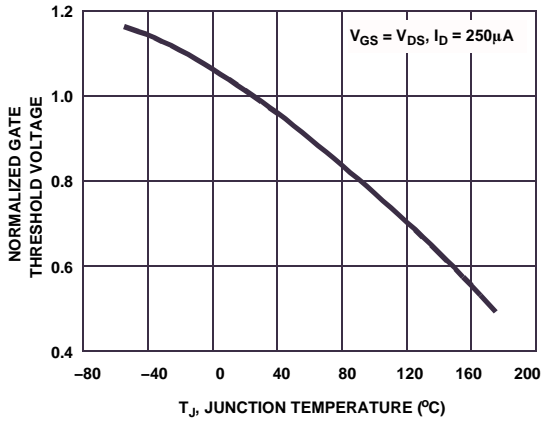


Figure 11. Normalized Gate Threshold Voltage vs. Junction Temperature

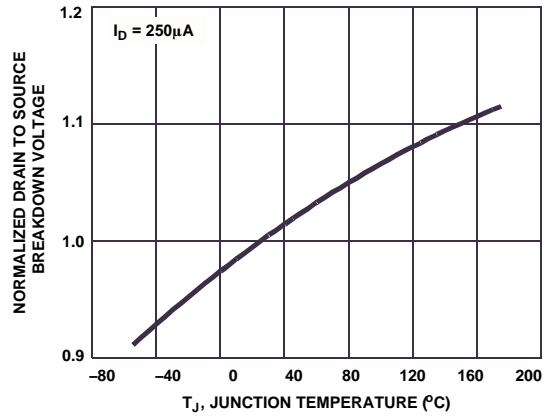


Figure 12. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

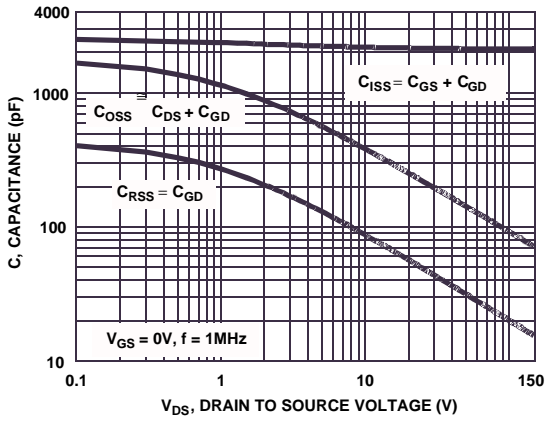


Figure 13. Capacitance vs. Drain to Source Voltage

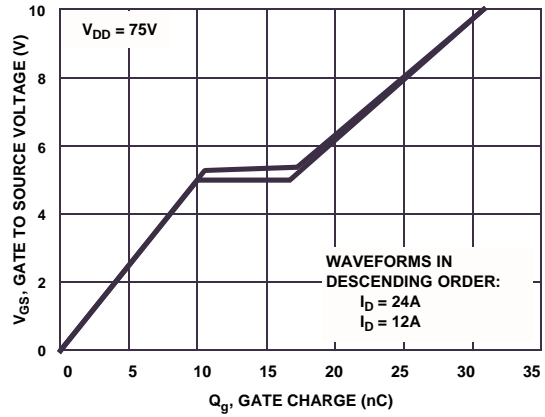


Figure 14. Gate Charge Waveforms for Constant Gate Current

Test Circuits and Waveforms

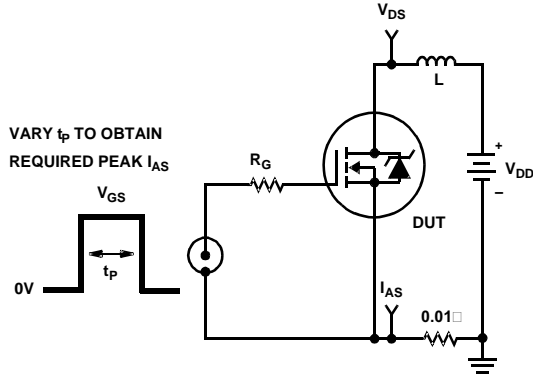


Figure 15. Unclamped Energy Test Circuit

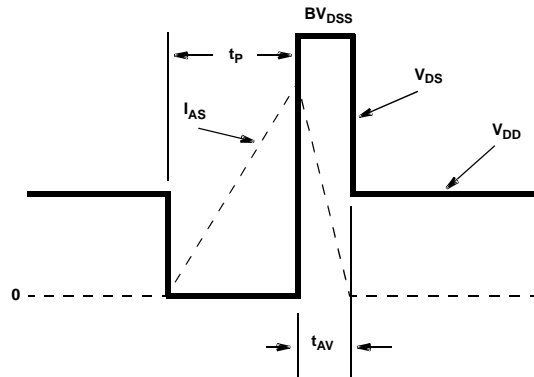


Figure 16. Unclamped Energy Waveforms

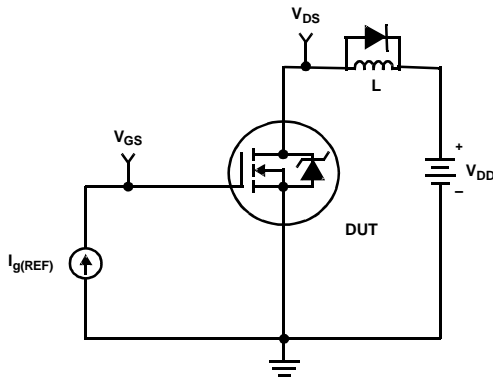


Figure 17. Gate Charge Test Circuit

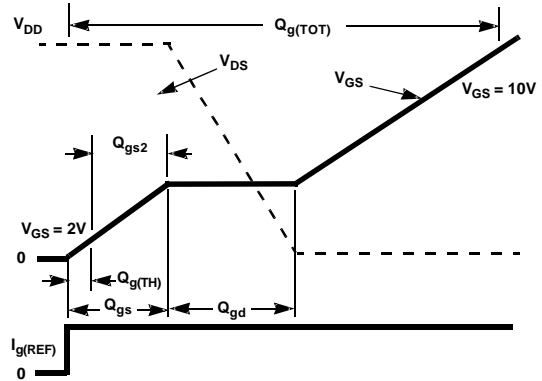


Figure 18. Gate Charge Waveforms

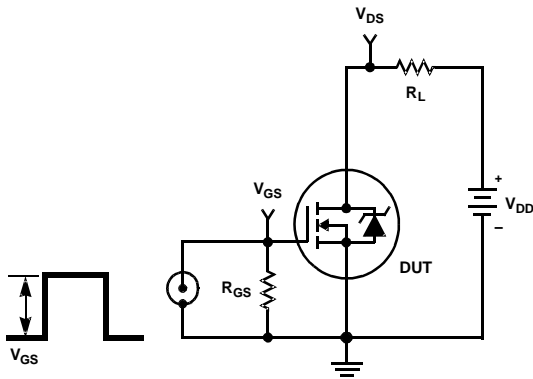


Figure 19. Switching Time Test Circuit

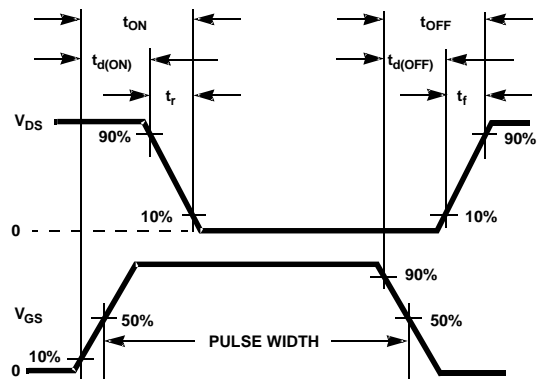


Figure 20. Switching Time Waveforms

# FDP42AN15A0

## PSPICE Electrical Model

.SUBCKT FDB42AN15A0 2 1 3 ; rev June 11, 2002  
 Ca 12 8 6.0e-10  
 Cb 15 14 8e-10  
 Cin 6 8 2.1e-9

Dbody 7 5 DbodyMOD  
 Dbreak 5 11 DbreakMOD  
 Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 159.5  
 Eds 14 8 5 8 1  
 Egs 13 8 6 8 1  
 Esg 6 10 6 8 1  
 Evthres 6 21 19 8 1  
 Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 4.81e-9  
 Ldrain 2 5 1.0e-9  
 Lsource 3 7 4.63e-9

RLgate 1 9 48.1  
 RLdrain 2 5 10  
 RLsource 3 7 46.3

Mmed 16 6 8 8 MmedMOD  
 Mstro 16 6 8 8 MstroMOD  
 Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1  
 Rdrain 50 16 RdrainMOD 14e-3  
 Rgate 9 20 1.36  
 RSLC1 5 51 RSLCMOD 1e-6  
 RSLC2 5 50 1e3  
 Rsource 8 7 RsourceMOD 20e-3  
 Rvthres 22 8 RvthresMOD 1  
 Rvtemp 18 19 RvtempMOD 1  
 S1a 6 12 13 8 S1AMOD  
 S1b 13 12 13 8 S1BMOD  
 S2a 6 15 14 13 S2AMOD  
 S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE=((V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51)/(1e-6\*65),3)))

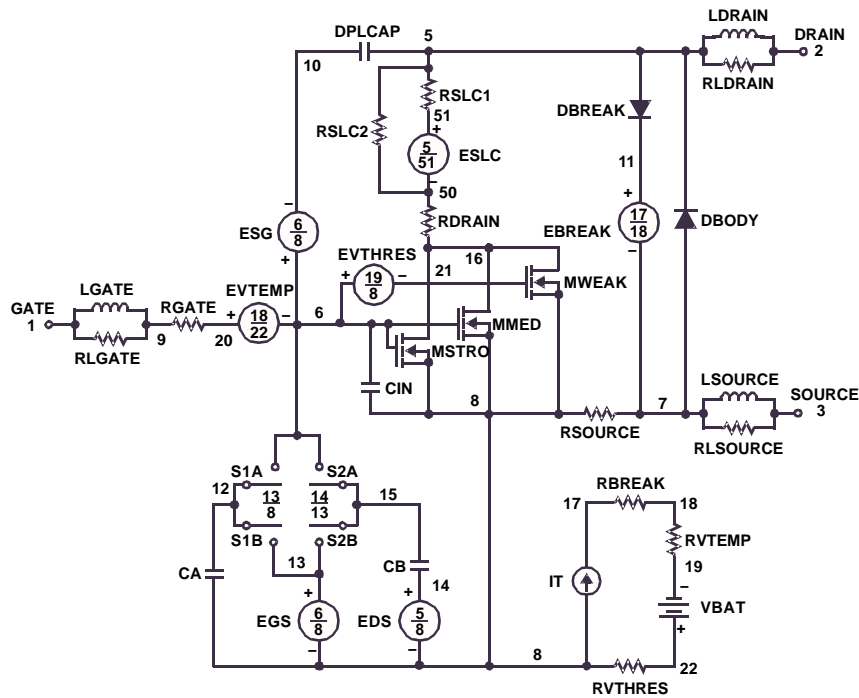
.MODEL DbodyMOD D (IS=2.4E-11 N=1.08 RS=4.2e-3 TRS1=2.2e-3 TRS2=2.5e-9  
 + CJO=1.35e-9 M=6.3e-1 TT=4.8e-8 XT1=3.9)  
 .MODEL DbreakMOD D (RS=1.5e-1 TRS1=1e-3 TRS2=-8.9e-6)  
 .MODEL DplcapMOD D (CJO=.43e-9 IS=1e-30 N=10 M=0.66)

.MODEL MmedMOD NMOS (VTO=3.5 KP=4 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=9.3e-1)  
 .MODEL MstroMOD NMOS (VTO=4.0 KP=70 IS=1e-30 N=10 TOX=1 L=1u W=1u)  
 .MODEL MweakMOD NMOS (VTO=3.12 KP=0.06 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=9.3e-1 RS=.1)

.MODEL RbreakMOD RES (TC1=1e-3 TC2=-15e-7)  
 .MODEL RdrainMOD RES (TC1=1.7e-2 TC2=4e-5)  
 .MODEL RSLCMOD RES (TC1=2.5e-3 TC2=1e-6)  
 .MODEL RsourceMOD RES (TC1=1e-3 TC2=1e-6)  
 .MODEL RvthresMOD RES (TC1=-5.3e-3 TC2=-1.5e-5)  
 .MODEL RvtempMOD RES (TC1=-2.7e-3 TC2=1e-6)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4 VOFF=-1.5)  
 .MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.5 VOFF=-4)  
 .MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1 VOFF=0.5)  
 .MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.5 VOFF=-1)  
 .ENDS

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



# FDP42AN15A0

## SABER Electrical Model

rev June 11, 2002

template FDP42AN15A0 n2,n1,n3

electrical n2,n1,n3

{

var i iscl

dp..model dbodymod = (isl=2.4e-11,nl=1.08,rs=4.2e-3,trs1=2.2e-3,trs2=2.5e-9,cjo=1.35e-9,m=6.3e-1,tt=4.8e-8,xti=3.9)

dp..model dbreakmod = (rs=1.5e-1,trs1=1e-3,trs2=-8.9e-6)

dp..model dplcapmod = (cjo=.43e-9,isl=10e-30,nl=10,m=0.66)

m..model mmedmod = (type=\_n,vto=3.5,kp=4,is=1e-30,tox=1)

m..model mstrongmod = (type=\_n,vto=4.0,kp=70,is=1e-30,tox=1)

m..model mweakmod = (type=\_n,vto=3.12,kp=0.06,is=1e-30,tox=1,rs=.1)

sw\_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-4,voff=-1.5)

sw\_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-1.5,voff=-4)

sw\_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-1,voff=0.5)

sw\_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=0.5,voff=-1)

c.ca n12 n8 = 6.0e-10

c.cb n15 n14 = 8e-10

c.cin n6 n8 = 2.1e-9

dp.dbody n7 n5 = model=dbodymod

dp.dbreak n5 n11 = model=dbreakmod

dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 159.5

spe.eds n14 n8 n5 n8 = 1

spe.egs n13 n8 n6 n8 = 1

spe.esg n6 n10 n6 n8 = 1

spe.evthres n6 n21 n19 n8 = 1

spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

l.lgate n1 n9 = 4.81e-9

l.ldrain n2 n5 = 1.0e-9

l.lsource n3 n7 = 4.63e-9

res.rlgate n1 n9 = 48.1

res.rldrain n2 n5 = 10

res.rlsource n3 n7 = 46.3

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u

m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u

m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1=1e-3,tc2=-15e-7

res.rdrain n50 n16 = 14e-3, tc1=1.7e-2,tc2=4e-5

res.rgate n9 n20 = 1.36

res.rslc1 n5 n51 = 1e-6, tc1=2.5e-3,tc2=1e-6

res.rslc2 n5 n50 = 1e3

res.rsource n8 n7 = 20e-3, tc1=1e-3,tc2=1e-6

res.rvthres n22 n8 = 1, tc1=-5.3e-3,tc2=-1.5e-5

res.rvtemp n18 n19 = 1, tc1=-2.7e-3,tc2=1e-6

sw\_vcsp.s1a n6 n12 n13 n8 = model=s1amod

sw\_vcsp.s1b n13 n12 n13 n8 = model=s1bmod

sw\_vcsp.s2a n6 n15 n14 n13 = model=s2amod

sw\_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

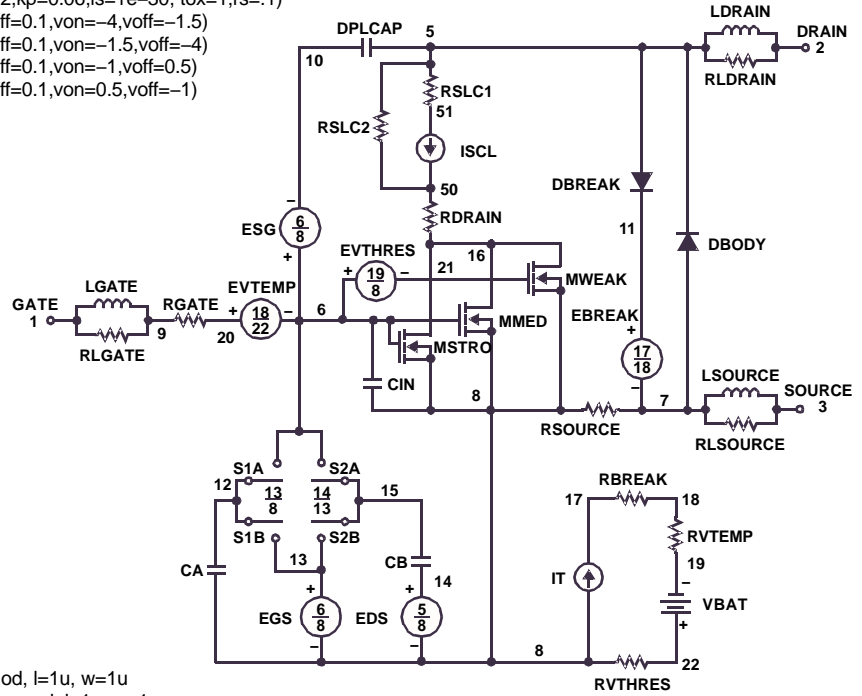
v.vbat n22 n19 = dc=1

equations {

i (n51->n50) +=iscl

iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))\*((abs(v(n5,n51))\*1e6/65)\*\* 3)))

}





**SPICE Thermal Model**

REV 23 June 11, 2002

FDB42AN15A0\_Thermal

CTHERM1 TH 6 2e-3  
 CHERM2 6 5 4.5e-3  
 CHERM3 5 4 7e-3  
 CHERM4 4 3 3e-2  
 CHERM5 3 2 4e-2  
 CHERM6 2 TL 8.5e-1

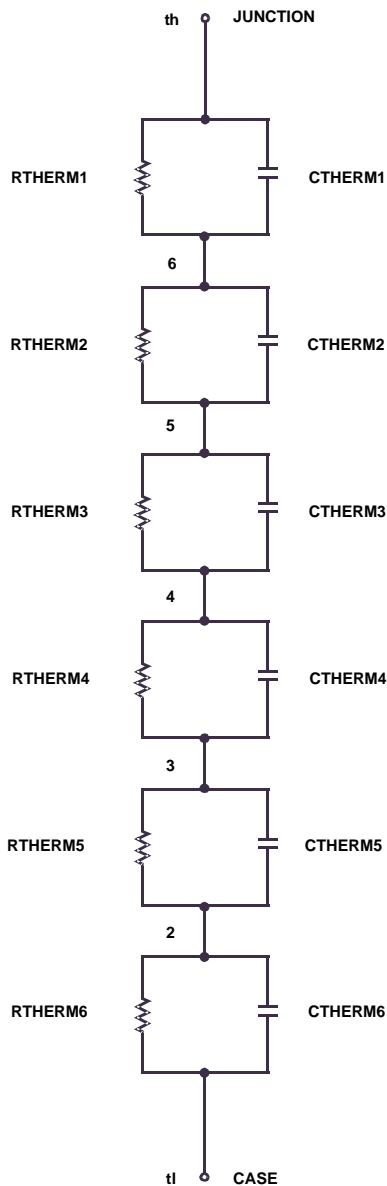
RHERM1 TH 6 6.2e-2  
 RHERM2 6 5 8.2e-2  
 RHERM3 5 4 9.2e-2  
 RHERM4 4 3 9.7e-2  
 RHERM5 3 2 0.2  
 RHERM6 2 TL 0.22

**SABER Thermal Model**

SABER thermal model FDB42AN15A0\_Thermal  
 template thermal\_model th tl  
 thermal\_c th, tl

```
{
    ctherm.ctherm1 th 6 =2e-3
    ctherm.ctherm2 6 5 =4.5e-3
    ctherm.ctherm3 5 4 =7e-3
    ctherm.ctherm4 4 3 =3e-2
    ctherm.ctherm5 3 2 =4e-2
    ctherm.ctherm6 2 tl =8.5e-1
```

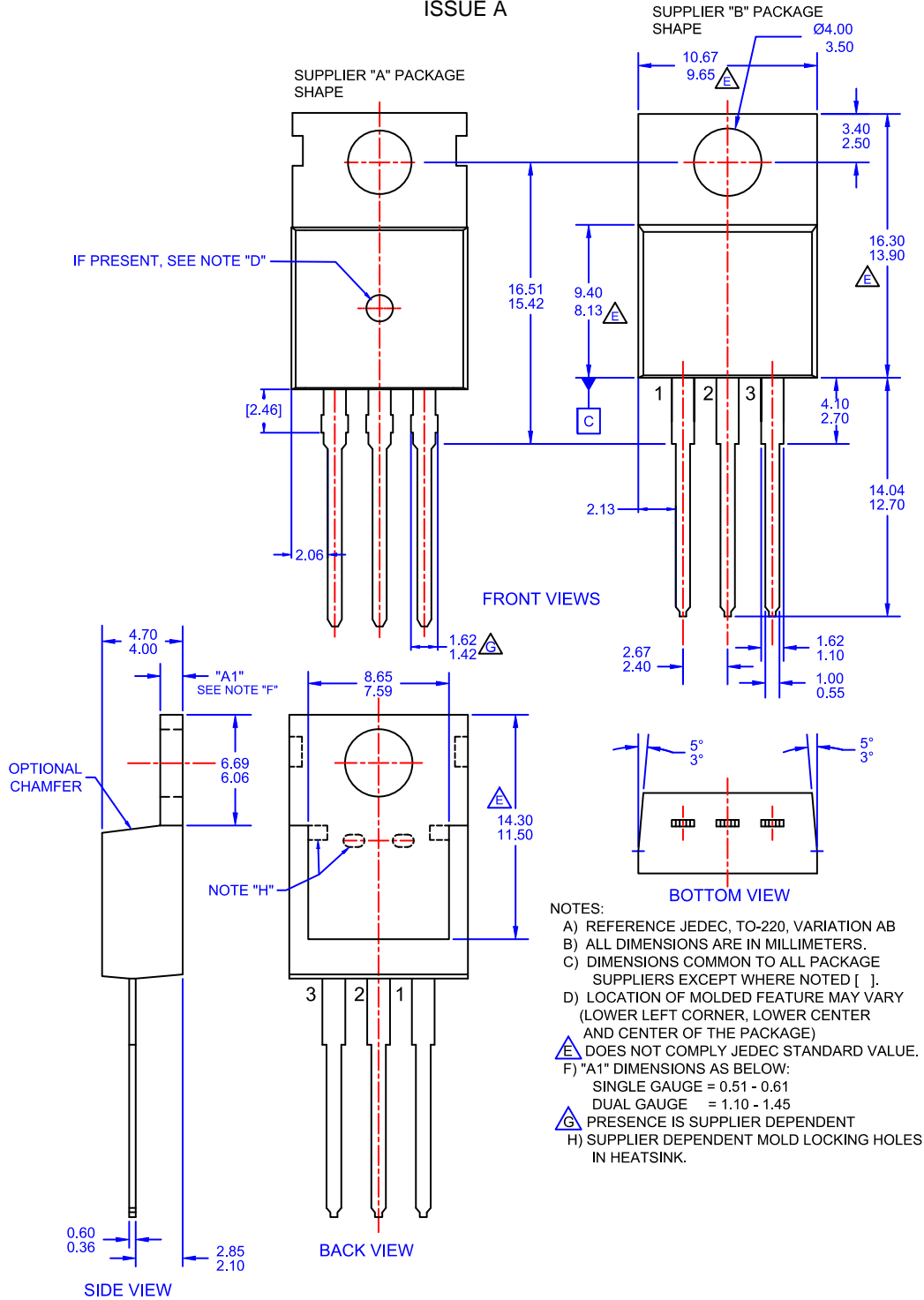
```
rtherm.rtherm1 th 6 =6.2e-2
rtherm.rtherm2 6 5 =8.2e-2
rtherm.rtherm3 5 4 =9.2e-2
rtherm.rtherm4 4 3 =9.7e-2
rtherm.rtherm5 3 2 =0.2
rtherm.rtherm6 2 tl =0.22}
```




# FDP42AN15A0

## PACKAGE DIMENSIONS

TO-220-3LD  
CASE 340AT  
ISSUE A



PowerTrench is a registered trademark of Semiconductor Components Industries, LLC (SCILLC)

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative