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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

March 2015

FDS8672S

N-Channel PowerTrench® SyncFET™

30V, 18A, 4.8mΩ

Features

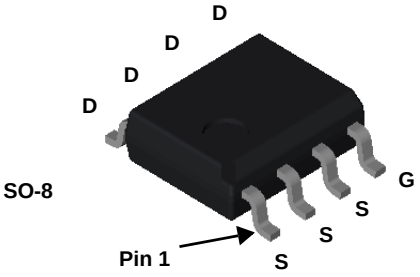
- Max $r_{DS(on)}$ = 4.8mΩ at V_{GS} = 10V, I_D = 18A
- Max $r_{DS(on)}$ = 7.0mΩ at V_{GS} = 4.5V, I_D = 15A
- Includes SyncFET Schottky Body Diode
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$ and Fast Switching
- High Power and Current Handling Capability
- 100% R_g (Gate Resistance) Tested
- Termination is Lead-free and RoHS Compliant

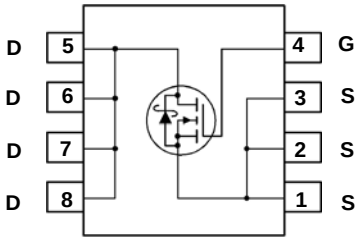
General Description

The FDS8672S is designed to replace a single MOSFET and Schottky diode in synchronous DC/DC power supplies. This 30V MOSFET is designed to maximize power conversion efficiency, providing a low $r_{DS(on)}$ and low gate charge. The FDS8672S includes a patented combination of a MOSFET monolithically integrated with a Schottky diode using Fairchild's monolithic SyncFET technology.

Applications

- Synchronous Rectifier for DC/DC Converters
- Notebook Vcore Low Side Switch
- Point of Load Low Side Switch





MOSFET Maximum Ratings T_A = 25°C unless otherwise noted.

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			30	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous			18	A
	-Pulsed		(Note 4)	80	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	216	mJ
P_D	Power Dissipation	T_A = 25°C	(Note 1a)	2.5	W
	Power Dissipation	T_A = 25°C	(Note 1b)	1.0	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	25	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS8672S	FDS8672S	SO8	13"	12mm	2500 units

Electrical Characteristics T_J = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 1mA, V_{GS} = 0V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 10mA, referenced to 25°C		33		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24V, V_{GS} = 0V			500	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 1mA	1.0	2.1	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 10mA, referenced to 25°C		-5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 18A		3.8	4.8	mΩ
		V_{GS} = 4.5V, I_D = 15A		5.3	7.0	
		V_{GS} = 10V, I_D = 18A, T_J = 125°C		5.3	7.8	
g_{FS}	Forward Transconductance	V_{DS} = 5V, I_D = 18A		78		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz		2005	2670	pF
C_{oss}	Output Capacitance			985	1310	pF
C_{rss}	Reverse Transfer Capacitance			135	205	pF
R_g	Gate Resistance	f = 1MHz		0.6	2.0	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15V, I_D = 18A, V_{GS} = 10V, R_{GEN} = 6Ω		12	22	ns
t_r	Rise Time			4	10	ns
$t_{d(off)}$	Turn-Off Delay Time			26	42	ns
t_f	Fall Time			3	10	ns
Q_g	Total Gate Charge	V_{GS} = 0V to 10V; V_{DD} = 15V, I_D = 18A		29	41	nC
Q_g	Total Gate Charge	V_{GS} = 0V to 5V; V_{DD} = 15V, I_D = 18A		15	21	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 15V, I_D = 18A		5.5		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 15V, I_D = 18A		3.7		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 18A		0.8	1.2	V
		V_{GS} = 0V, I_S = 1.8A		0.4	0.7	
t_{rr}	Reverse Recovery Time	I_F = 18A, di/dt = 300A/μs		27	43	ns
Q_{rr}	Reverse Recovery Charge			31	50	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 50°C/W when mounted on a 1in^2 pad of 2 oz copper.

b) 125°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.
3. Starting T_J = 25°C, L = 3mH, I_{AS} = 12A, V_{DD} = 30V, V_{GS} = 10V.
4. Pulse current was measured at 250uS pulse, refer to Fig 11 Forward Safe Operation Area for detail.

Typical Characteristics T_J = 25°C unless otherwise noted.

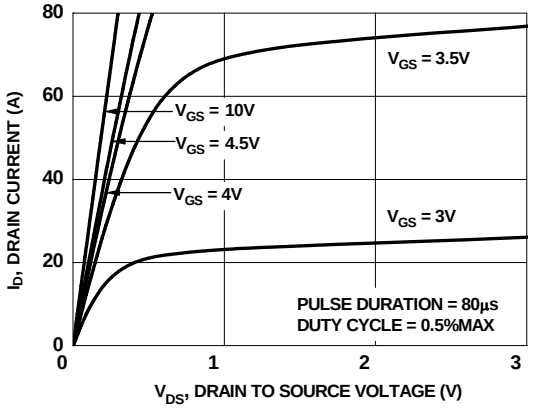


Figure 1. On-Region Characteristics

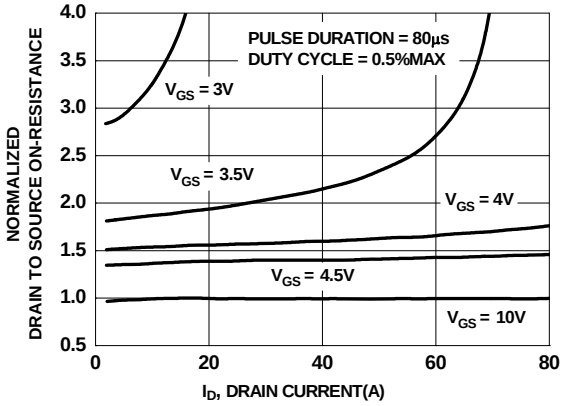


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

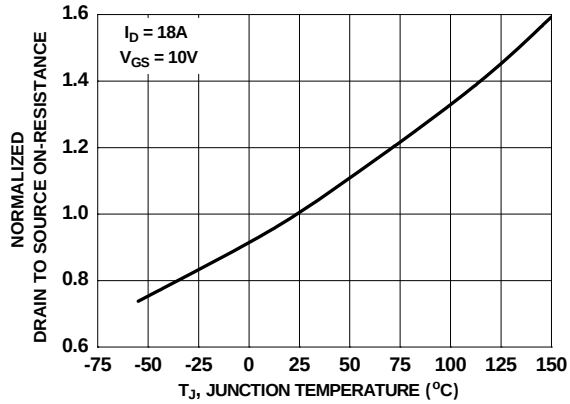


Figure 3. Normalized On-Resistance vs. Junction Temperature

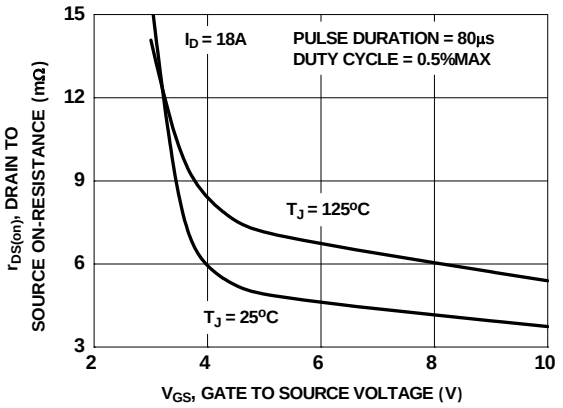


Figure 4. On-Resistance vs. Gate to Source Voltage

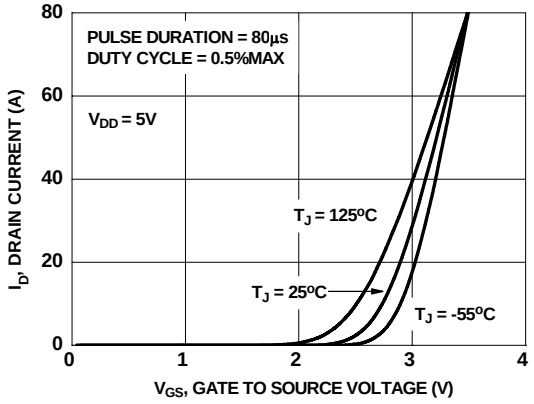


Figure 5. Transfer Characteristics

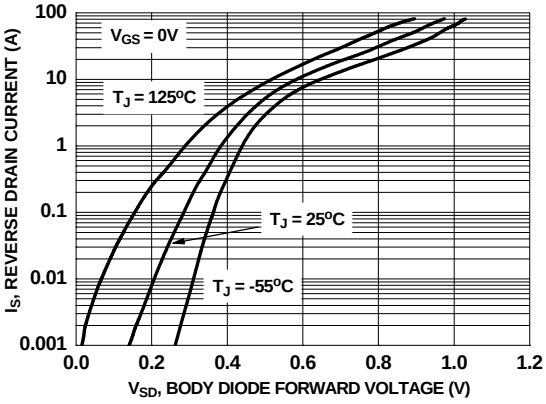


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics T_J = 25°C unless otherwise noted.

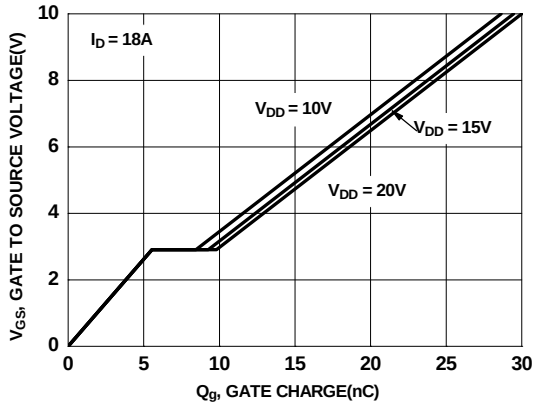


Figure 7. Gate Charge Characteristics

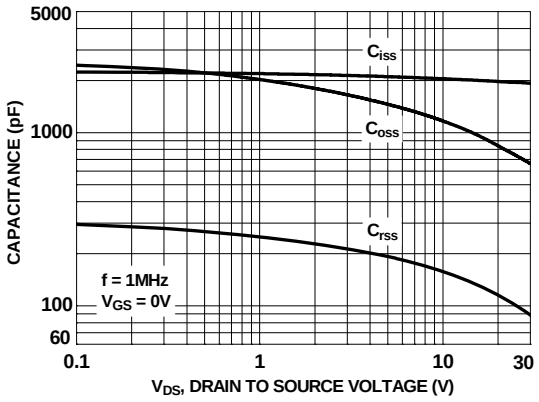


Figure 8. Capacitance vs. Drain to Source Voltage

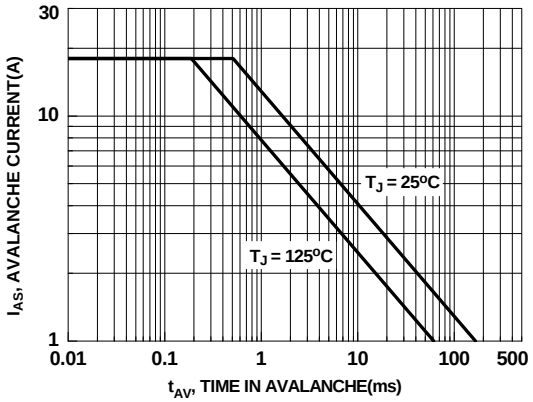


Figure 9. Unclamped Inductive Switching Capability

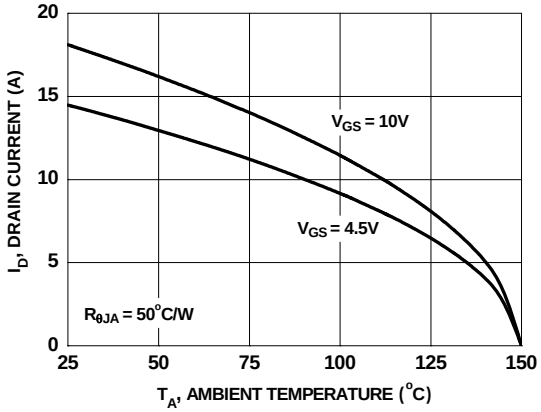


Figure 10. Maximum Continuous Drain Current vs. Ambient Temperature

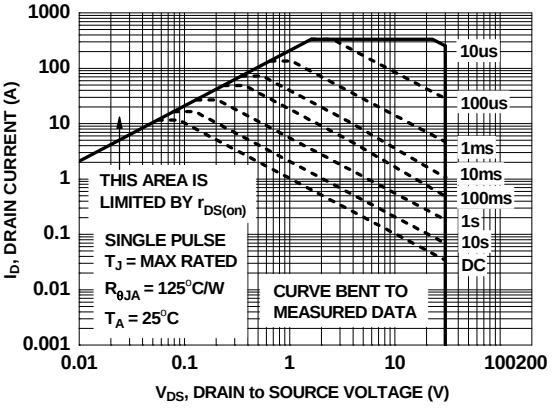


Figure 11. Forward Bias Safe Operating Area

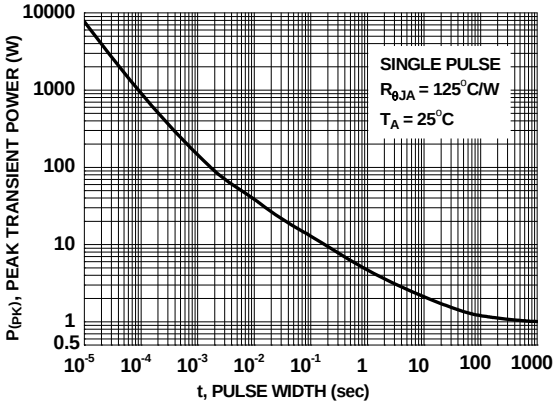


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted.

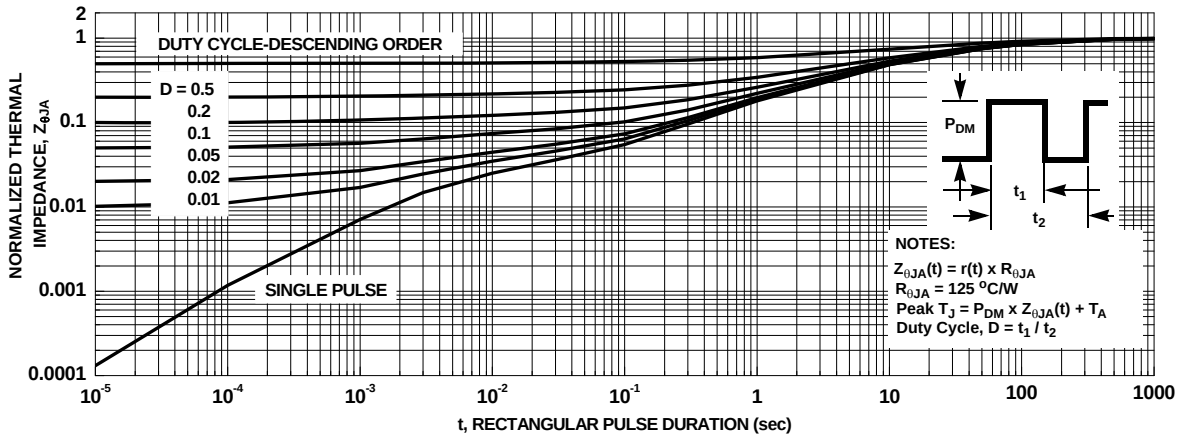
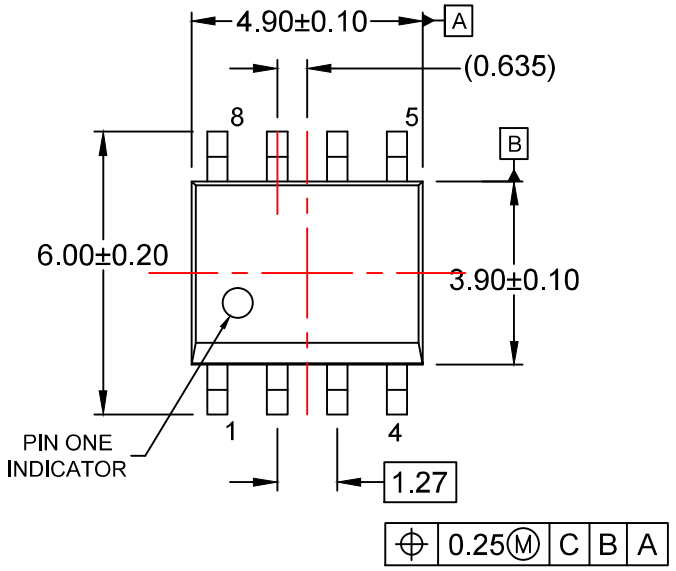
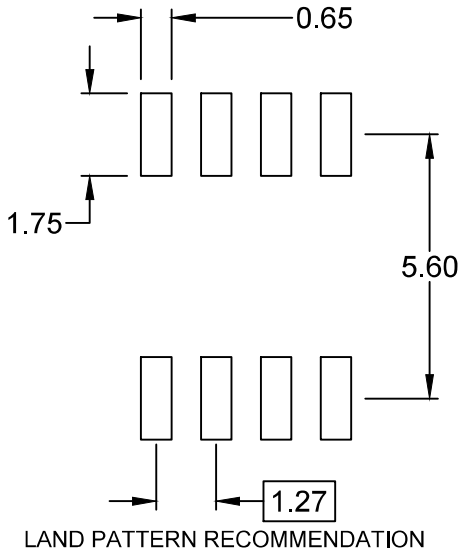
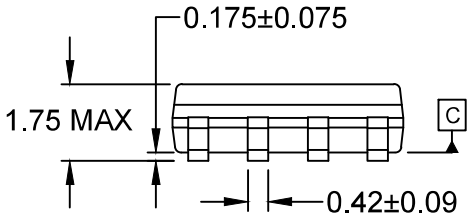


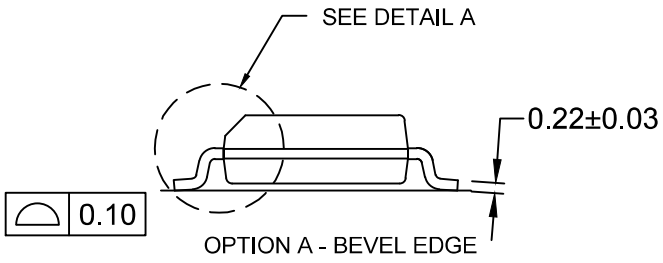
Figure 13. Junction-to-Ambient Transient Thermal Response Curve



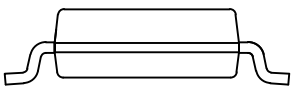


LAND PATTERN RECOMMENDATION

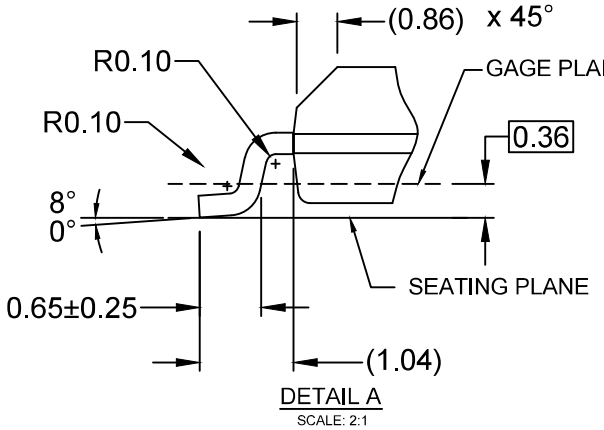




OPTION A - BEVEL EDGE



OPTION B - NO BEVEL EDGE



DETAIL A
SCALE: 2:1

NOTES:

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M
E) DRAWING FILENAME: M08Arev16

FAIRCHILD.

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