



FDWS9509L-F085 (Note1)

P-Channel Logic Level Power Trench® MOSFET

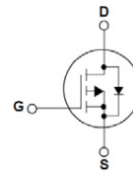
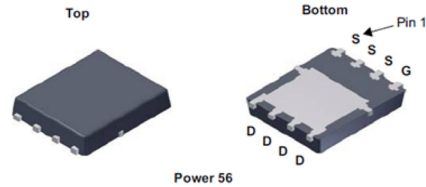
- 40 V, - 65 A, 8.0 mΩ

Features

- Typical $R_{DS(on)}$ = 6.3 mΩ at $V_{GS} = -10V$, $I_D = -65 A$
- Typical $Q_{g(tot)}$ = 48 nC at $V_{GS} = -10V$, $I_D = -65 A$
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101
- Wettable flanks for automatic optical inspection (AOI)

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Electronic Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12V Systems



MOSFET Maximum Ratings $T_J = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-to-Source Voltage	-40	V
V_{GS}	Gate-to-Source Voltage	± 16	V
I_D	Drain Current - Continuous ($V_{GS}=10$) (Note 2)	$T_C = 25^\circ C$	A
	Pulsed Drain Current	$T_C = 25^\circ C$	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	84	mJ
P_D	Power Dissipation	107	W
	Derate Above $25^\circ C$	0.71	W/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature	-55 to + 175	$^\circ C$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.4	$^\circ C/W$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 4)	50	$^\circ C/W$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDWS9509L	FDWS9509L-F085	Power 56	13"	12mm	3000 units

Notes:

- 1: Due to system integration constraints between Fairchild and ON semiconductor, as of November 1, 2017 any product part number with a underscore will be replaced with a dash. This is a notification.
- 2: Current is limited by bondwire configuration.
- 3: Starting $T_J = 25^\circ C$, $L = 50\mu H$, $I_{AS} = 56A$, $V_{DD} = -40V$ during inductor charging and $V_{DD} = 0V$ during time in avalanche.
- 4: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

B_{VDSS}	Drain-to-Source Breakdown Voltage	$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	-40	-	-	V
I_{DSS}	Drain-to-Source Leakage Current	$V_{DS} = -40\text{V}, T_J = 25^\circ\text{C}$	-	-	1	μA
		$V_{GS} = 0\text{V}, T_J = 175^\circ\text{C}$ (Note 5)	-	-	1	mA
I_{GSS}	Gate-to-Source Leakage Current	$V_{GS} = \pm 16\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	-1	-1.7	-3	V
$R_{DS(on)}$	Drain to Source On Resistance	$I_D = -65\text{A}, V_{GS} = -4.5\text{V}$	-	10.7	15.3	
		$I_D = -65\text{A}, T_J = 25^\circ\text{C}$	-	6.3	8.0	$\text{m}\Omega$
		$V_{GS} = -10\text{V}, T_J = 175^\circ\text{C}$ (Note 5)	-	10.6	13.0	$\text{m}\Omega$

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$	-	3360	-	pF
C_{oss}	Output Capacitance		-	1230	-	pF
C_{rss}	Reverse Transfer Capacitance		-	38	-	pF
R_g	Gate Resistance	$V_{GS} = 0.5\text{V}, f = 1\text{MHz}$	-	21	-	Ω
$Q_{g(ToT)}$	Total Gate Charge	$V_{GS} = 0 \text{ to } -10\text{V}$	-	48	67	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0 \text{ to } -2\text{V}$				
Q_{gs}	Gate-to-Source Gate Charge	$V_{DD} = -20\text{V}$ $I_D = -65\text{A}$	-	12	-	nC
Q_{gd}	Gate-to-Drain "Miller" Charge		-	6	-	nC

Switching Characteristics

t_{on}	Turn-On Time	$V_{DD} = -20\text{V}, I_D = -65\text{A},$ $V_{GS} = -10\text{V}, R_{GEN} = 6\Omega$	-	-	22	ns
$t_{d(on)}$	Turn-On Delay		-	10	-	ns
t_r	Rise Time		-	5	-	ns
$t_{d(off)}$	Turn-Off Delay		-	198	-	ns
t_f	Fall Time		-	71	-	ns
t_{off}	Turn-Off Time		-	-	405	ns

Drain-Source Diode Characteristics

V_{SD}	Source-to-Drain Diode Voltage	$I_{SD} = -65\text{A}, V_{GS} = 0\text{V}$	-	1.0	-1.25	V
		$I_{SD} = -32.5\text{A}, V_{GS} = 0\text{V}$	-	0.9	-1.2	V
t_{rr}	Reverse-Recovery Time	$I_F = -65\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	57	80	ns
Q_{rr}	Reverse-Recovery Charge		-	45	67	nC

Note:

5: The maximum value is specified by design at $T_J = 175^\circ\text{C}$. Product is not tested to this condition in production.

Typical Characteristics

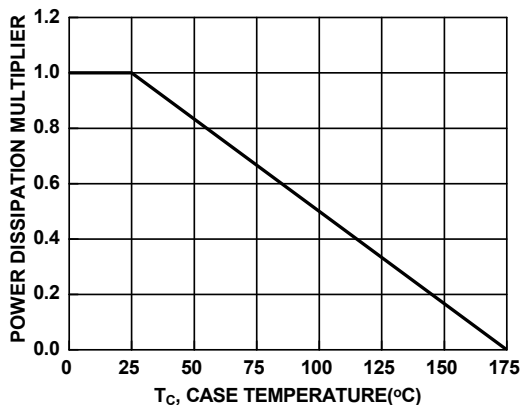


Figure 1. Normalized Power Dissipation vs. Case Temperature

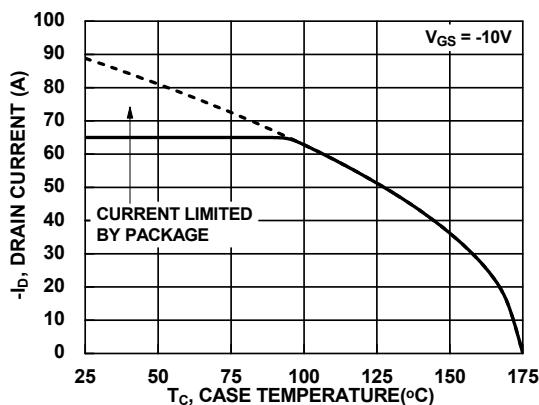


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

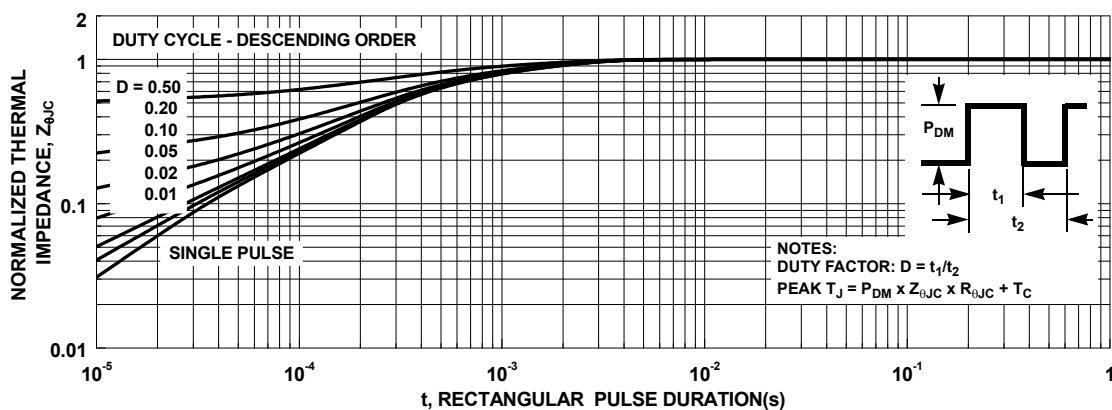


Figure 3. Normalized Maximum Transient Thermal Impedance

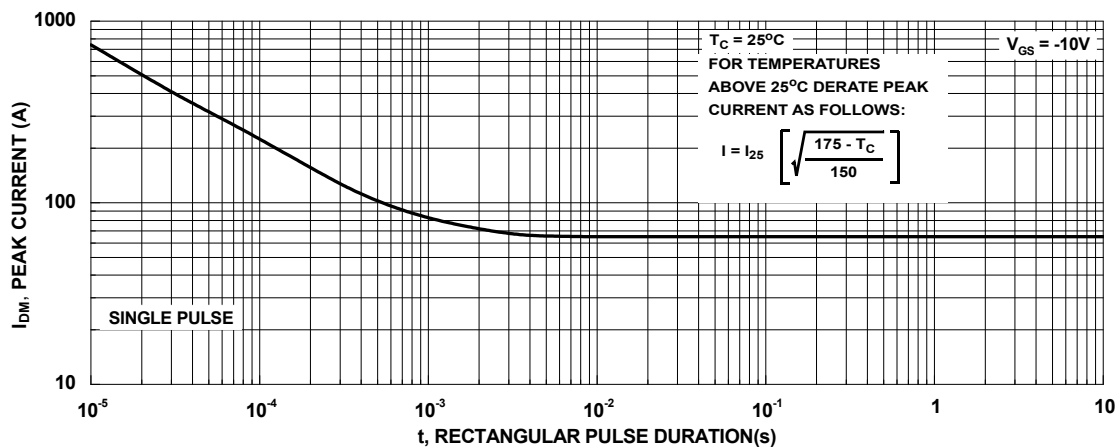


Figure 4. Peak Current Capability

Typical Characteristics

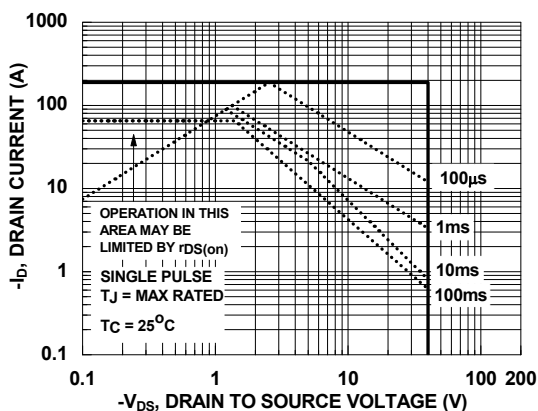
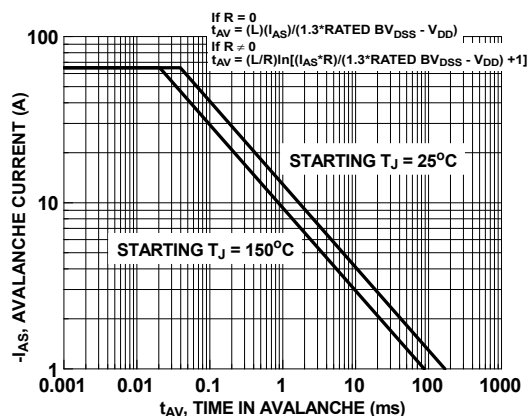


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to ONsemi Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

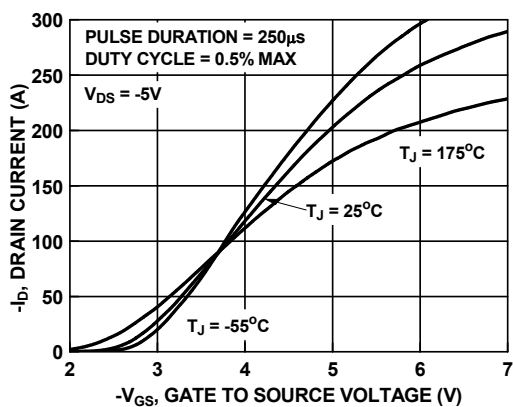


Figure 7. Transfer Characteristics

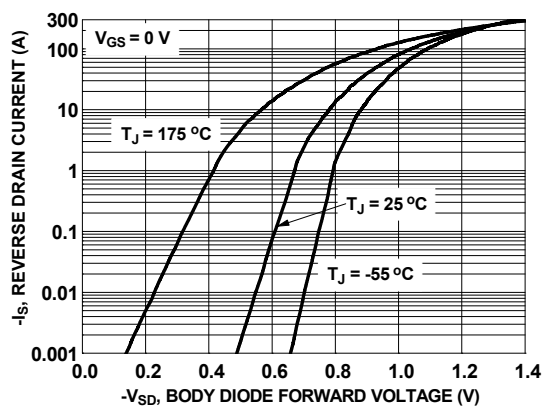


Figure 8. Forward Diode Characteristics

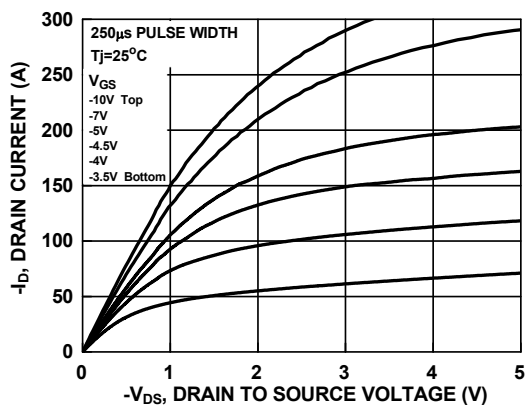


Figure 9. Saturation Characteristics

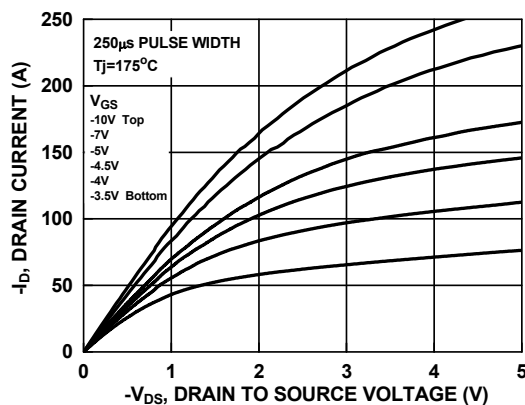


Figure 10. Saturation Characteristics

Typical Characteristics

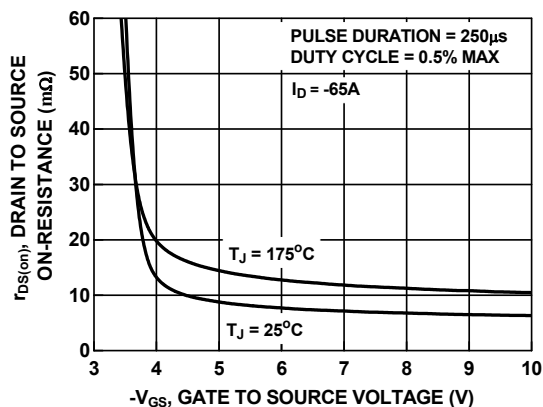


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

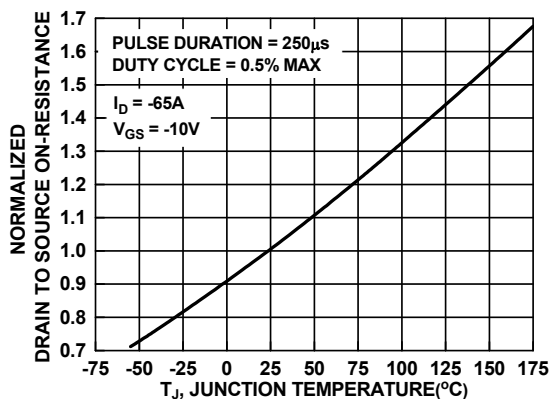


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

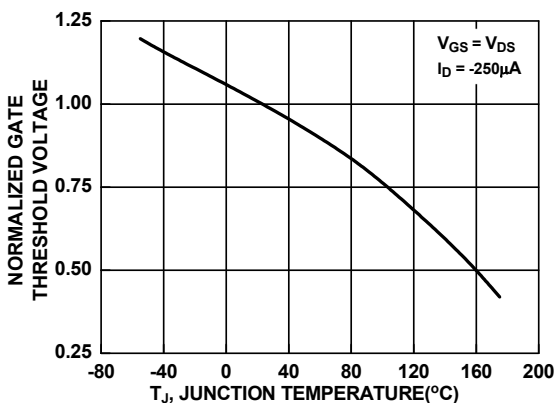


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

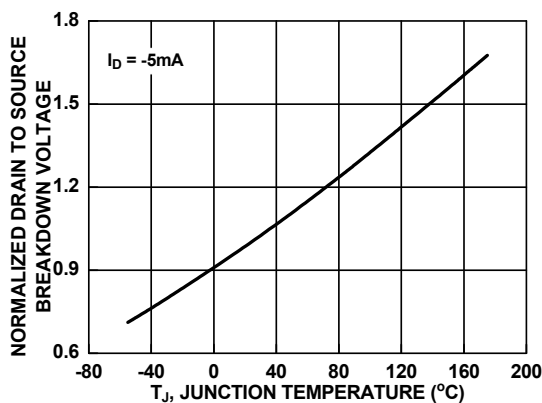


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

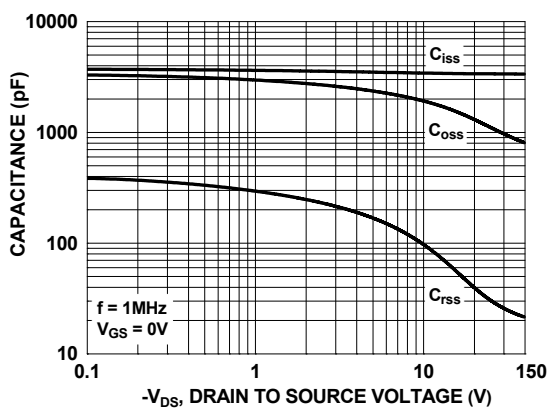


Figure 15. Capacitance vs. Drain to Source Voltage

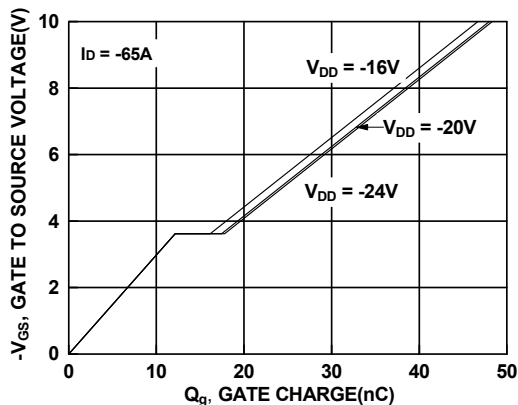
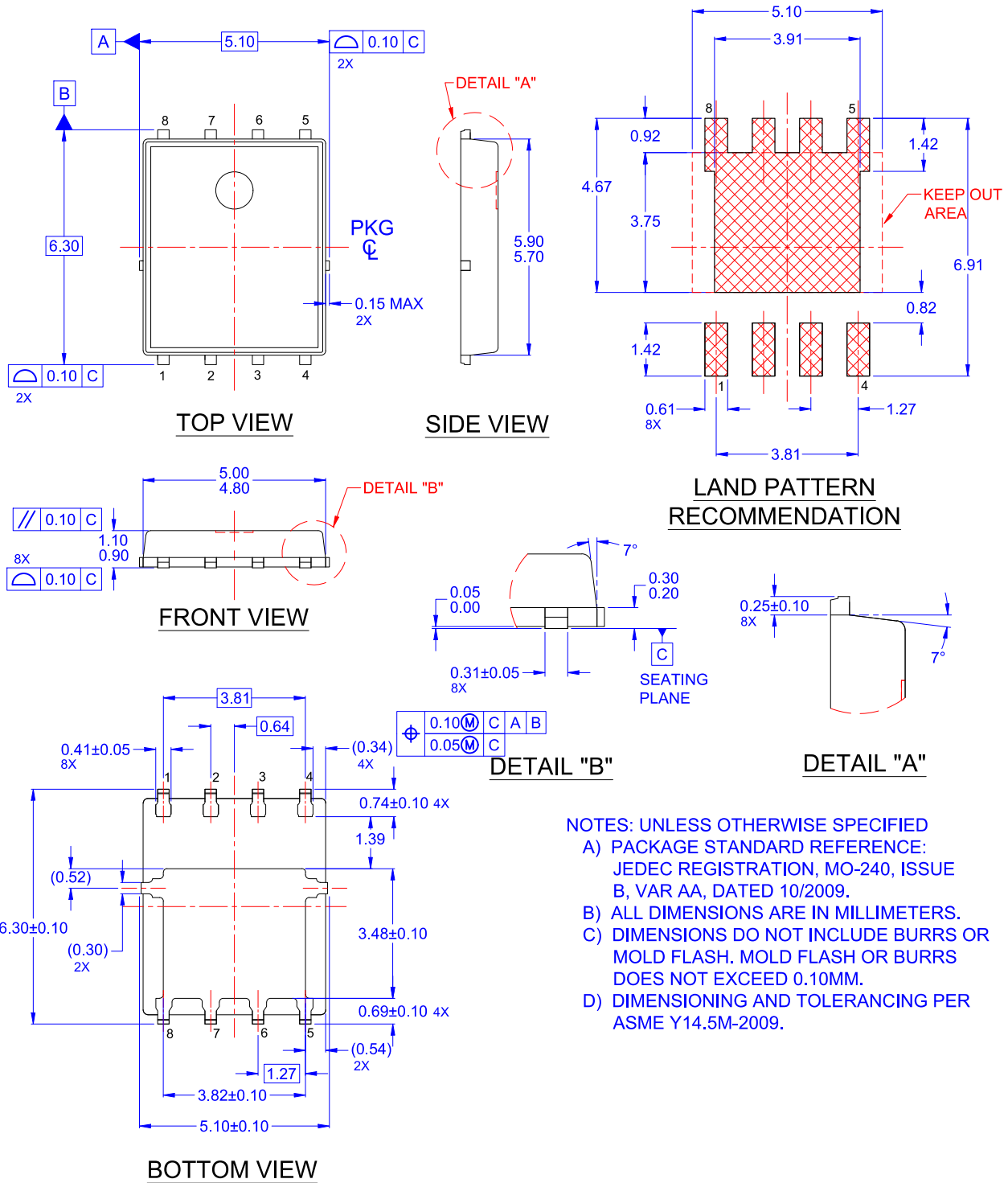



Figure 16. Gate Charge vs. Gate to Source Voltage

DFN8 5.1x6.3, 1.27P
CASE 506DW
ISSUE O



- NOTES:** UNLESS OTHERWISE SPECIFIED
- A) PACKAGE STANDARD REFERENCE: JEDEC REGISTRATION, MO-240, ISSUE B, VAR AA, DATED 10/2009.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
 - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

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