FPF2G75FH07BP

Product Preview

F2, HERIC Module with PCM and NTC

The FPF2G75FH07BP is the HERIC topology which is providing a high efficiency solution for the solar application. And the integrated high speed field stop IGBTs are providing lower conduction and switching losses. And the pre−applied PCM requires no additional process of the thermal interface material printing. Furthermore, the screw clamp provides a fast and reliable mounting method.

Electrical Features

- High Efficiency
- Low Conduction and Switching Losses
- High Speed Field Stop IGBT
- Built−in NTC for Temperature Monitoring
- This is a Pb−Free Device

Mechanical Features

- Compact Size: F2 Package
- Soldering Pin
- Al_2O_3 Substrate with Low Thermal Resistance
- Pre−applied PCM (Phase Change Material)

Applications

- Solar Inverter

Related Materials

- AN−5077: Design Considerations for High Power Module (HPM)
- AN−4186: F1 and F2 Modules with Pre−applied Phase Change Material (PCM)

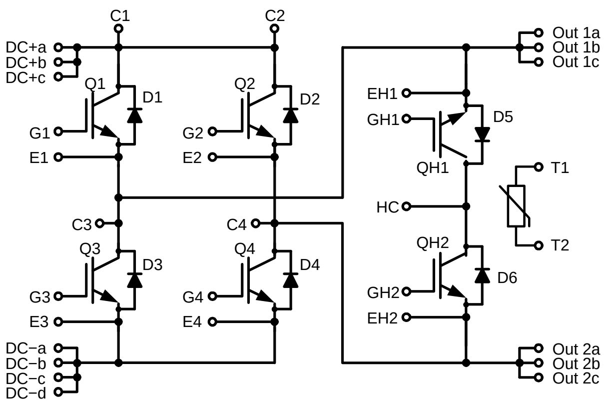

Figure 1. Internal Circuit Diagram

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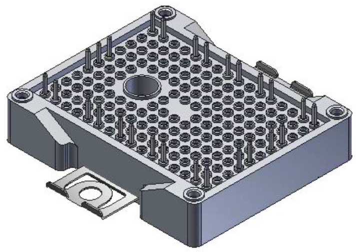


CODE: F2
CASE MODFS

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	PCM	Packing Type	Quantity / Tray
FPF2G75FH07BP	FPF2G75FH07BP	F2	O	Tray	14

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Description	Condition	Rating	Units
IGBT				
V_{CES}	Collector−Emitter Voltage		650	V
V_{GES}	Gate−Emitter Voltage		±25	V
I_C	Continuous Collector Current	T_C = 80°C, T_{Jmax} = 175°C	75	A
I_{CM}	Pulsed Collector Current	limited by T_{Jmax}	150	A
P_D	Maximum Power Dissipation		236	W
T_J	Operating Junction Temperature		−40 to +150	°C
FULL−BRIDGE DIODE (D1, D2, D3, D4)				
V_{RRM}	Peak Repetitive Reverse Voltage		650	V
I_F	Continuous Forward Current	T_C = 80°C, T_{Jmax} = 175°C	50	A
I_{FM}	Maximum Forward Current		100	A
P_D	Maximum Power Dissipation		208	W
T_J	Operating Junction Temperature		−40 to +150	°C
HERIC DIODE (D5, D6)				
V_{RRM}	Peak Repetitive Reverse Voltage		650	V
I_F	Continuous Forward Current	T_C = 80°C, T_{Jmax} = 175°C	75	A
I_{FM}	Maximum Forward Current		150	A
P_D	Maximum Power Dissipation		272	W
T_J	Operating Junction Temperature		−40 to +150	°C
MODULE				
T_{STG}	Storage Temperature (Note 1)		−40 to +125	°C
V_{ISO}	Isolation Voltage	AC 1 min.	2500	V
Iso._Material	Internal Isolation Material		Al_2O_3	−
T_{MOUNT}	Mounting Torque (Note 2)	M4	2.4	N•m
Creepage	Terminal to Heat Sink		11.5	mm
	Terminal to Terminal		6.3	mm
Clearance	Terminal to Heat Sink		10.0	mm
	Terminal to Terminal		5.0	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. In the case of PCM pre−applied module, please refer to the application note (AN−4186)
2. Recommendable value : 2.0 ~ 2.4 Nm (M4)

ELECTRICAL CHARACTERISTICS T_C = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
IGBT OFF CHARACTERISTICS						
BV_{CES}	Collector−Emitter Breakdown Voltage	V_{GE} = 0 V, I_C = 1 mA	650	−	−	V
I_{CES}	Collector Cut−off Current	V_{CE} = V_{CES}, V_{GE} = 0 V	−	−	250	μA
I_{GES}	Gate−Emitter Leakage Current	V_{GE} = V_{GES}, V_{CE} = 0 V	−	−	±2	μA
ON CHARACTERISTICS						
$V_{GE(th)}$	Gate−Emitter Threshold Voltage	V_{GE} = V_{CE}, I_C = 75 mA	4.2	5.4	6.8	V
$V_{CE(sat)}$	Collector−Emitter Saturation Voltage	I_C = 75 A, V_{GE} = 15 V	−	1.58	2.2	V
		I_C = 75 A, V_{GE} = 15 V, T_C = 125°C	−	1.85	−	V
R_{LEAD}	Lead Resistance of Pin to Chip	per Chip	−	3.3	−	mΩ
SWITCHING CHARACTERISTICS (Q3−D5 / Q4−D6)						
$t_{d(on)}$	Turn−On Delay Time	V_{CC} = 300 V I_C = 75 A V_{GE} = 15 V R_G = 30 Ω Inductive Load T_C = 25°C	−	75	−	ns
t_r	Rise Time		−	54	−	ns
$t_{d(off)}$	Turn−Off Delay Time		−	380	−	ns
t_f	Fall Time		−	52	−	ns
E_{ON}	Turn−On Switching Loss per Pulse		−	0.93	−	mJ
E_{OFF}	Turn−Off Switching Loss per Pulse		−	1.26	−	mJ
$t_{d(on)}$	Turn−On Delay Time	V_{CC} = 300 V I_C = 75 A V_{GE} = 15 V R_G = 30 Ω Inductive Load T_C = 125°C	−	65	−	ns
t_r	Rise Time		−	59	−	ns
$t_{d(off)}$	Turn−Off Delay Time		−	410	−	ns
t_f	Fall Time		−	52	−	ns
E_{ON}	Turn−On Switching Loss per Pulse		−	1.66	−	mJ
E_{OFF}	Turn−Off Switching Loss per Pulse		−	1.53	−	mJ
Q_g	Total Gate Charge	V_{CC} = 300 V, I_C = 75 A, V_{GE} = 0 ~ 15 V	−	123	−	nC
$R_{\theta JC}$	Thermal Resistance of Junction to Case	per Chip	−	−	0.63	°C/W
$R_{\theta CH}$	Thermal Resistance of Case to Heat sink	per Chip, λ_{PCM} = 3.4 W/mK	−	0.49	−	°C/W
FULL−BRIDGE DIODE (D1, D2, D3, D4)						
V_F	Diode Forward Voltage	I_F = 50 A	−	2.03	2.8	V
		I_F = 50 A, T_C = 125°C	−	1.7	−	V
R_{LEAD}	Lead Resistance of Pin to Chip	per Chip	−	3.4	−	mΩ
I_R	Reverse Leakage Current	V_R = 650 V	−	−	250	μA
I_{rr}	Reverse Recovery Current	V_R = 300 V, I_F = 50 A di / dt = 1300 A/μs T_C = 25°C	−	28	−	A
Q_{rr}	Reverse Recovery Charge		−	0.5	−	μC
E_{rec}	Reverse Recovery Energy		−	51	−	μJ
I_{rr}	Reverse Recovery Current	V_R = 300 V, I_F = 50 A di / dt = 1300 A/μs T_C = 125°C	−	40	−	A
Q_{rr}	Reverse Recovery Charge		−	1.2	−	μC
E_{rec}	Reverse Recovery Energy		−	145	−	μJ
$R_{\theta JC}$	Thermal Resistance of Junction to Case	per Chip	−	−	0.72	°C/W
$R_{\theta CH}$	Thermal Resistance of Case to Heat sink	per Chip, λ_{PCM} = 3.4 W/mK	−	0.38	−	°C/W
HERIC DIODE (D5, D6)						
V_F	Diode Forward Voltage	I_F = 75 A	−	2.28	2.9	V
		I_F = 75 A, T_C = 125°C	−	1.74	−	V
R_{LEAD}	Lead Resistance of Pin to Chip	per Chip	−	1.1	−	mΩ
I_R	Reverse Leakage Current	V_R = 650 V	−	−	250	μA

ELECTRICAL CHARACTERISTICS T_C = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
HERIC DIODE (D5, D6)						
I_{rr}	Reverse Recovery Current	V_R = 300 V, I_F = 75 A di / dt = 1220 A/μs T_C = 25°C	−	32	−	A
Q_{rr}	Reverse Recovery Charge		−	0.79	−	μC
E_{rec}	Reverse Recovery Energy		−	113	−	μJ
I_{rr}	Reverse Recovery Current	V_R = 300 V, I_F = 75 A di / dt = 1220 A/μs T_C = 125°C	−	52	−	A
Q_{rr}	Reverse Recovery Charge		−	1.9	−	μC
E_{rec}	Reverse Recovery Energy		−	288	−	μJ
$R_{\theta JC}$	Thermal Resistance of Junction to Case	per Chip	−	−	0.55	°C/W
$R_{\theta CH}$	Thermal Resistance of Case to Heat sink	per Chip, λ_{PCM} = 3.4 W/mK	−	0.39	−	°C/W
NTC (Thermistor)						
R_{NTC}	Rated Resistance	T_C = 25°C	−	10	−	kΩ
		T_C = 100°C	−	936	−	Ω
	Tolerance	T_C = 25°C	−3	−	+3	%
P_D	Power Dissipation	T_C = 25°C	−	−	20	mW
B_{Value}	B−Constant	$B_{25/50}$	−	3450	−	K
		$B_{25/100}$	−	3513	−	K

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS − IGBT

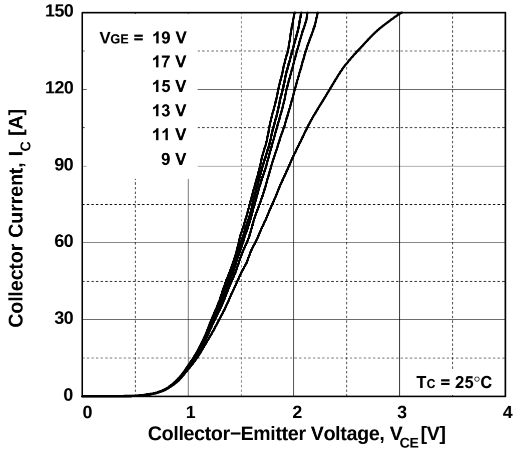


Figure 2. Output Characteristics

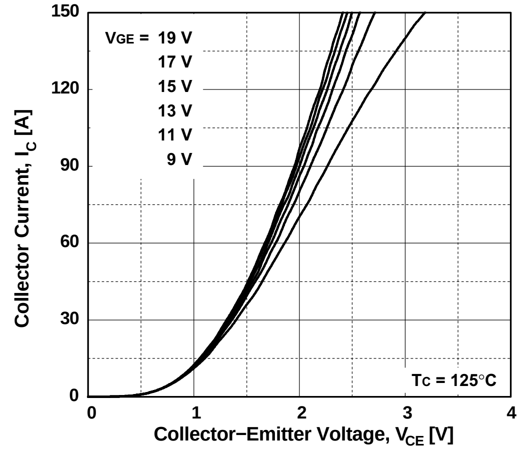


Figure 3. Output Characteristics

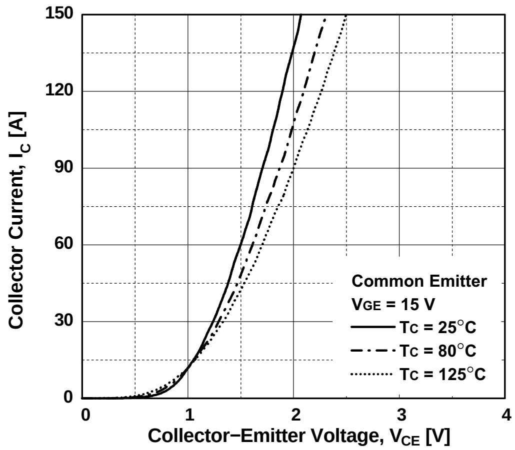


Figure 4. Saturation Voltage Characteristics

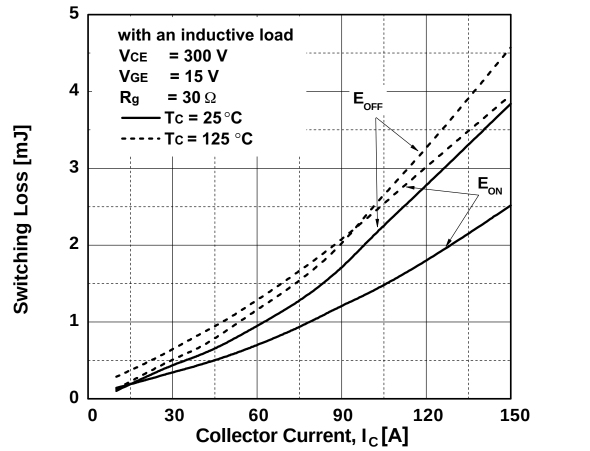


Figure 5. Switching Loss vs. Collector Current

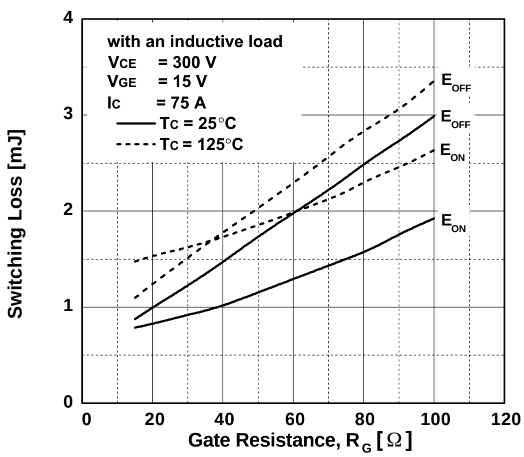


Figure 6. Switching Loss vs. Gate Resistance

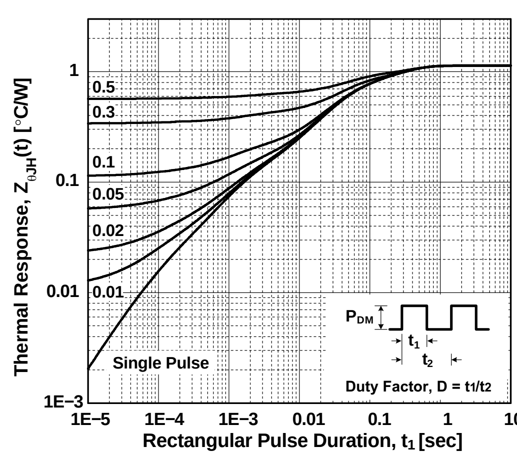


Figure 7. Transient Thermal Impedance

TYPICAL CHARACTERISTICS − FULL−BRIDGE DIODE

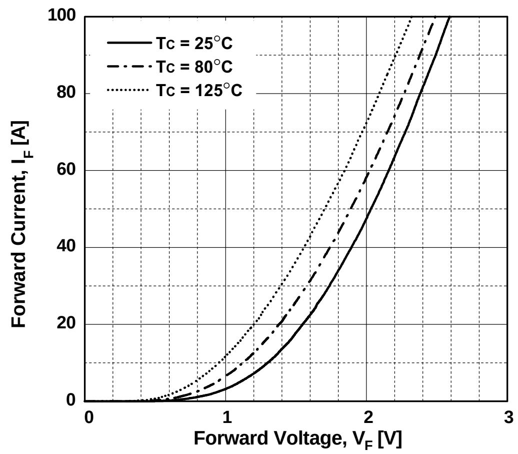


Figure 8. Forward Voltage Drop

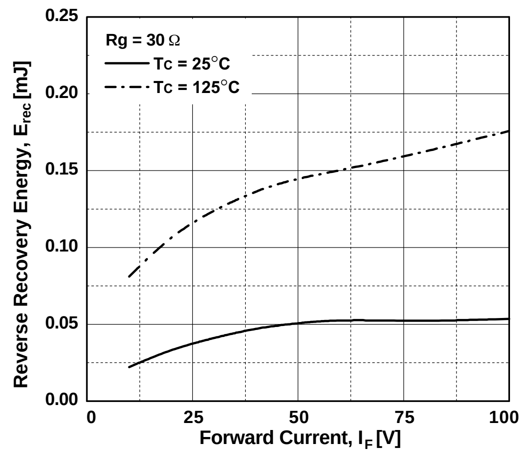


Figure 9. Reverse Recovery Energy vs. Forward Current

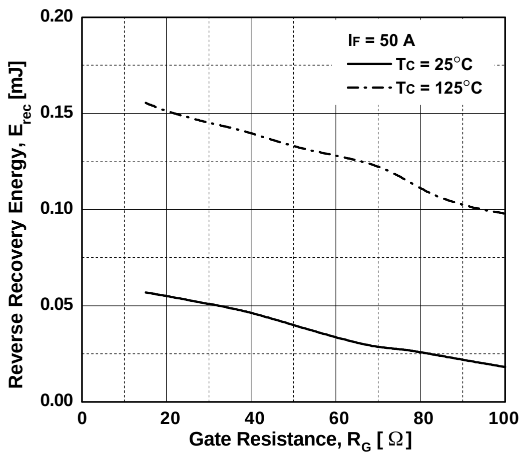


Figure 10. Reverse Recovery Energy vs. Gate Resistance

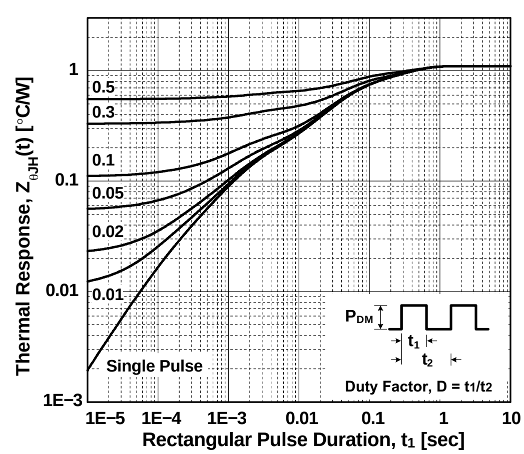


Figure 11. Transient Thermal Impedance

TYPICAL CHARACTERISTICS − HERIC DIODE

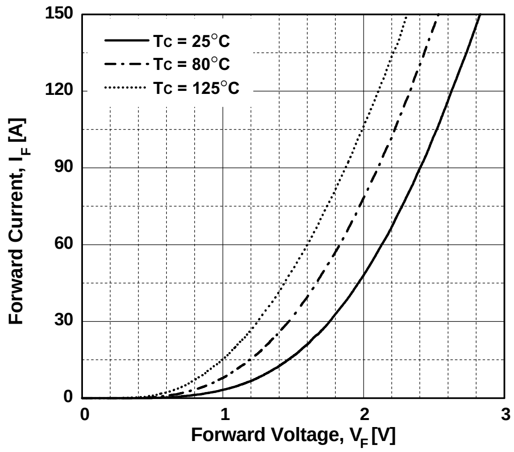


Figure 12. Forward Voltage Drop

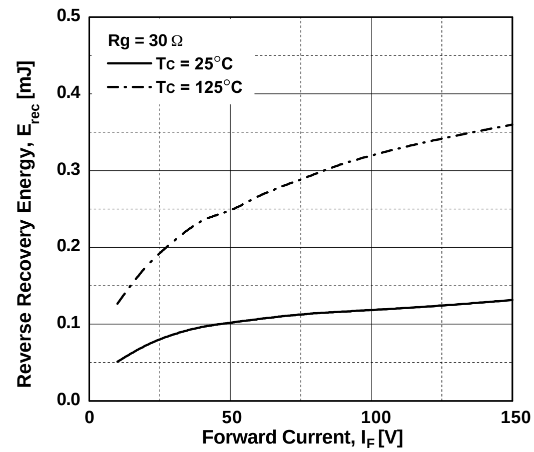


Figure 13. Reverse Recovery Energy vs. Forward Current

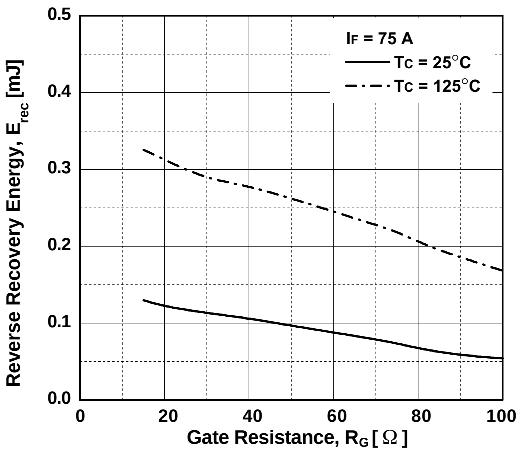


Figure 14. Reverse Recovery Energy vs. Gate Resistance

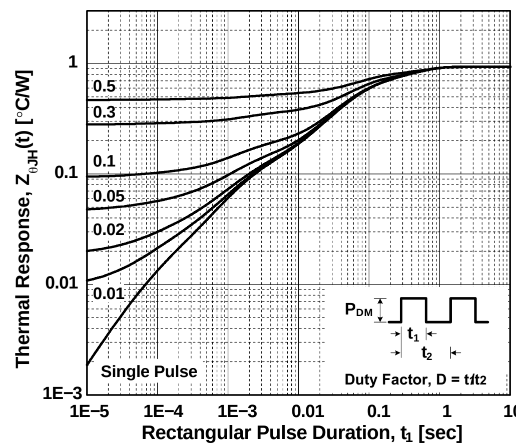


Figure 15. Transient Thermal Impedance

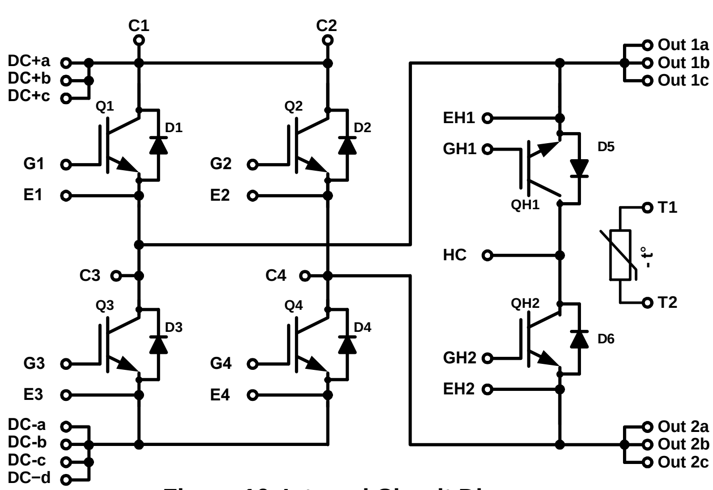
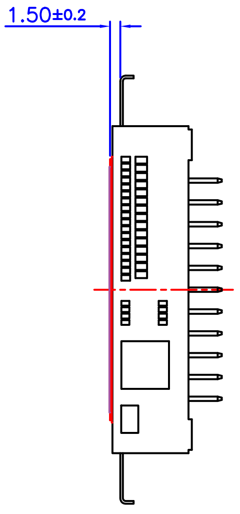


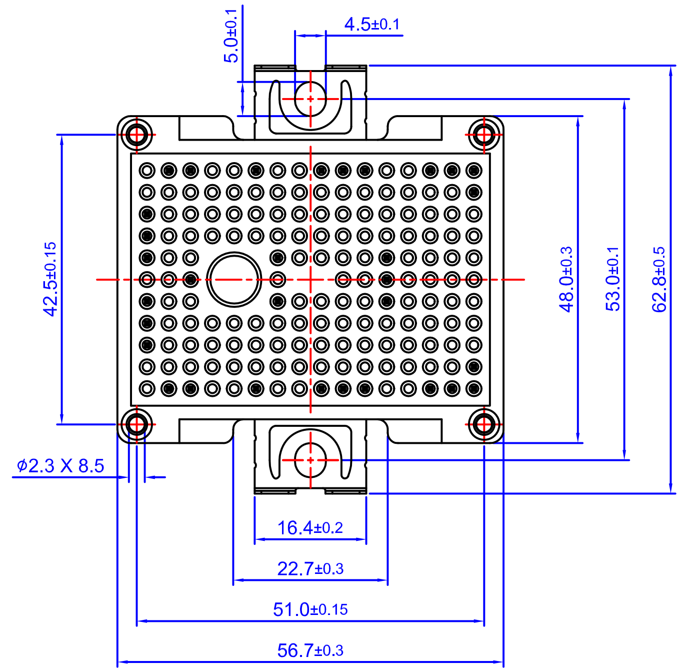
Figure 16. Internal Circuit Diagram

PACKAGE DIMENSIONS

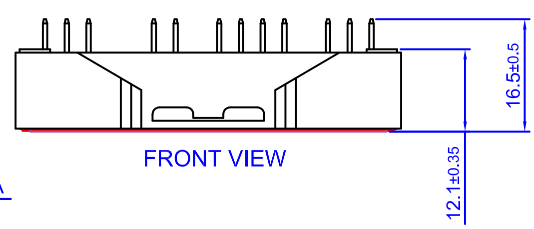
HF2GB−N32
CASE MODFS
ISSUE O



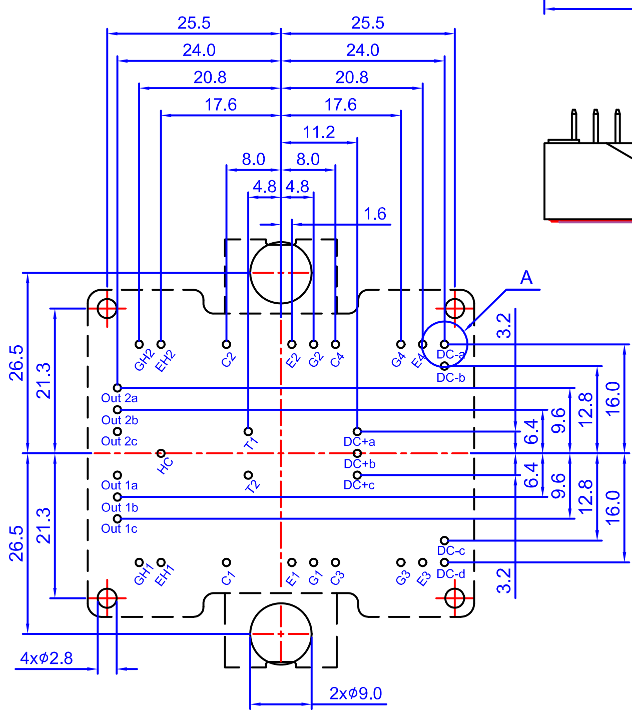
SIDE VIEW



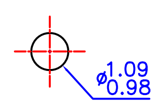
TOP VIEW



FRONT VIEW



PCB HOLE PATTERN RECOMMENDATION



DETAIL A
: END HOLE SIZE
(SCALE N/A)

NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
- B) ALL DIMENSIONS ARE IN MILLIMETERS
- C) FB+HERIC MODULE_VER.B TYPE

- PIN-GRID 3.2mm
- TOLERANCE OF PCB HOLE PATTERN ⌖ Ø0.1

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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