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June 2014

FQA24N50

N-Channel QFET® MOSFET

### 500 V, 24 A, 200 mΩ

Features

- 24 A, 500 V, $R_{DS(on)}$ = 200 mΩ (Max.) @ V_{GS} = 10 V, I_D = 12 A
- Low Gate Charge (Typ. 90 nC)
- Low Crss (Typ. 55 pF)
- 100% Avalanche Tested
- RoHS compliant

Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply, power factor correction, electronic lamp ballast based on half bridge.

TO-3PN
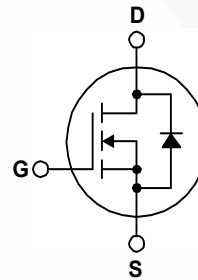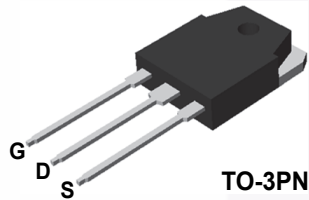
Absolute Maximum Ratings

T_C = 25°C unless otherwise noted.

Symbol	Parameter			FQA24N50	Unit
V_{DSS}	Drain-Source Voltage			500	V
I_D	Drain Current	- Continuous (T_C = 25°C)		24	A
		- Continuous (T_C = 100°C)		15.2	A
I_{DM}	Drain Current	- Pulsed	(Note 1)	96	A
V_{GSS}	Gate-Source Voltage			± 30	V
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	1100	mJ
I_{AR}	Avalanche Current		(Note 1)	24	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	29	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	4.5	V/ns
P_D	Power Dissipation (T_C = 25°C)			290	W
		- Derate above 25°C		2.33	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds			300	°C

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.43	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink	0.24	--	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	40	°C/W

www.fairchildsemi.com

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQA24N50	FQA24N50	TO-3PN	Tube	N/A	N/A	30 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	500	--	--	V
$\Delta BV_{DSS}/$ ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.53	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 400 V, T_C = 125°C	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 12 A	--	0.156	0.2	Ω
g_{FS}	Forward Transconductance	V_{DS} = 50 V, I_D = 12 A	--	22	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	3500	4500	pF
C_{oss}	Output Capacitance		--	520	670	pF
C_{rss}	Reverse Transfer Capacitance		--	55	70	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250 V, I_D = 24 A, R_G = 25 Ω	--	80	170	ns
t_r	Turn-On Rise Time		--	250	500	ns
$t_{d(off)}$	Turn-Off Delay Time		--	200	400	ns
t_f	Turn-Off Fall Time	(Note 4)	--	155	320	ns
Q_g	Total Gate Charge	V_{DS} = 400 V, I_D = 24 A, V_{GS} = 10 V	--	90	120	nC
Q_{gs}	Gate-Source Charge		--	23	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4)	--	44	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	24	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	96	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 24 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 24 A, dI_F / dt = 100 A/μs	--	400	--	ns
Q_{rr}	Reverse Recovery Charge		--	4.3	--	μC

Notes :

1. Repetitive rating : pulse width limited by maximum junction temperature.

2. L = 3.4 mH, I_{AS} = 24 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.

3. $I_{SD} \leq$ 24 A, di/dt $\leq$ 200 A/μs, $V_{DD} \leq BV_{DSS,}$ starting T_J = 25°C.

4. Essentially independent of operating temperature.
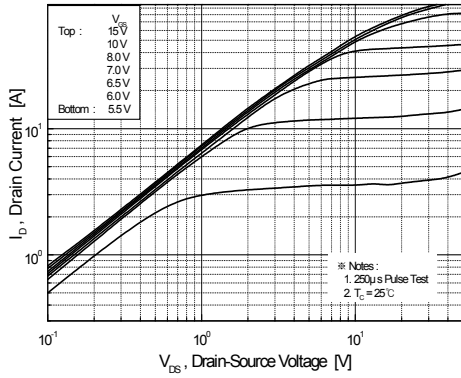
Typical Characteristics

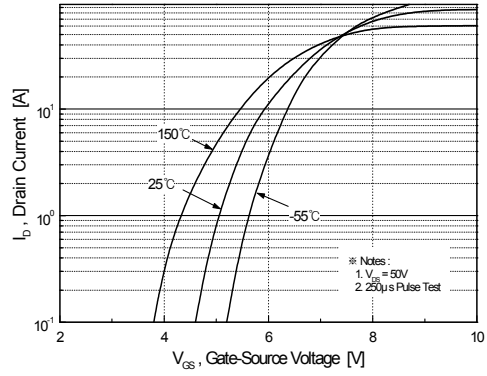**Figure 1. On-Region Characteristics**
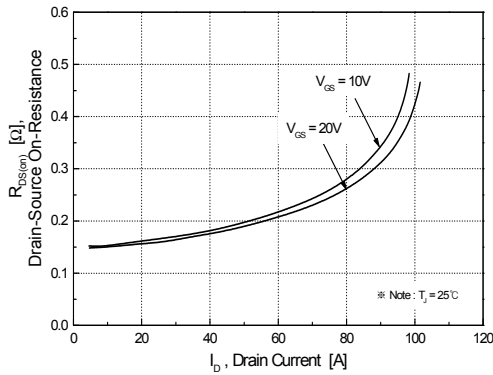
Figure 2. Transfer Characteristics

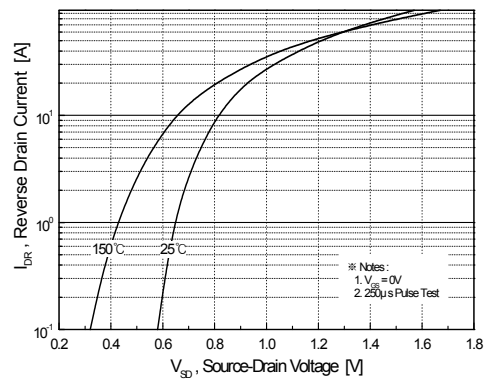**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature
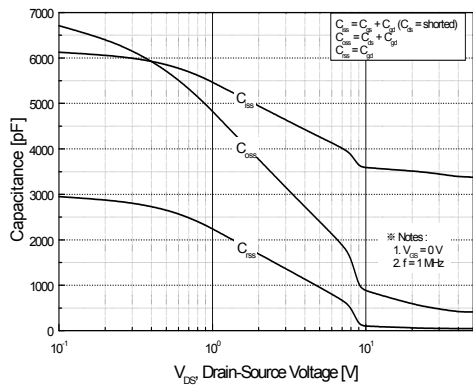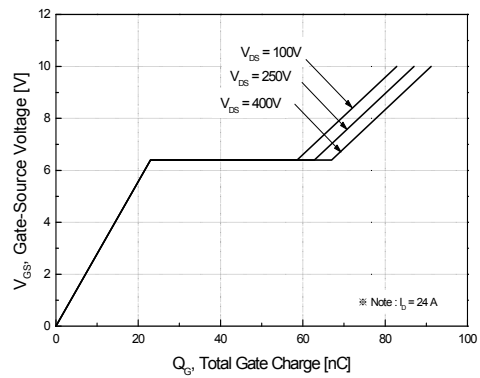
Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics
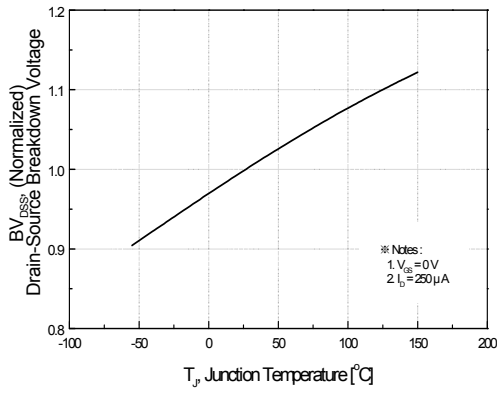
Typical Characteristics (Continued)

**Figure 7. Breakdown Voltage Variation
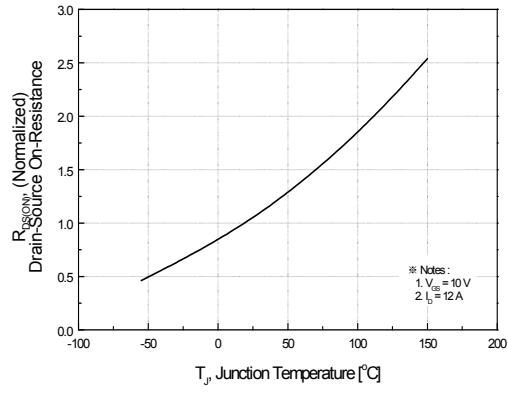vs. Temperature**
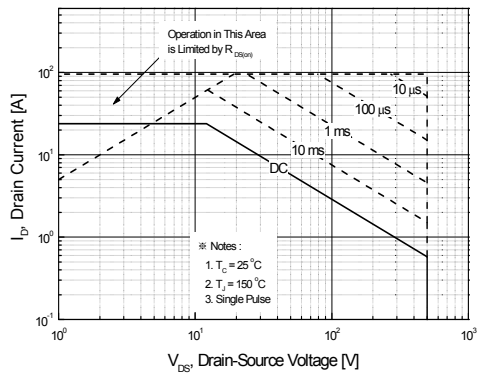

**Figure 8. On-Resistance Variation
vs. Temperature**
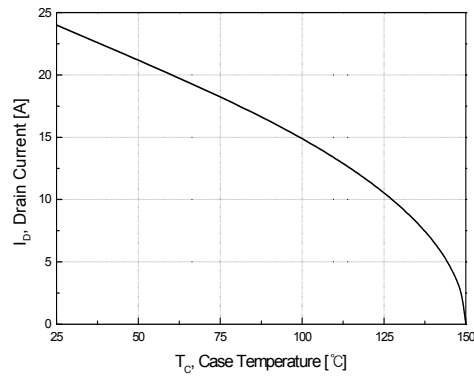

Figure 9. Maximum Safe Operating Area
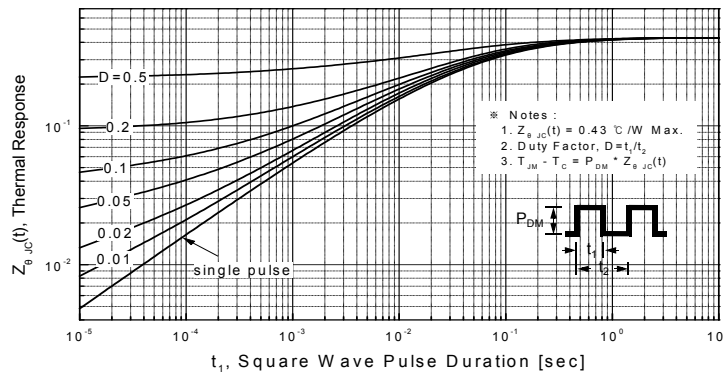

**Figure 10. Maximum Drain Current
vs. Case Temperature**

Figure 11. Transient Thermal Response Curve

Figure 12. Gate Charge Test Circuit & Waveform

12V 200nF 50KΩ 300nF Same Type as DUT

V_{GS}

I_G = const.

DUT

V_{DS}

V_{GS}

Q_g

Q_{gs} Q_{gd}

Charge
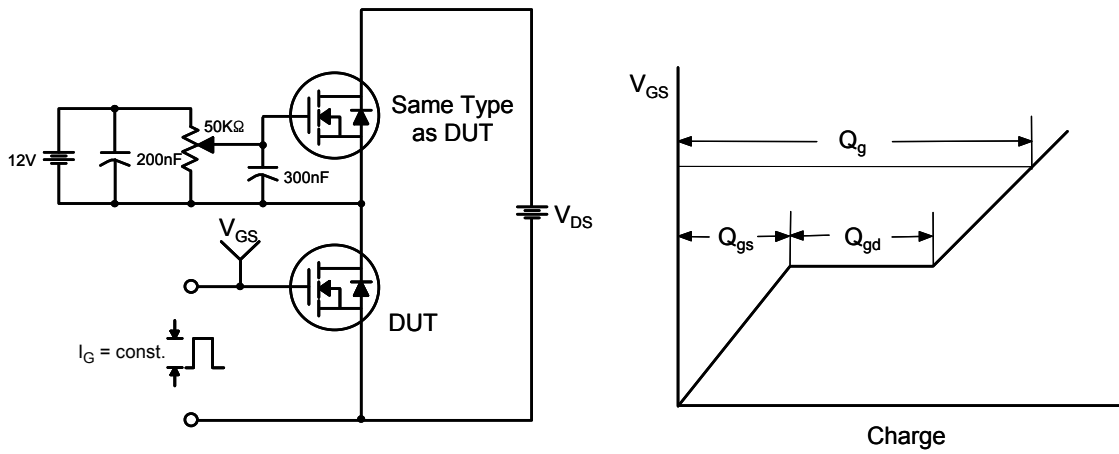
Figure 13. Resistive Switching Test Circuit & Waveforms

V_{DS} R_L V_{DD}

R_G V_{GS}

V_{GS}

DUT

V_{DS} 90%

V_{GS} 10%

$t_{d(on)}$ t_r $t_{d(off)}$ t_f

t_{on} t_{off}
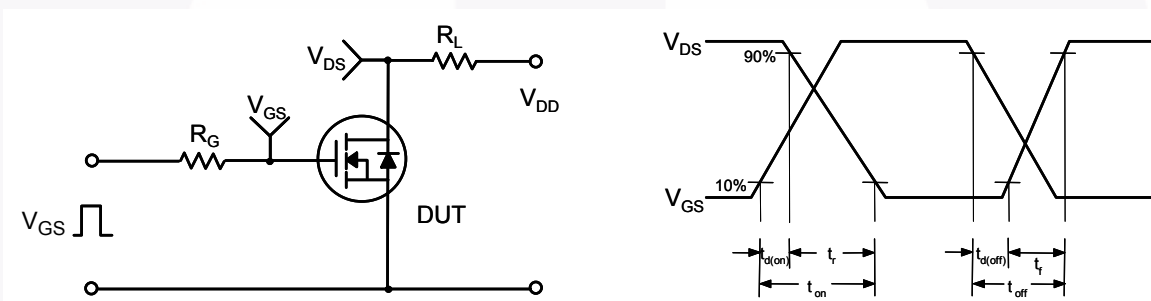
Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

V_{DS} L

I_D

R_G V_{DD}

V_{GS}

t_p

DUT

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \ \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

BV_{DSS}

I_{AS}

$I_D (t)$

V_{DD}

$V_{DS} (t)$

t_p

Time
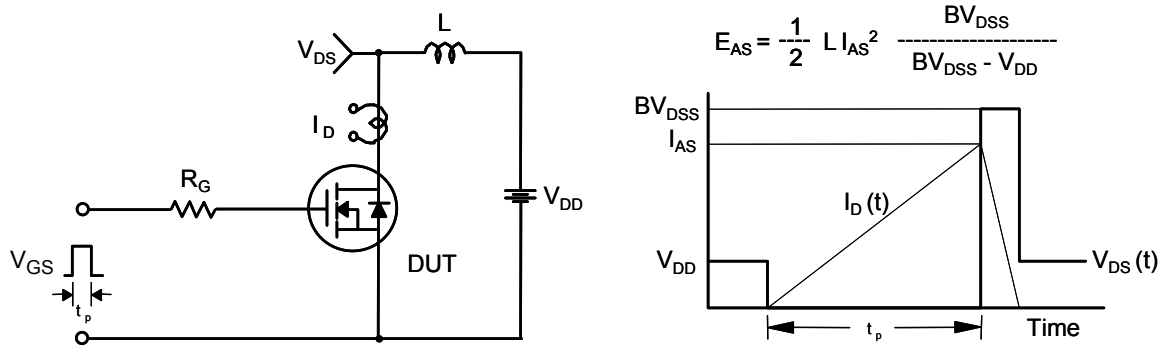
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

DUT

V_{DS}

I_{SD}

L

Driver

R_G

Same Type
as DUT

V_{DD}

V_{GS}

• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

V_{GS}
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_{SD}
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode
Forward Voltage Drop

Mechanical Dimensions

5.20
4.80

16.20
15.40

20.10
19.70

18.90
18.50

(1.85)

1

3

3.70
3.30

2.20
1.80

3.20
2.80

1.20
0.80

$\bigoplus \phi$ 0.55 ⓜ

5.45

5.45

(R0.50)

5.00
4.60

1.65
1.45

(R0.50)

3°

4°

3°

2.90
1.90

0.75
0.55

13.80
13.40

ϕ 3.30
3.10

ϕ 7.20
6.80

16.96
16.56

20.30
19.70

NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO EIAJ
   SC-65 PACKAGING STANDARD.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSION AND TOLERANCING PER
   ASME14.5-2009.
D) DIMENSIONS ARE EXCLUSIVE OF BURRS,
   MOLD FLASH, AND TIE BAR EXTRUSSIONS.
E) DRAWING FILE NAME: TO3PN03AREV1.
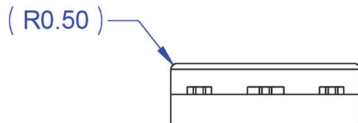F) FAIRCHILD SEMICONDUCTOR.

Figure 16. TO3PN, 3-Lead, Plastic, EIAJ SC-65

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