

MOSFET – P-Channel, QFET®

FQD3P50

-500 V, 4.9 Ω, -2.1 A

Description

This P-Channel enhancement mode power MOSFET is produced using ON Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- -2.1 A, -500 V, $R_{DS(on)} = 4.9 \Omega$ (Max.) @ $V_{GS} = -10$ V, $I_D = -1.05$ A
- Low Gate Charge (Typ. 18 nC)
- Low Crss (Typ. 9.5 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS ($T_C = 20^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage	-500	V
I_D	Drain Current		A
	- Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	-2.1 -1.33	
I_{DM}	Drain Current - Pulsed (Note 1)	-8.4	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	250	mJ
I_{AR}	Avalanche Current (Note 1)	-2.1	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-4.5	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) (Note 4)	2.5	W
	Power Dissipation ($T_C = 25^\circ\text{C}$) - Derate above 25°C	50 0.4	W W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C

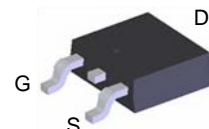
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $L = 102$ mH, $I_{AS} = -2.1$ A, $V_{DD} = -50$ V, $R_G = 25 \Omega$, Starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq -2.7$ A, $di/dt \leq 200$ A/ms, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$.
4. When mounted on the minimum pad size recommended (PCB Mount).

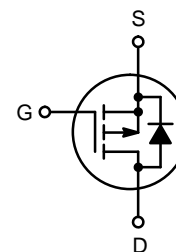


ON Semiconductor®

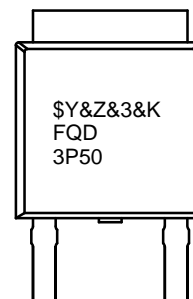
www.onsemi.com



DPAK3
CASE 369AS



MARKING DIAGRAM



\$Y = ON Semiconductor Logo
 &Z = Assembly Code
 &3 = Date Code (Year and Week)
 &K = Lot Code
 FQD3P50 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FQD3P50	DPAK3 (Pb-Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

FQD3P50

THERMAL CHARACTERISTICS

Symbol	Parameter	FQD3P50	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max. (Note 5)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	110	°C/W

5. When mounted on the minimum pad size recommended (PCB Mount).

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
--------	----------------	-----------------	-----	-----	-----	------

OFF CHARACTERISTICS

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ mA}$	-500	-	-	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ mA}$, Referenced to 25°C	-	0.42	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -500\text{ V}, V_{GS} = 0\text{ V}$	-	-	-1	μA
		$V_{DS} = -400\text{ V}, T_C = 125^\circ\text{C}$	-	-	-10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	-	-	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	-	-	100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ mA}$	-3.0	-	-5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -1.05\text{ A}$	-	3.9	4.9	Ω
g_{FS}	Forward Transconductance	$V_{DS} = -50\text{ V}, I_D = -1.05\text{ A}$	-	2.1	-	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	-	510	660	pF
C_{oss}	Output Capacitance		-	70	90	pF
C_{rss}	Reverse Transfer Capacitance		-	9.5	12	pF

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -250\text{ V}, I_D = -2.7\text{ A},$ $R_G = 25\ \Omega$ (Note 6)	-	12	35	ns
t_r	Turn-On Rise Time		-	56	120	ns
$t_{d(off)}$	Turn-Off Delay Time		-	35	80	ns
t_f	Turn-Off Fall Time		-	45	100	ns
Q_g	Total Gate Charge	$V_{DS} = -400\text{ V}, I_D = -2.7\text{ A},$ $V_{GS} = -10\text{ V}$ (Note 6)	-	18	23	nC
Q_{gs}	Gate-Source Charge		-	3.6	-	nC
Q_{gd}	Gate-Drain Charge		-	9.2	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I_S	Maximum Continuous Drain-Source Diode Forward Current	-	-	-2.1	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	-	-	-8.4	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -2.1\text{ A}$	-	-	-5.0	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = -2.7\text{ A},$ $dI_F/dt = 100\text{ A/ms}$	-	270	-	ns
Q_{rr}	Reverse Recovery Charge		-	1.5	-	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Essentially independent of operating temperature.

TYPICAL PERFORMANCE CURVES

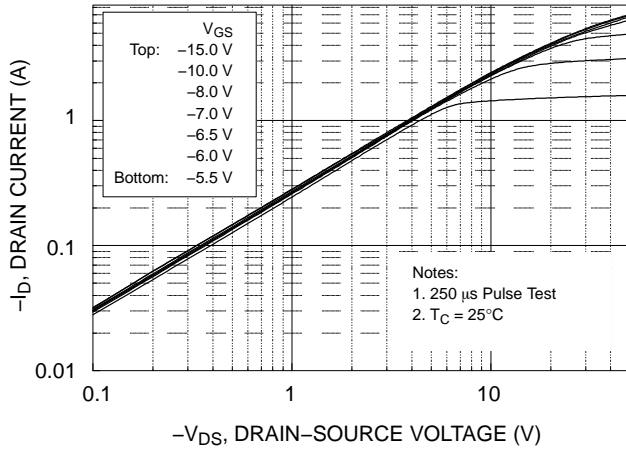


Figure 1. On-Region Characteristics

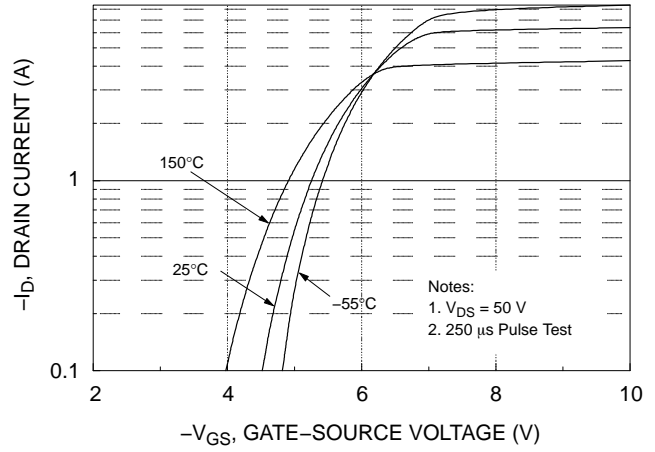


Figure 2. Transfer Characteristics

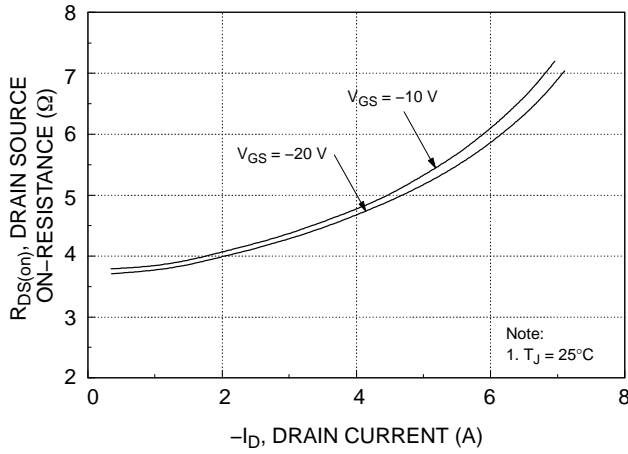


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

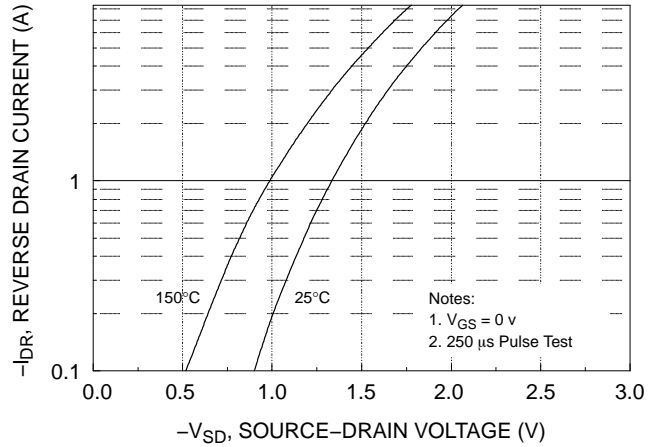


Figure 4. Body Diode Forward Voltage Variant vs. Source Current and Temperature

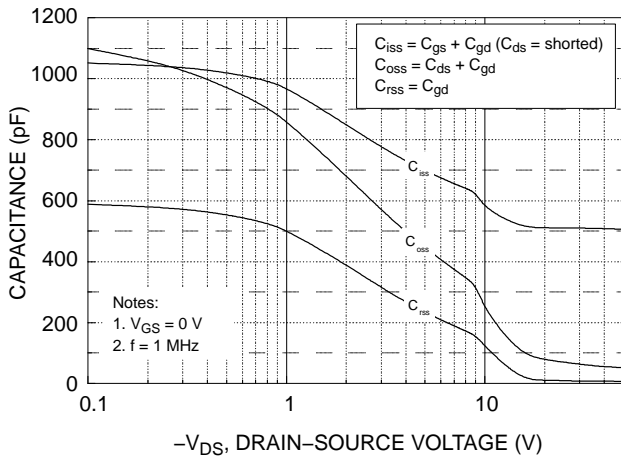


Figure 5. Capacitance Characteristics

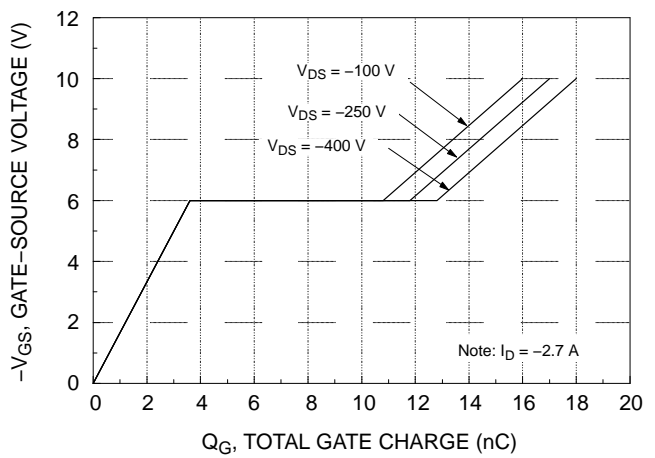


Figure 6. Gate Charge Characteristics

FQD3P50

TYPICAL PERFORMANCE CURVES (CONTINUED)

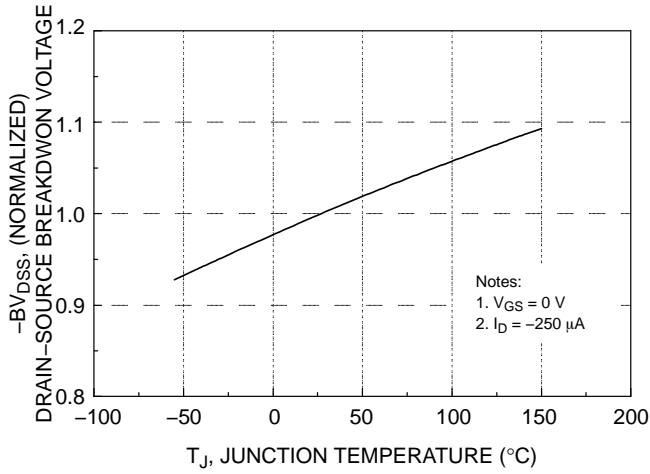


Figure 7. Breakdown Voltage Variation vs. Temperature

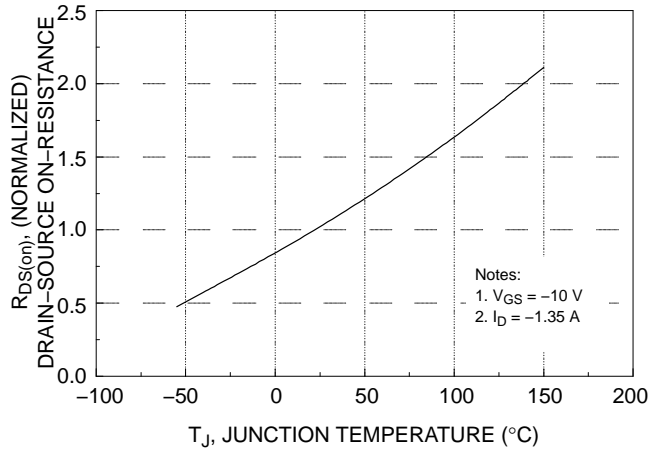


Figure 8. On-Resistance Variation vs. Temperature

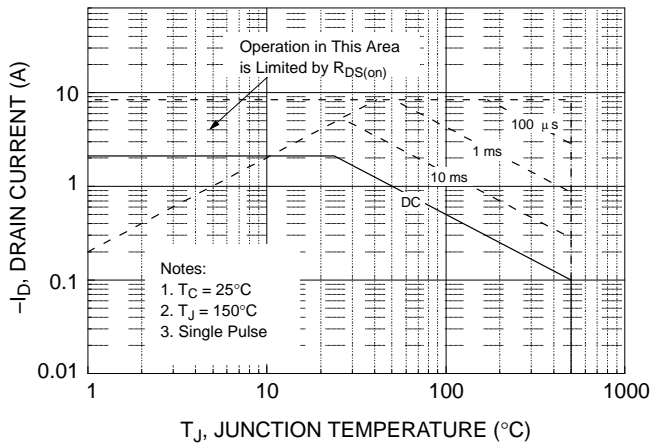


Figure 9. Maximum Safe Operation Area

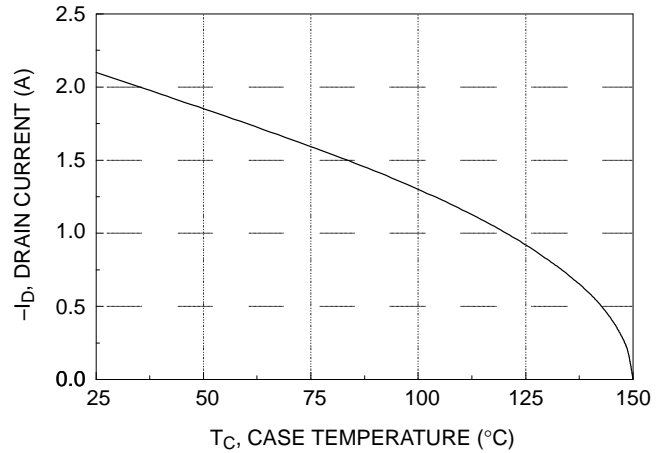


Figure 10. Maximum Drain Current vs. Case Temperature

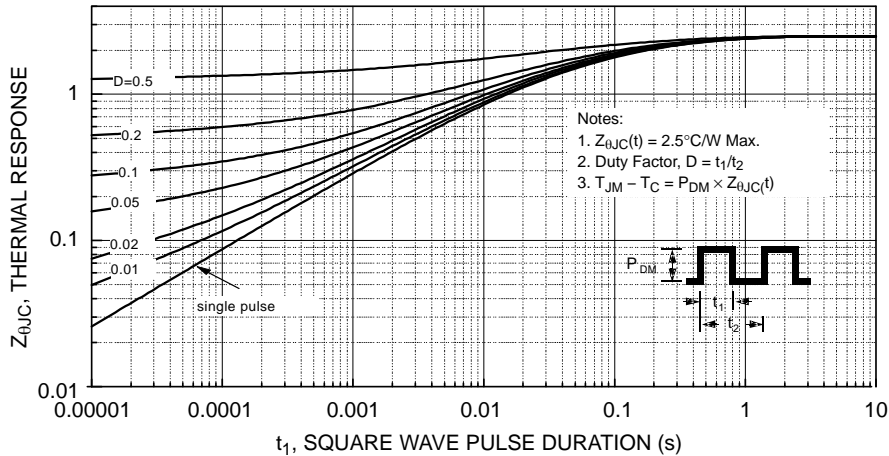


Figure 11. Transient Thermal Response Curve

FQD3P50

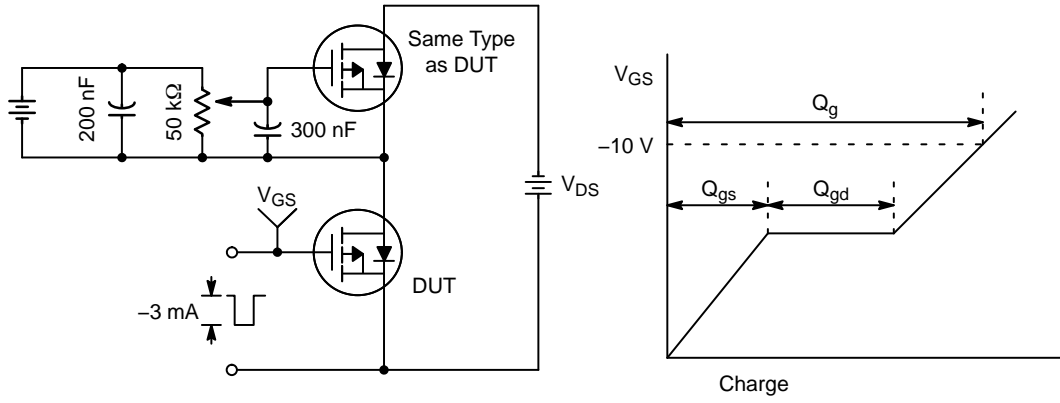


Figure 12. Gate Charge Test Circuit & Waveform

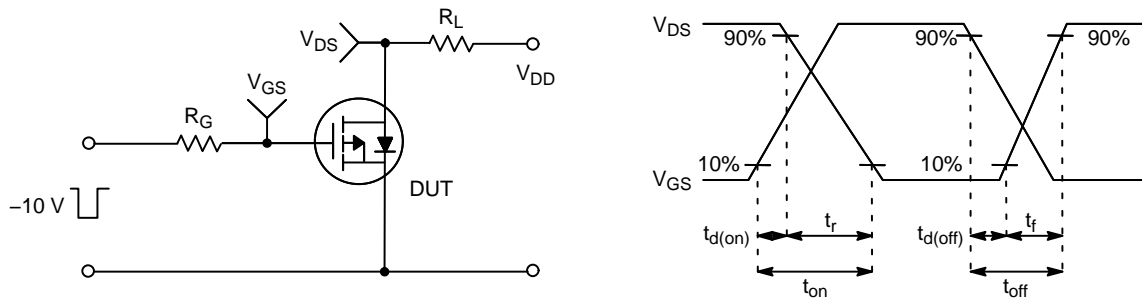


Figure 13. Resistive Switching Test Circuit & Waveforms

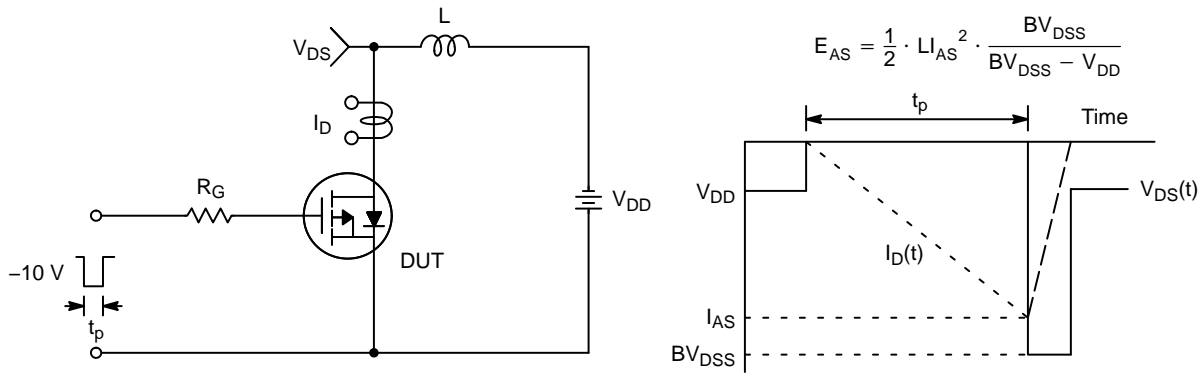


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

FQD3P50

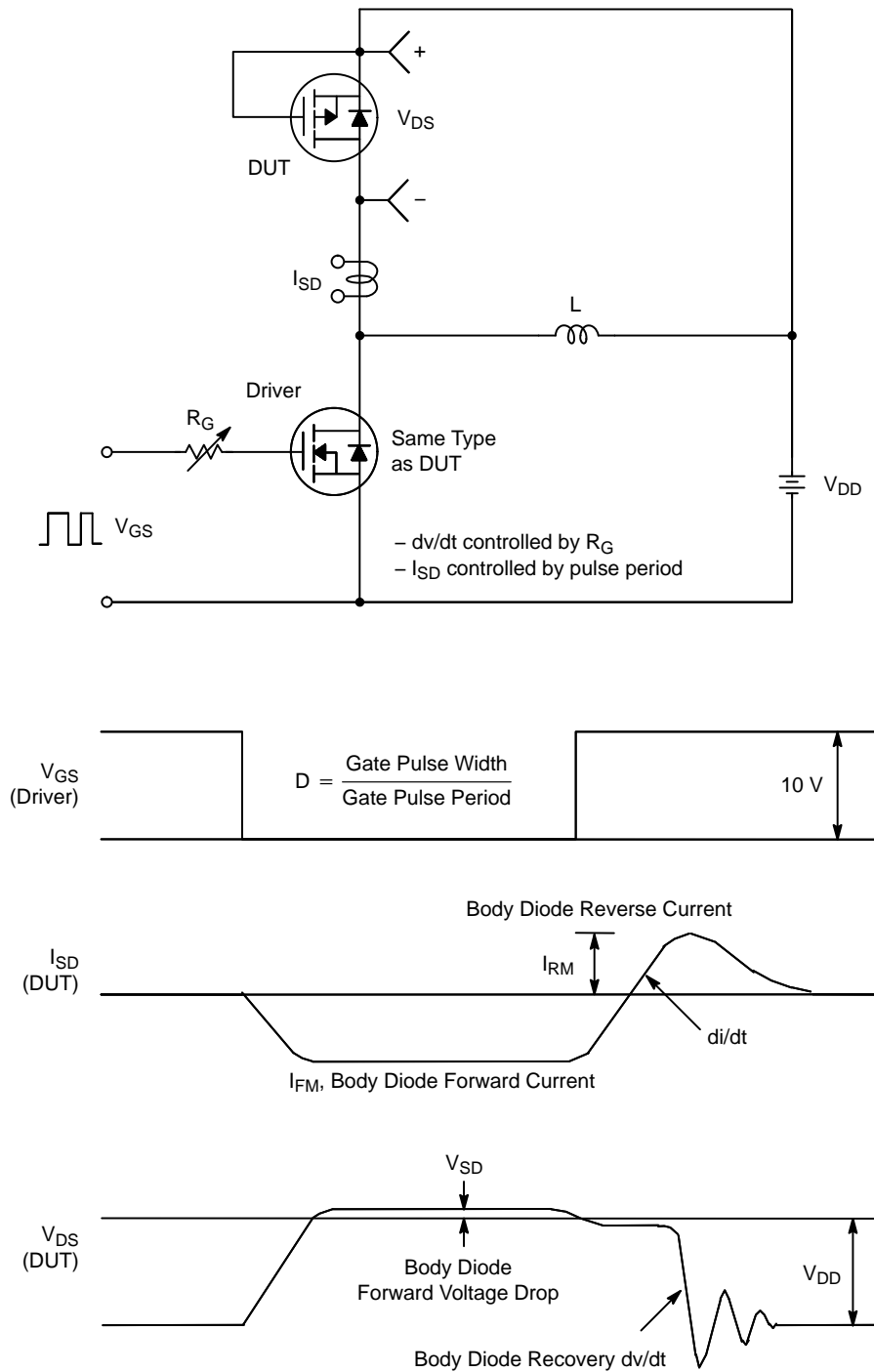


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

QFET is a registered trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

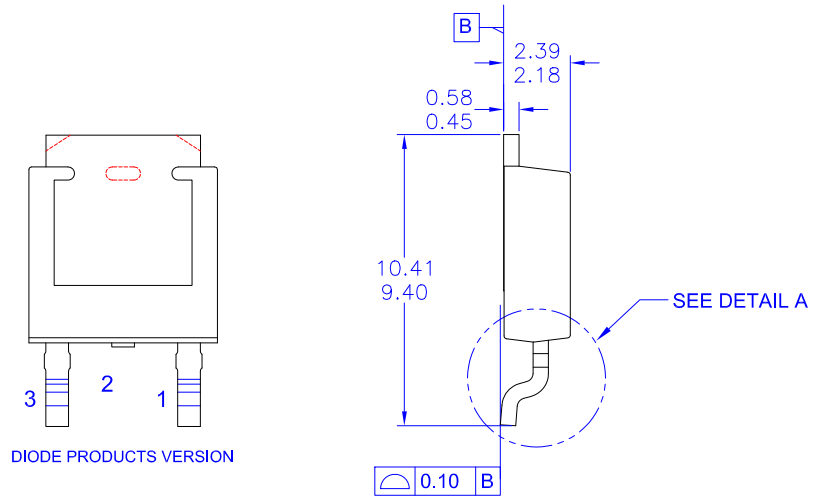
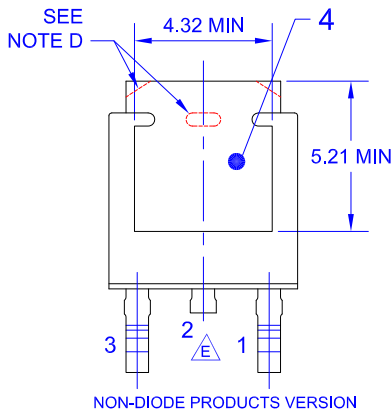
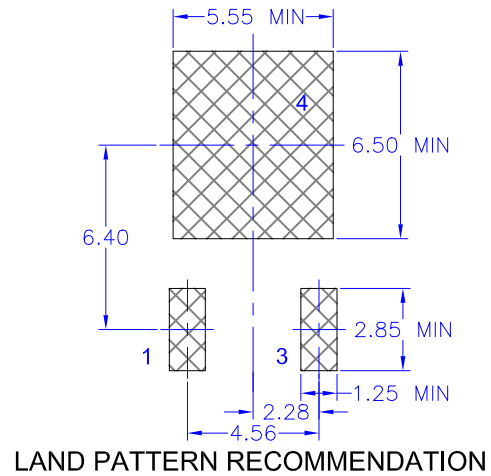
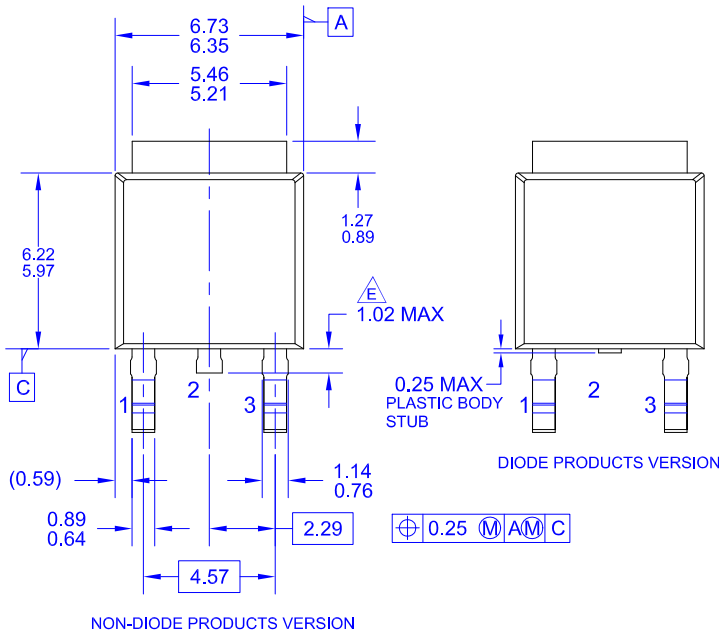


DPAK3 (TO-252 3 LD)

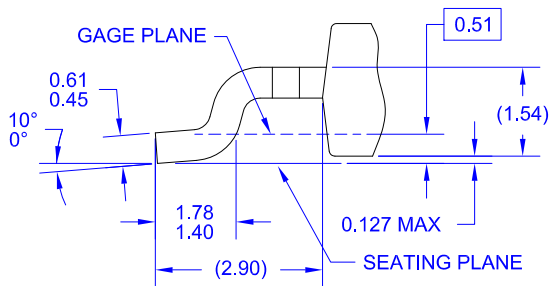
CASE 369AS

ISSUE O

DATE 30 SEP 2016




- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
 - D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
 - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



DOCUMENT NUMBER:	98AON13810G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	DPAK3 (TO-252 3 LD)	PAGE 1 OF 2



ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION FROM FAIRCHILD TO263A03 TO ON SEMICONDUCTOR. REQ. BY I. CAMBALIZA.	30 SEP 2016

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local
Sales Representative