FQP11N40C, FQPF11N40C

QFET® MOSFET, N-Channel

400 V, 10.5 A, 530 mΩ

ON Semiconductor®

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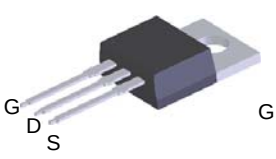
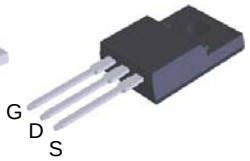
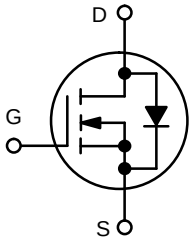


TO−220−3LD
CASE 340AT



TO−220F−3SG
CASE 221AT



Description

This N−Channel enhancement mode power MOSFET is produced using ON Semiconductor proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on−state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 10.5 A, 400 V, $R_{DS(on)}$ = 530 mΩ (Max.) @ V_{GS} = 10 V, I_D = 5.25 A
- Low Gate Charge (Typ. 28 nC)
- Low Crss (Typ. 85 pF)
- 100% Avalanche Tested
- These Devices are Pb−Free and are RoHS Compliant

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Device	Device Marking	Package	Shipping
FQP11N40C	FQP11N40C	TO−220 (Pb−Free)	1,000 Units / Tube
FQPF11N40C	FQPF11N40C	TO−220 Fullpack, TO−220F−3SG (Pb−Free)	1,000 Units / Tube

MOSFET MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		FQP11N40C	FQPF11N40C	Unit
V_{DSS}	Drain to Source Voltage		400		V
I_D	Drain Current −Continuous (T_C = 25°C)		10.5	10.5 *	A
	−Continuous (T_C = 100°C)		6.6	6.6 *	A
I_{DM}	Drain Current − Pulsed	(Note 1)	42	42 *	A
V_{GSS}	Gate to Source Voltage		± 30		V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	360		mJ
I_{AR}	Avalanche Current	(Note 1)	11		A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	13.5		mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5		V/ns
P_D	Power Dissipation (T_C = 25°C)		135	44	W
	− Derate above 25°C		1.07	0.35	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to 150		°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8” from Case for 5 Seconds		300		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*Drain current limited by maximum junction temperature
1. Repetitive Rating : Pulse width limited by maximum junction temperature.
2. L = 5.7 mH, I_{AS} = 10.5 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 10.5 A, di/dt ≤ 200 A/μs, V_{DD} ≤ $BV_{DSS,}$ starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	FQP11N40C	FQPF11N40C	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	0.93	2.86	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max	62.5	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	400			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		0.54		V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 400 V, V_{GS} = 0 V			1	μA
		V_{DS} = 320 V, T_C = 125°C			10	μA
I_{GSSF}	Gate−Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate−Body Leakage Current, Reverse	V_{GS} = −30 V, V_{DS} = 0 V			−100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.0		4.0	V
$r_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 10 V, I_D = 5.25 A		0.43	0.53	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 5.25 A		7.1		s
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz		840	1090	pF
C_{oss}	Output Capacitance			250	325	pF
C_{rss}	Reverse Transfer Capacitance			85	110	pF
Switching Characteristics						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 200 V, I_D = 10.5 A, R_G = 25 Ω (Note 4)		14	40	ns
t_r	Turn−On Rise Time			89	190	ns
$t_{d(off)}$	Turn−Off Delay Time			81	170	ns
t_f	Turn−Off Fall Time			81	170	ns
Q_g	Total Gate Charge	V_{DS} = 320 V, I_D = 10.5 A, R_G = 25 Ω (Note 4)		28	35	nC
Q_{gs}	Gate−Source Charge			4		nC
Q_{gd}	Gate−Drain Charge			15		nC
Drain−Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain−Source Diode Forward Current				10.5	A
I_{SM}	Maximum Pulsed Drain−Source Diode Forward Current				42	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 10.5 A			1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 10.5 A, dI_F/dt = 100 A/μs		290		ns
Q_{rr}	Reverse Recovery Charge			2.4		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

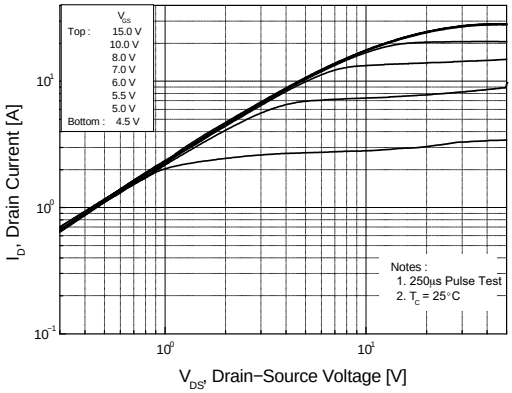


Figure 1. On−Region Characteristics

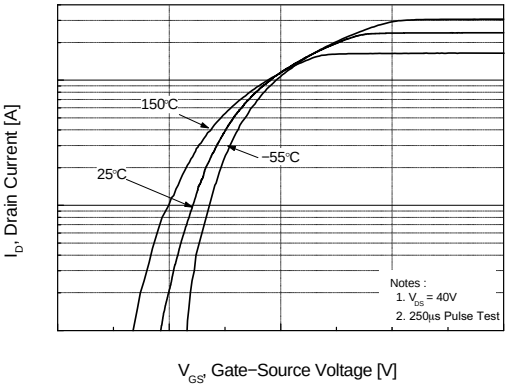


Figure 2. Transfer Characteristics

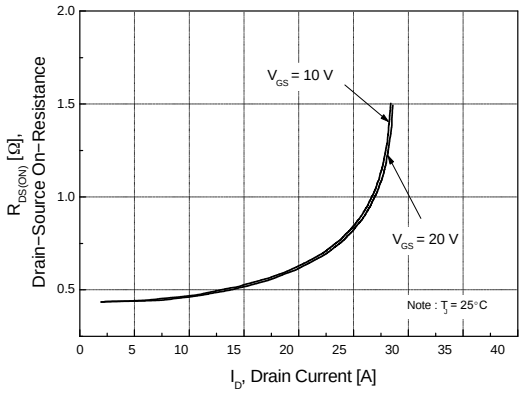


Figure 3. On−Resistance Variation vs Drain Current and Gate Voltage

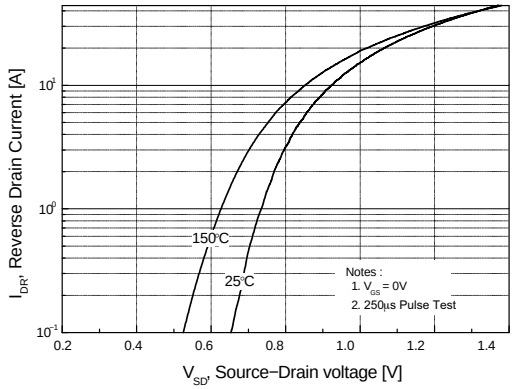


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

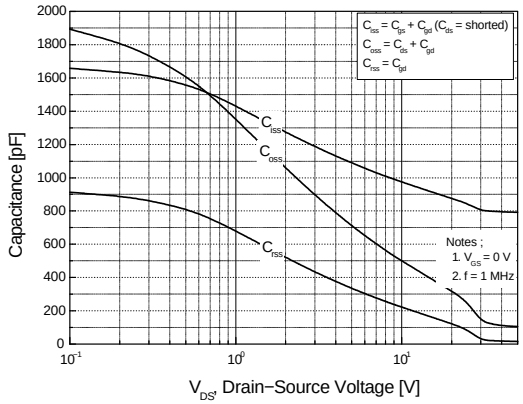


Figure 5. Capacitance Characteristics

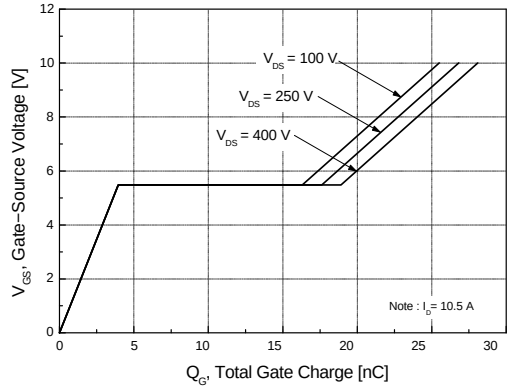


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS

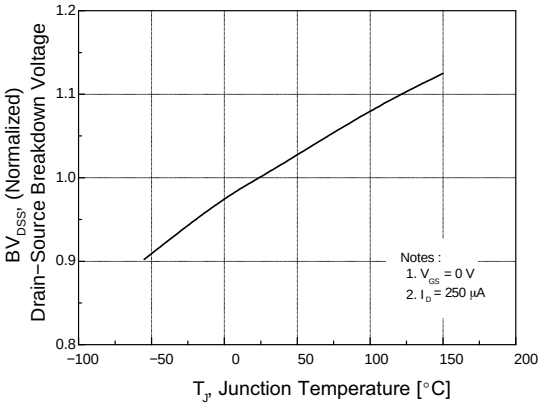


Figure 7. Breakdown Voltage Variation vs. Temperature

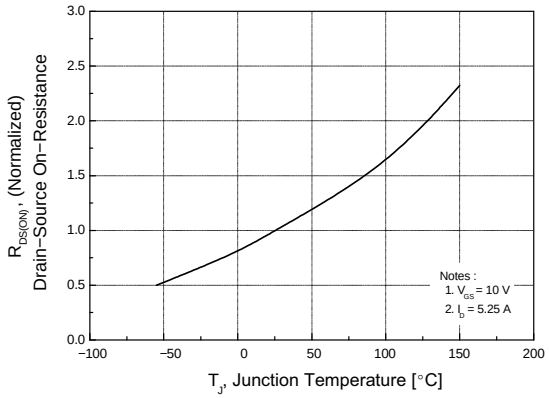


Figure 8. On−Resistance Variation vs. Temperature

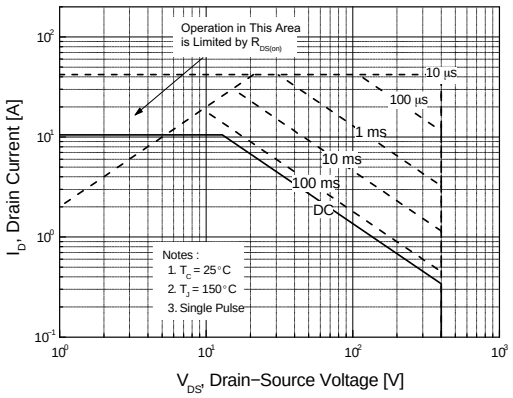


Figure 9. Maximum Safe Operating Area of FQP11N40C

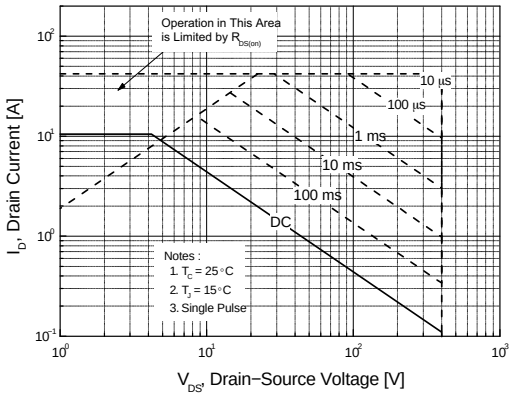


Figure 10. Maximum Safe Operating Area of FQPF11N40C

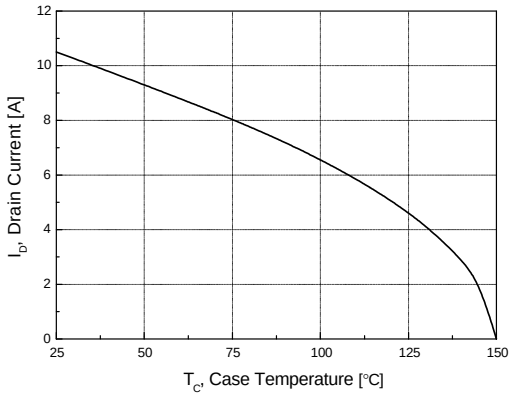


Figure 11. Maximum Drain Current

TYPICAL PERFORMANCE CHARACTERISTICS

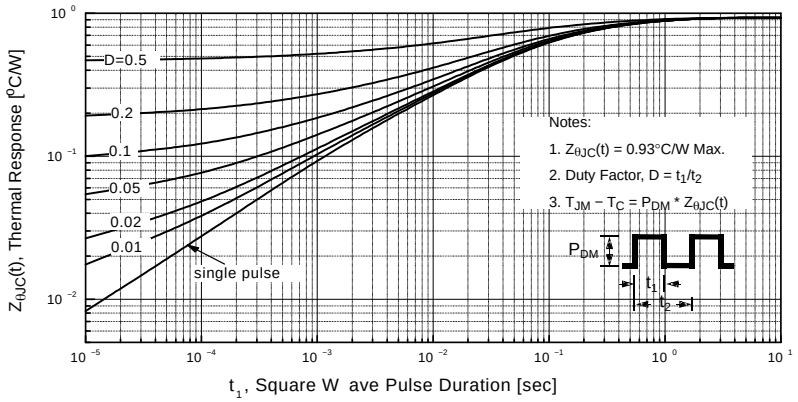


Figure 12. Transient Thermal Response Curve of FQP11N40C

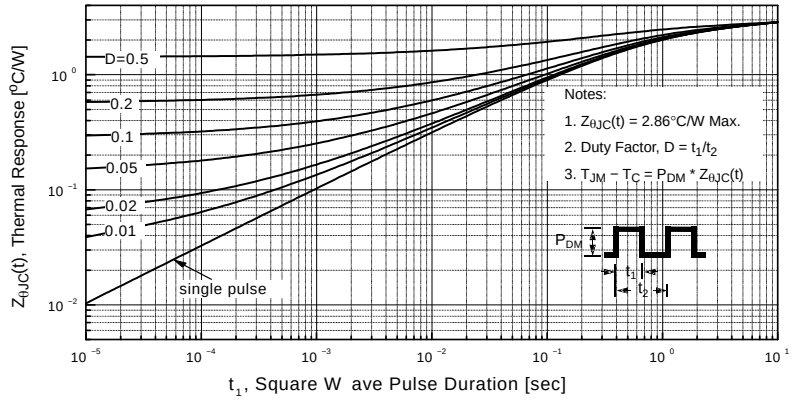


Figure 13. Transient Thermal Response Curve of FQPF11N40C

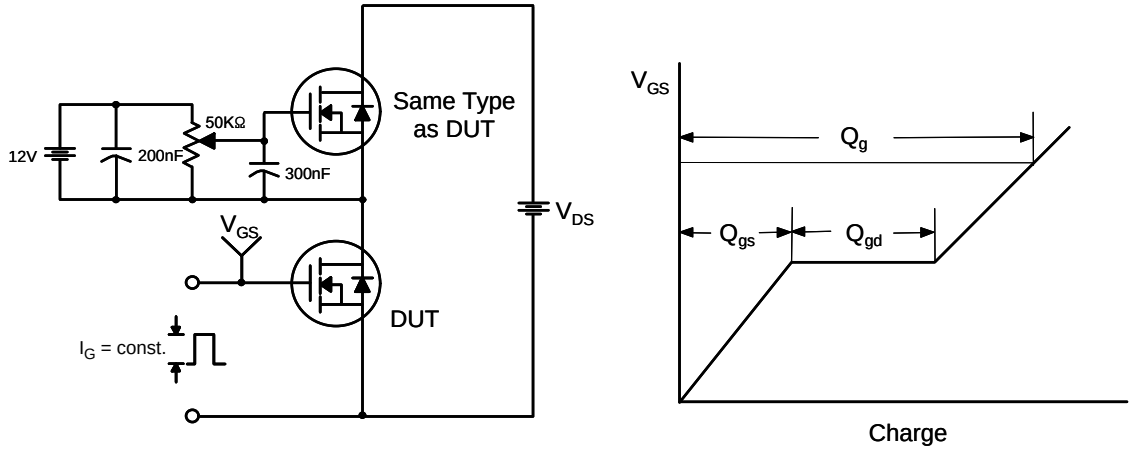


Figure 14. Gate Charge Test Circuit & Waveform

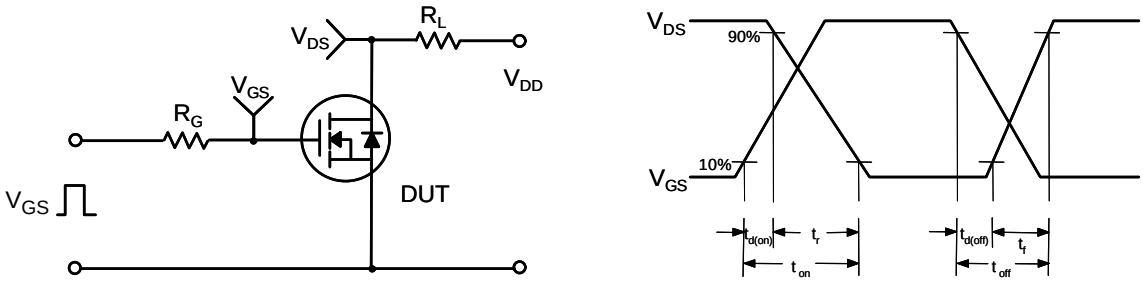


Figure 15. Resistive Switching Test Circuit & Waveforms

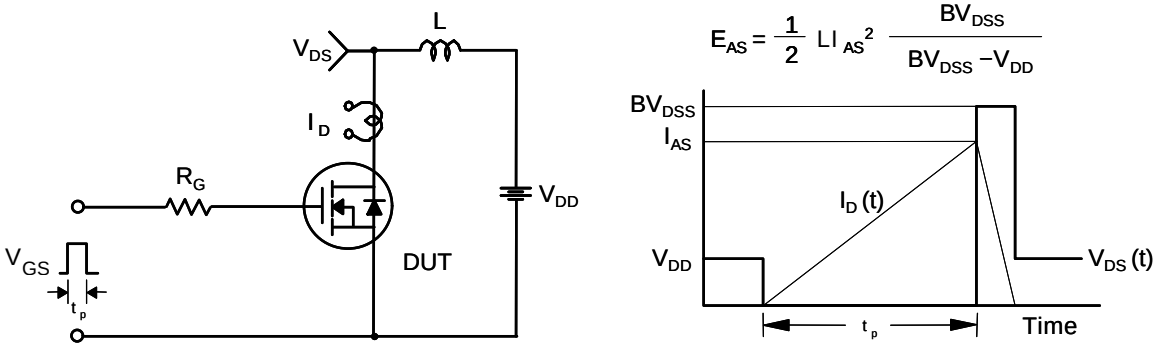


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

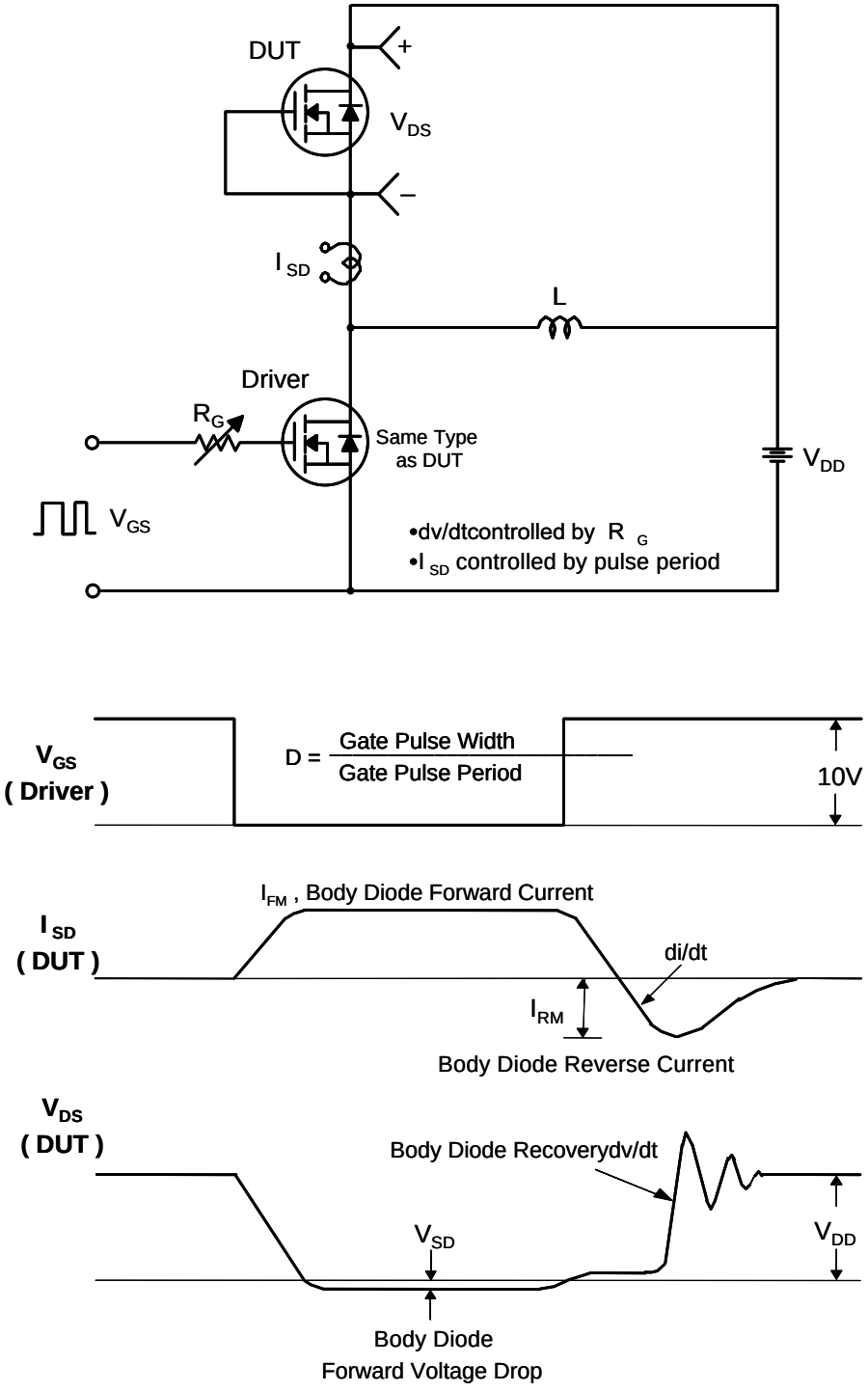


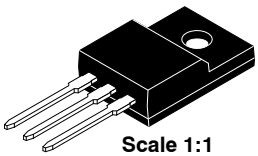
Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

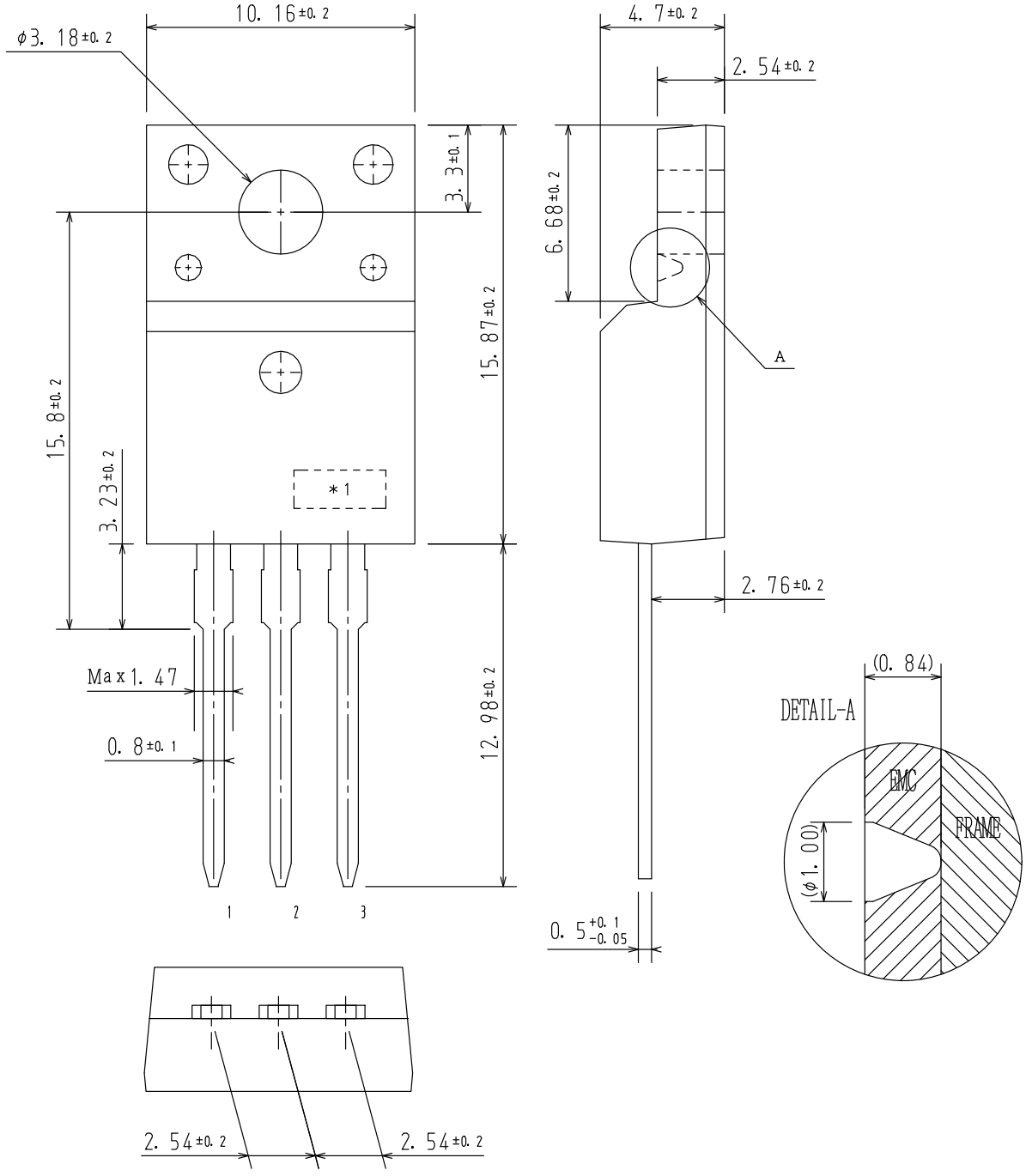
ON Semiconductor®

TO−220 Fullpack, 3−Lead / TO−220F−3SG
CASE 221AT
ISSUE A

DATE 12 NOV 2013



Scale 1:1



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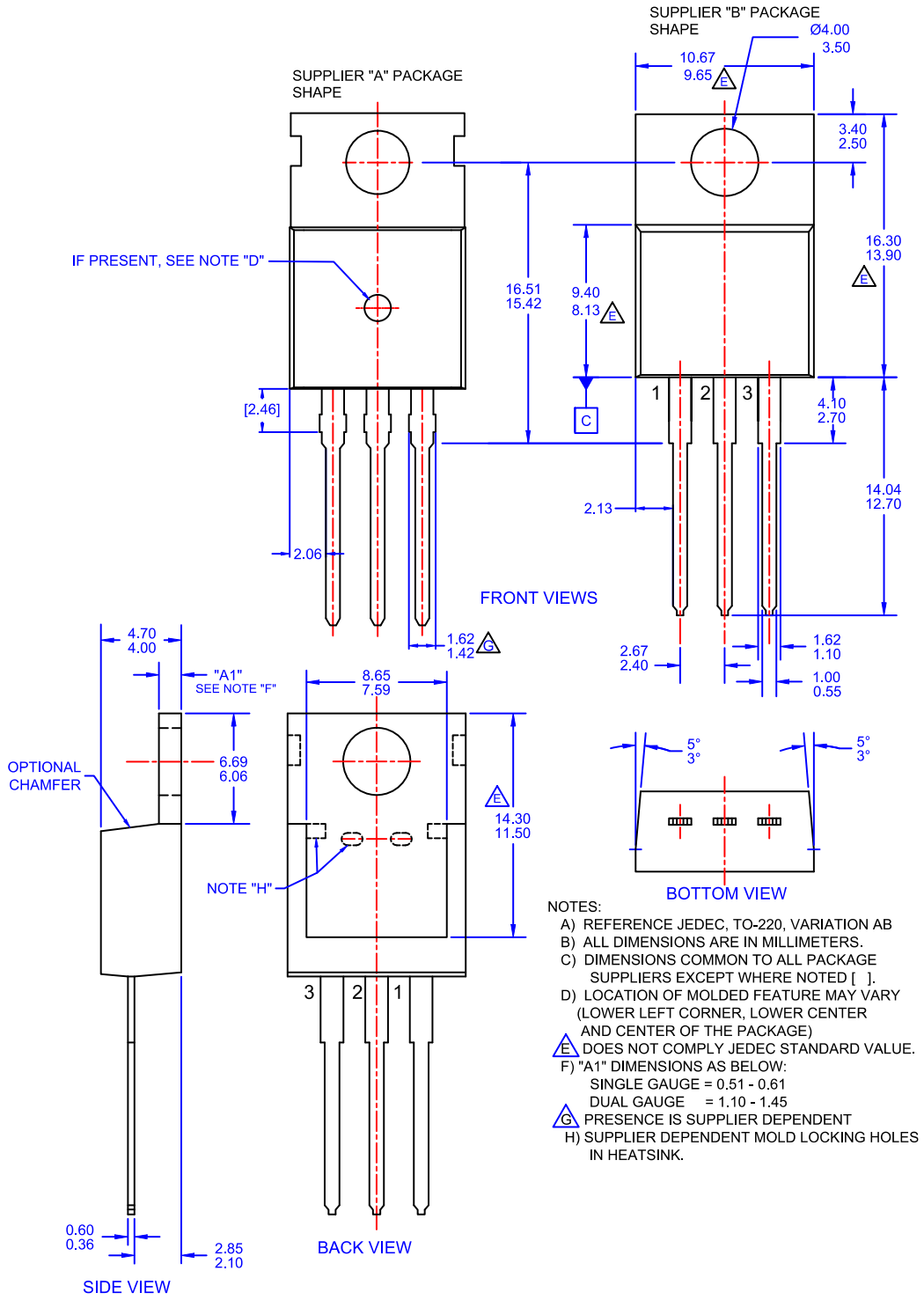
TO−220−3LD
CASE 340AT
ISSUE A

DATE 03 OCT 2017



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NEW STANDARD:			
DESCRIPTION:	**TO−220−3LD**		**PAGE 1 OF 2**

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION FROM FAIRCHILD TO220B03 TO ON SEMICONDUCTOR. REQ. BY B. NG.	30 SEP 2016
A	CHANGED NOTE I LABEL TO NOTE H IN BACK VIEW. REQ. BY H. ALLEN.	03 OCT 2017

PUBLICATION ORDERING INFORMATION

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