



ON Semiconductor®

# FQU2N50B

## N-Channel QFET® MOSFET

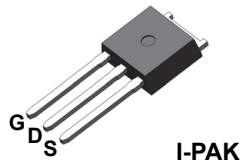
500 V, 1.6 A, 5.3 Ω

### Description

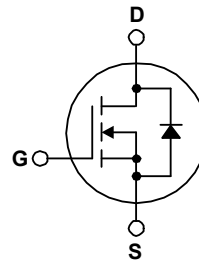
This N-Channel enhancement mode power MOSFET is produced using ON Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

### Features

- 1.6 A, 500 V,  $R_{DS(on)} = 5.3 \Omega$  (Max.) @  $V_{GS} = 10 V$ ,  $I_D = 0.8 A$
- Low Gate Charge (Typ. 6.0 nC)
- Low Crss (Typ. 4.3 pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability



I-PAK



### Absolute Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	FQU2N50BTU-WS	Units
$V_{DSS}$	Drain-Source Voltage	500	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ C$ )	1.6	A
	- Continuous ( $T_C = 100^\circ C$ )	1.0	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	6.4	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	120	mJ
$I_{AR}$	Avalanche Current (Note 1)	1.6	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	3.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ C$ ) *	2.5	W
	Power Dissipation ( $T_C = 25^\circ C$ )	30	W
	- Derate above $25^\circ C$	0.24	W/ $^\circ C$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ C$

### Thermal Characteristics

Symbol	Parameter	FQU2N50BTU_WS	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	4.17	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	110	
	Thermal Resistance, Junction to Ambient (*1 in <sup>2</sup> Pad of 2-oz Copper), Max.	50	

FQU2N50B — N-Channel QFET® MOSFET

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQU2N50BTU-WS	FQU2N50B	I-PAK	Tube	N/A	N/A	75 units

## Electrical Characteristics T<sub>c</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	500	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.48	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V	--	--	1	μA
		V <sub>DS</sub> = 400 V, T <sub>C</sub> = 125°C	--	--	10	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA

### On Characteristics

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.3	3.0	3.7	V
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 mA	3.6	4.3	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.8 A	--	4.2	5.3	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 0.8 A	--	1.3	--	S

### Dynamic Characteristics

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	180	230	pF
C <sub>oss</sub>	Output Capacitance		--	30	40	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	4	6	pF

### Switching Characteristics

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 2.1 A, R <sub>G</sub> = 25 Ω  (Note 4)	--	6	20	ns
t <sub>r</sub>	Turn-On Rise Time		--	25	60	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	10	30	ns
t <sub>f</sub>	Turn-Off Fall Time		--	20	50	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 2.1 A, V <sub>GS</sub> = 10 V  (Note 4)	--	6.0	8.0	nC
Q <sub>gs</sub>	Gate-Source Charge		--	1.3	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	3.0	--	nC

### Drain-Source Diode Characteristics and Maximum Ratings

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current	--	--	1.6	A	
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current	--	--	6.4	A	
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.6 A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2.1 A,	--	195	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> / dt = 100 A/μs	--	0.69	--	μC

#### Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. L = 85 mH, I<sub>AS</sub> = 1.6 A, V<sub>DD</sub> = 50 V, R<sub>G</sub> = 25 Ω, starting T<sub>J</sub> = 25°C.
3. I<sub>SD</sub> ≤ 2.1 A, di/dt ≤ 200 A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, starting T<sub>J</sub> = 25°C.
4. Essentially independent of operating temperature.

## Typical Characteristics

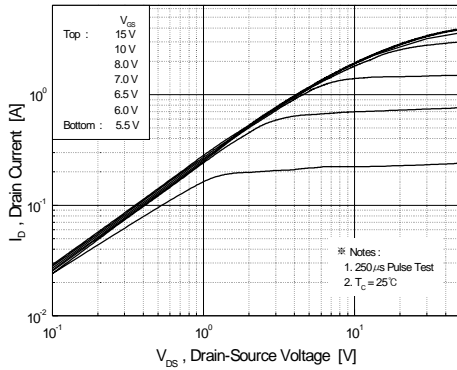


Figure 1. On-Region Characteristics

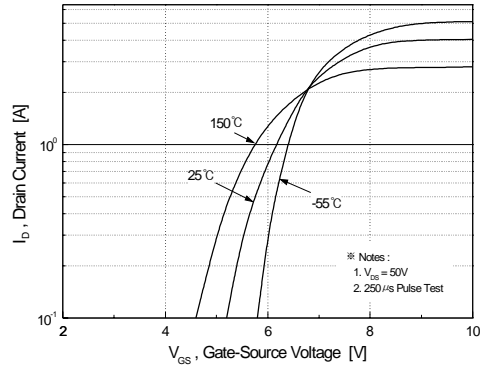


Figure 2. Transfer Characteristics

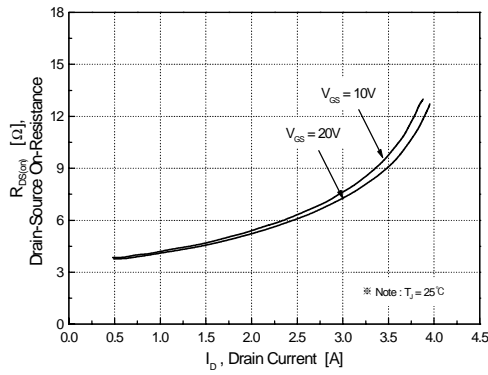


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

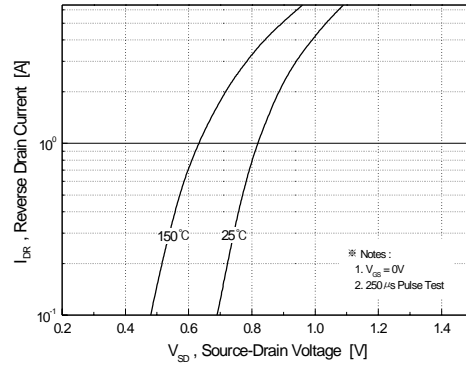


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

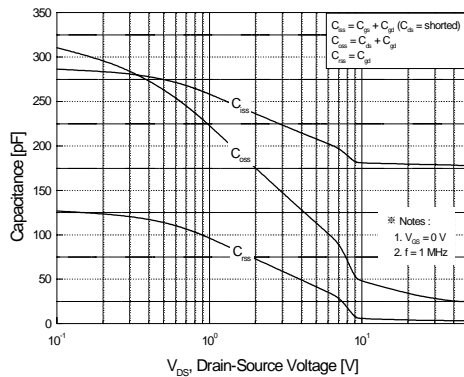


Figure 5. Capacitance Characteristics

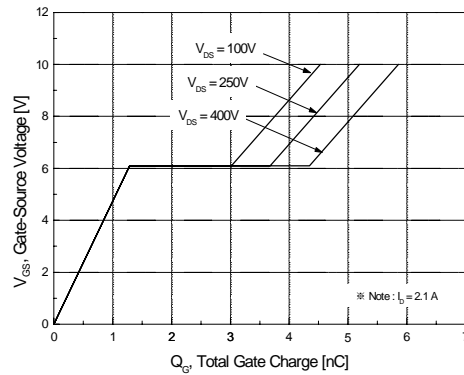
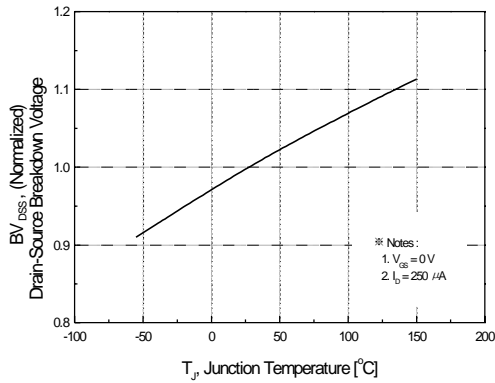
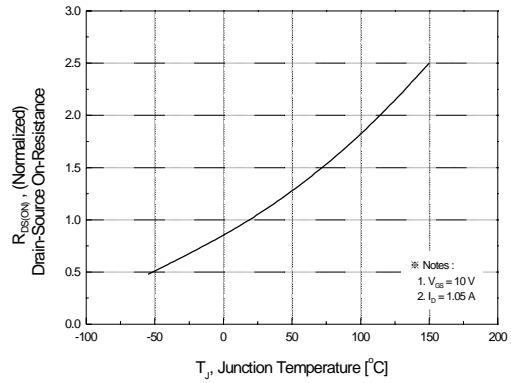


Figure 6. Gate Charge Characteristics

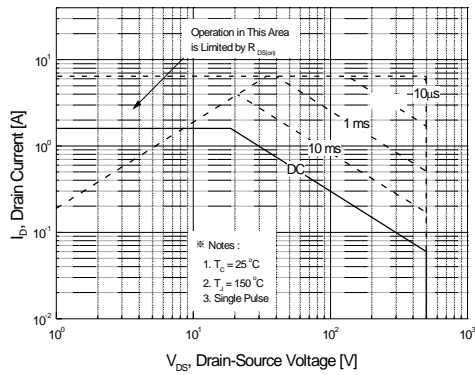
**Typical Characteristics** (Continued)



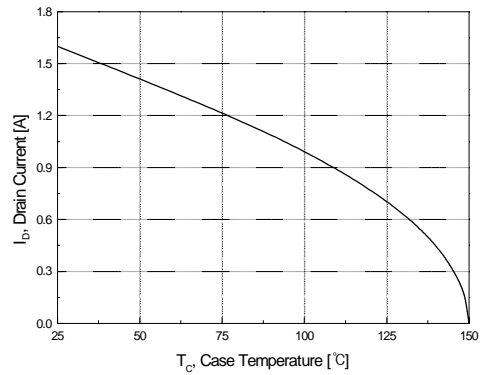
**Figure 7. Breakdown Voltage Variation vs. Temperature**



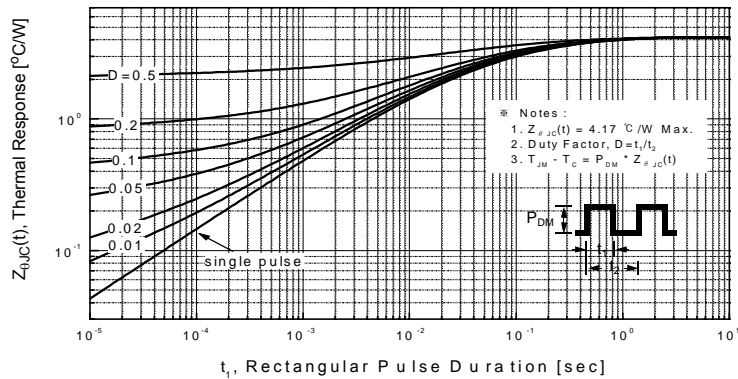
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

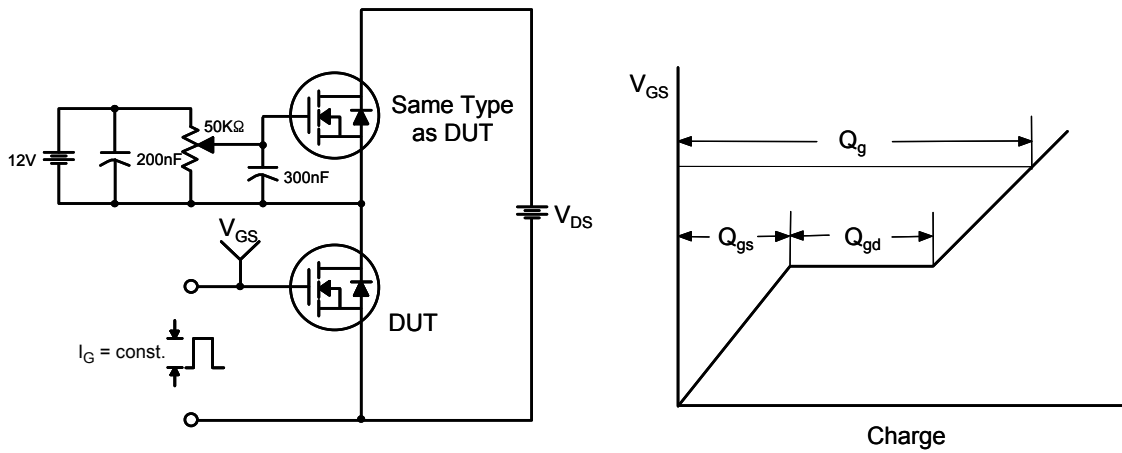


Figure 12. Gate Charge Test Circuit & Waveform

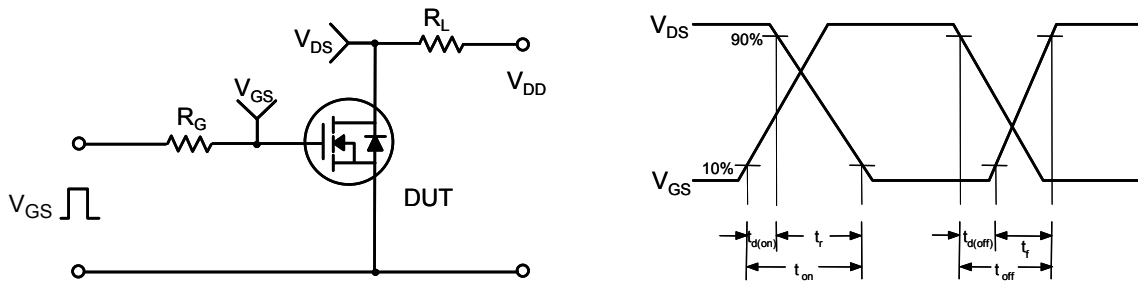


Figure 13. Resistive Switching Test Circuit & Waveforms

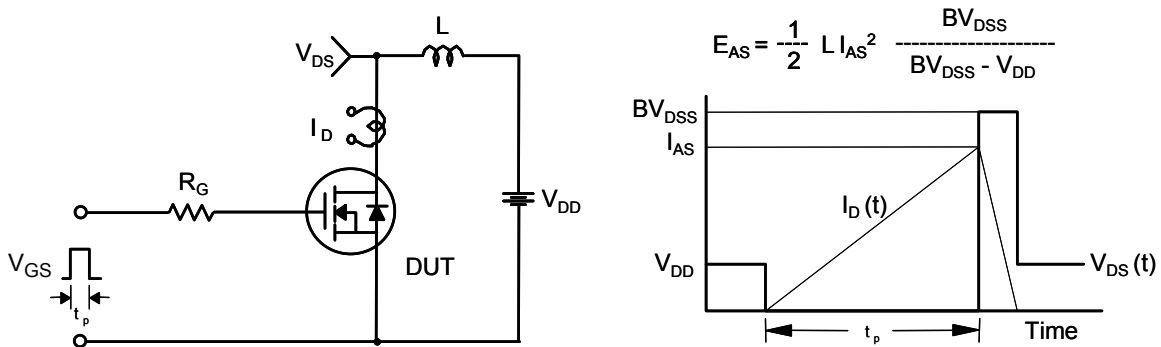


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

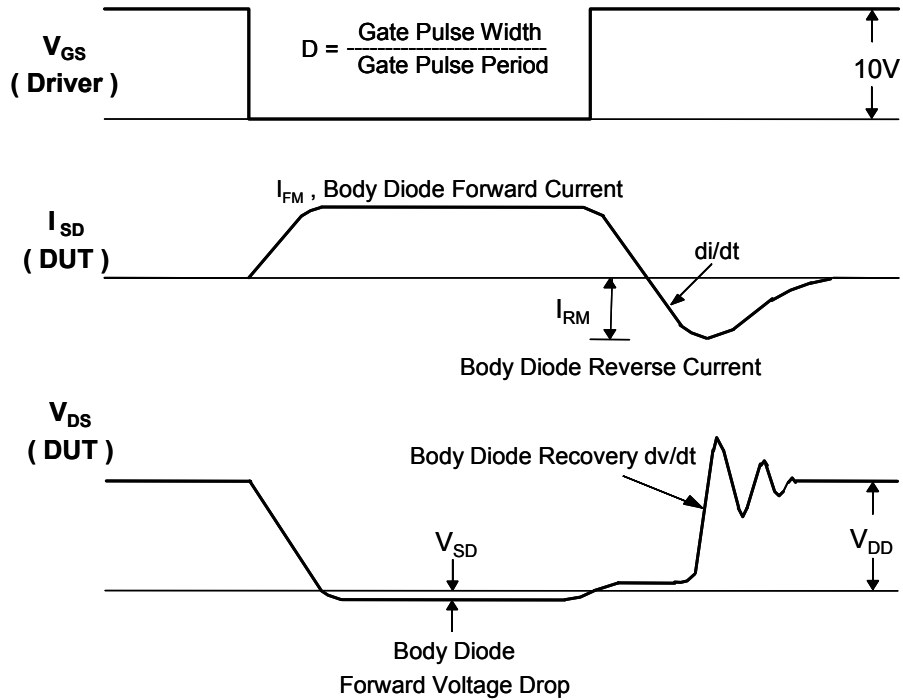
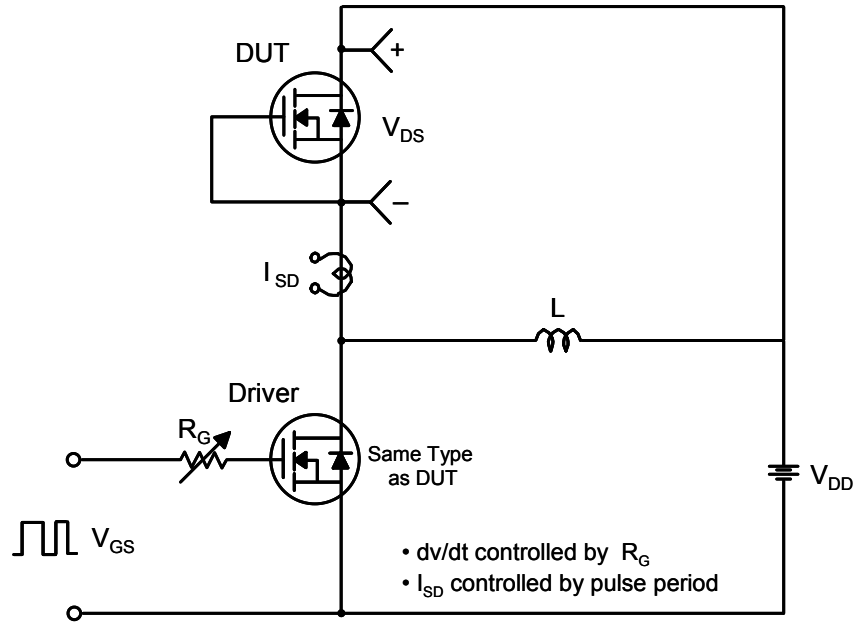
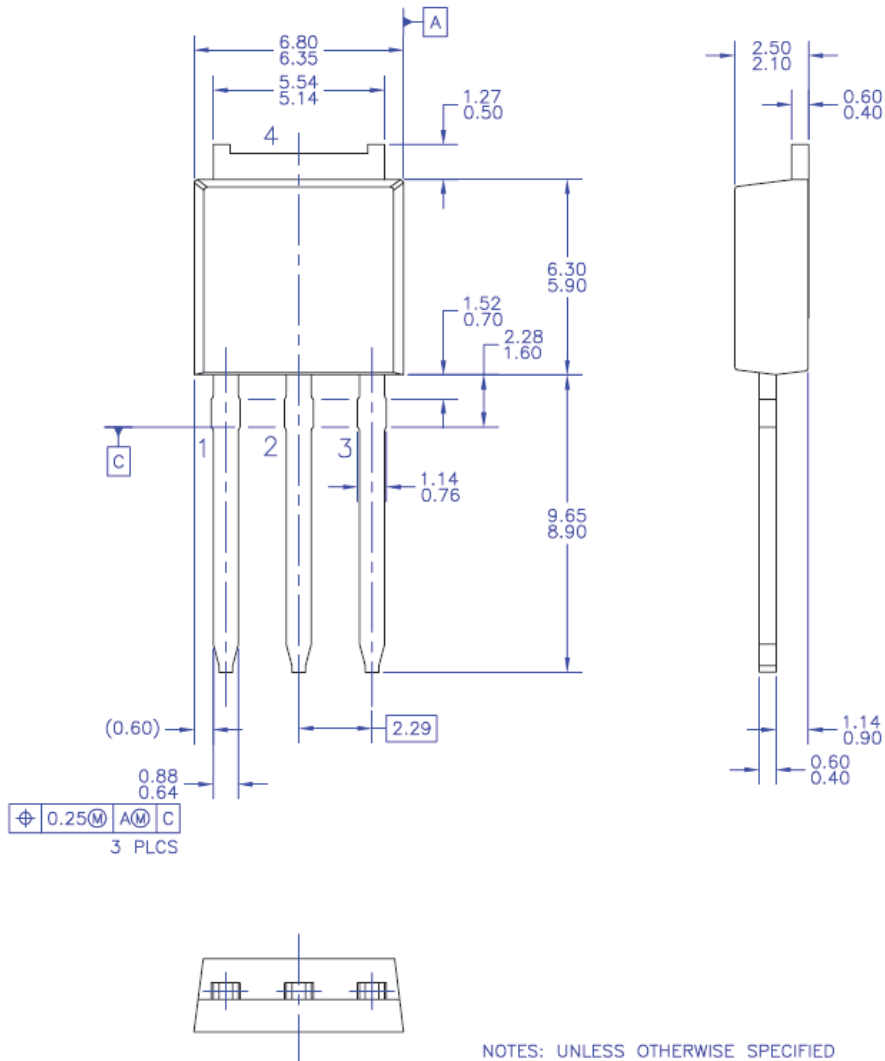


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) THIS PACKAGE CONFORMS TO JEDEC, TO-251, ISSUE C, VARIATION AA, DATED SEP 1988.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

**Figure 16. TO-251 (I-PAK), Molded, 3-Lead, Option AA**

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