# FSA646A

# 2:1 MIPI D-PHY (4.5 Gbps) 4-Data-Lane & C-PHY (3.5 Gsps) 3-Data-Lane Switch

### Description

The FSA646A can be configured as a four−data−lane MIPI, D−PHY switch or a three−data−lane MIPI, C−PHY switch. This single−pole, double−throw (SPDT) switch is optimized for switching between two high−speed or low−power MIPI sources. The FSA646A is designed for the MIPI specification and allows connection to a CSI or DSI module.

### Features

- Switch Type: SPDT (10x)
- Signal Types:
  - MIPI, D−PHY V2.1 & C−PHY V1.2
- $V_{CC}$: 1.5 to 5.0 V
- Input Signals: 0 to 1.3 V
- $R_{ON}$:
  - 6 Ω Typical HS MIPI
  - 6 Ω Typical LP MIPI
- $\Delta R_{ON}$: 0.1 Ω Typical LP & HS MIPI
- $\Delta R_{ON\_FLAT}$: 0.9 Ω Typical LP & HS MIPI
- $I_{CCZ}$: 1 μA Maximum
- $I_{CC}$: 30 μA Maximum
- $O_{IRR}$: −24 dB Typical
- Bandwidth: 4.7 GHz Typical
- Xtalk: −30 dB Typical
- $C_{ON}$: 1.4 pF Typical
- Skew (P), Skew (O): 6 ps Typical

### Applications

- Cellular Phones, Smart Phones
- Tablets
- Laptops
- Displays

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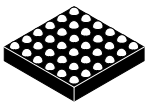


(Bottom View)

**WLCSP36,**
**2.43x2.43x0.599**
**CASE 567XH**

### MARKING DIAGRAM


GQ = Specific Device Code
KK = Assembly Lot
X = Year
Y = Work Week
Z = Assembly Location

### ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

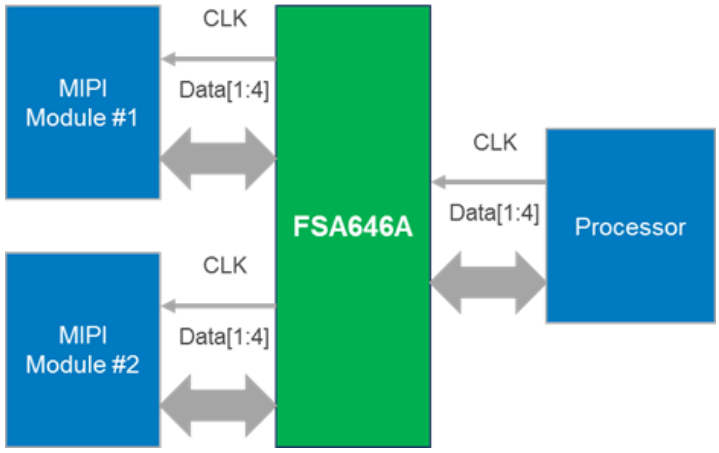
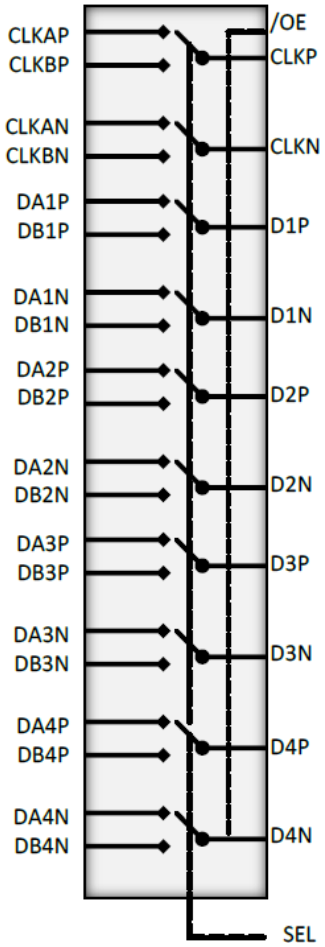



**Figure 1. Typical D−PHY Application**

## PIN DESCRIPTIONS




| Pin Name | Description | | |
|---|---|---|---|
| CLKBP/N | B Side Clock Path | | |
| DB1P/N | B Side Data Path 1 | | |
| DB2P/N | B Side Data Path 2 | | |
| DB3P/N | B Side Data Path 3 | | |
| DB4P/N | B Side Data Path 4 | | |
| CLKAP/N | A Side Clock Path | | |
| DA1P/N | A Side Data Path 1 | | |
| DA2P/N | A Side Data Path 2 | | |
| DA3P/N | A Side Data Path 3 | | |
| DA4P/N | A Side Data Path 4 | | |
| CLKP/N | Common Clock Path | | |
| D1P/N | Common Data Path 1 | | |
| D2P/N | Common Data Path 2 | | |
| D3P/N | Common Data Path 3 | | |
| D4P/N | Common Data Path 4 | | |
| /OE | Output Enable | | |
| SEL | Control Pin | SEL=0 | CLKP/N=CLKAP/N, DnP/N=DAnP/N |
| | | SEL=1 | CLKP/N=CLKBP/N, DnP/N=DBnP/N |
| VCC | Power | | |
| GND | Ground | | |
| NC | No Connect | | |

**Figure 2. Analog Symbol**

## PIN DEFINITIONS

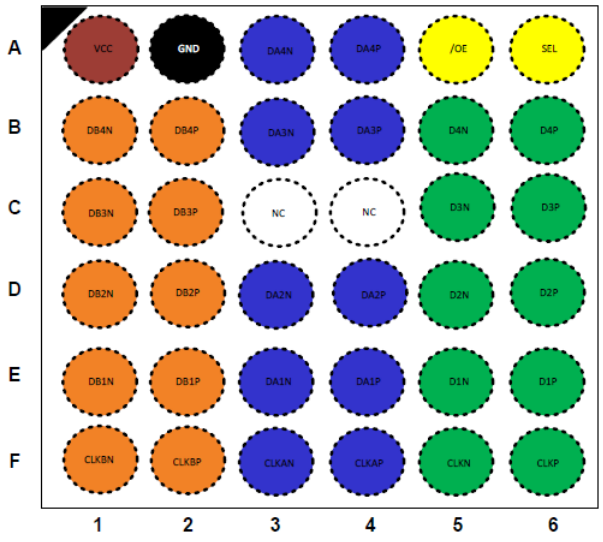



**Figure 3. Top Through View**

**Table 1. BALL−TO−PIN MAPPINGS**

| Ball | Pin Name | Ball | Pin Name | Ball | Pin Name |
|---|---|---|---|---|---|
| A1 | $V_{CC}$ | C1 | DB3N | E1 | DB1N |
| A2 | GND | C2 | DB3P | E2 | DB1P |
| A3 | DA4N | C3 | NC | E3 | DA1N |
| A4 | DA4P | C4 | NC | E4 | DA1P |
| A5 | /OE | C5 | D3N | E5 | D1N |
| A6 | SEL | C6 | D3P | E6 | D1P |
| B1 | DB4N | D1 | DB2N | F1 | CLKBN |
| B2 | DB4P | D2 | DB2P | F2 | CLKBP |
| B3 | DA3N | D3 | DA2N | F3 | CLKAN |
| B4 | DA3P | D4 | DA2P | F4 | CLKAP |
| B5 | D4N | D5 | D2N | F5 | CLKN |
| B6 | D4P | D6 | D2P | F6 | CLKP |

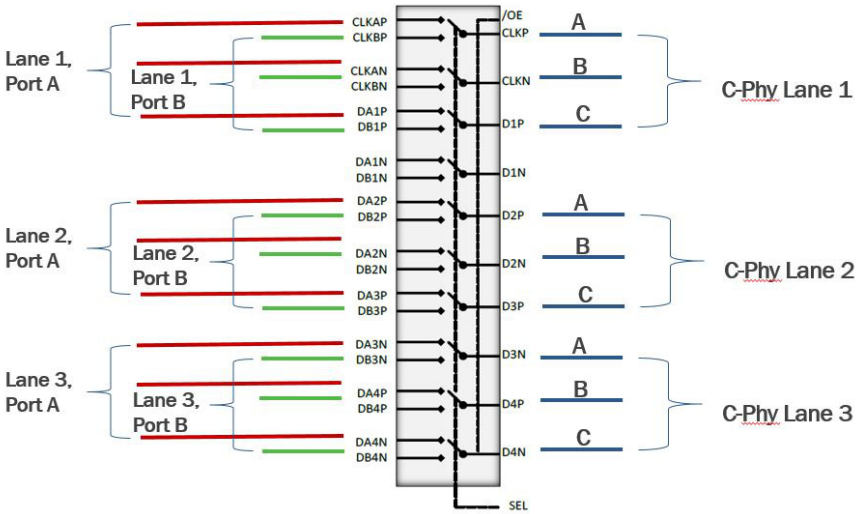



**Figure 4. Recommended Configuration for C−PHY**

### TRUTH TABLE

| SEL | /OE | Function |
|---|---|---|
| LOW | LOW | $CLK_P$ = $CLKA_P$, $CLK_N$ = $CLKA_N$, Dn(P/N) = DAn(P/N) |
| HIGH | LOW | $CLK_P$ = $CLKB_P$, $CLK_N$ = $CLKB_N$, Dn(P/N) = DBn(P/N) |
| X | HIGH | Clock and Data Ports High Impedance |

### ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | −0.5 | 6.0 | V |
| $V_{CNTRL}$ | DC Input Voltage (/OE, SEL) (Note 1) | | −0.5 | $V_{CC}$ | V |
| $V_{SW}$ | DC Switch I/O Voltage (Note 1,2) | | −0.3 | 2.1 | V |
| $I_{IK}$ | DC Input Diode Current | | −50 | | mA |
| $I_{OUT}$ | DC Output Current | | | 25 | mA |
| $T_{STG}$ | Storage Temperature | | −65 | +150 | °C |
| ESD | Human Body Model, JEDEC: JESD22−A114 | All Pins | 2.0 | | kV |
| | Charged Device Model, JEDEC: JESD22−C101 | | 0.5 | | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.
2. $V_{SW}$ refers to analog data switch paths.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 1.5 | 5.0 | V |
| $V_{CNTRL}$ | Control Input Voltage (SEL, /OE) (Note 3) | | 0 | $V_{CC}$ | V |
| $V_{SW}$ | Switch I/O Voltage (CLKn, Dn, CLKAn, CLKBn, Dan, DBn) | HS Mode | 0 | 0.425 | V |
| | | LP Mode | −0.05 | 1.3 | V |
| $T_A$ | Operating Temperature | | −40 | +85 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. The control inputs must be held HIGH or LOW; they must not float.

## DC AND TRANSIENT CHARACTERISTICS ($T_A$ = 25°C unless otherwise specified)

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = −40 to +85°C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{IK}$ | Clamp Diode Voltage (/OE, SEL) | $I_{IN}$ = −18 mA | 1.5 | −1.2 | | −0.6 | V |
| $V_{IH}$ | Input Voltage High | SEL, /OE | 1.5 to 5 | 1.3 | | | V |
| $V_{IL}$ | Input Voltage Low | SEL, /OE | 1.5 to 5 | | | 0.5 | V |
| $I_{IN}$ | Control Input Leakage (/OE, SEL) | $V_{CNTRL}$ = 0 to $V_{CC}$ | 5 | −0.5 | | 0.5 | μA |
| $I_{NO(OFF)}$ $I_{NC(OFF)}$ | Off Leakage Current of Port CLKAn, Dan, CLKBn and DBn | $V_{SW}$ = 0.0 ≤ DATA ≤ 1.3 V | 5 | −0.5 | | 0.5 | μA |
| $I_{A(ON)}$ | ON Leakage Current of Common Ports (CLKn, Dn) | $V_{SW}$ = 0.0 ≤ DATA ≤ 1.3 V | 5 | −0.5 | | 0.5 | μA |
| $I_{OFF}$ | Power−Off Leakage Current (All I/O Ports) | $V_{SW}$ = 0.0 or 1.3 V | 0 | −0.5 | | 0.5 | μA |
| $I_{OZ}$ | Off−State Leakage | $V_{SW}$ = 0.0 ≤ DATA ≤ 1.3 V /OE = High | 5 | −0.5 | | 0.5 | μA |
| $R_{ON\_MIPI\_HS}$ | Switch On Resistance for HS MIPI Applications (Note 4) | $I_{ON}$ = −8 mA, /OE = 0 V, SEL = $V_{CC}$ or 0 V, CLKA, CLKB, $DB_N$ or $DA_N$ = 0.2 V | 1.5 | | 6 | | Ω |
| | | | 2.5 | | | | |
| | | | 3.3 | | | | |
| | | | 5 | | | | |
| $R_{ON\_MIPI\_LP}$ | Switch On Resistance for LP MIPI Applications (Note 4) | $I_{ON}$ = −8 mA, /OE = 0 V, SEL = $V_{CC}$ or 0 V, CLKA, CLKB, $DB_N$ or $DA_N$ = 1.2 V | 1.5 | | 6 | | Ω |
| | | | 2.5 | | | | |
| | | | 3.3 | | | | |
| | | | 5 | | | | |
| $\Delta R_{ON\_MIPI\_HS}$ | On Resistance Matching Between HS MIPI Channels (Note 4) | $I_{ON}$ = −8 mA, /OE = 0 V, SEL = $V_{CC}$ or 0 V, CLKA, CLKB, $DB_N$ or $DA_N$ = 0.2 V | 1.5 | | 0.1 | | Ω |
| | | | 2.5 | | | | |
| | | | 3.3 | | | | |
| | | | 5 | | | | |
| $\Delta R_{ON\_MIPI\_LP}$ | On Resistance Matching Between LP MIPI Channels (Note 4) | $I_{ON}$ = −8 mA, /OE = 0 V, SEL = $V_{CC}$ or 0 V, CLKA, CLKB, $DB_N$ or $DA_N$ = 1.2 V | 1.5 | | 0.1 | | Ω |
| | | | 2.5 | | | | |
| | | | 3.3 | | | | |
| | | | 5 | | | | |

**DC AND TRANSIENT CHARACTERISTICS** ($T_A$ = 25°C unless otherwise specified) (continued)

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = −40 to +85°C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $R_{ON\_FLAT\_MIPI\_HS}$ | On Resistance Flatness for HS MIPI Signals (Note 4) | $I_{ON}$ = −8 mA, /OE = 0 V, SEL = $V_{CC}$ or 0 V, CLKA, CLKB, $DB_N$ or $DA_N$ = 0 to 0.3 V | 1.5 | | 0.9 | | Ω |
| | | | 2.5 | | | | |
| | | | 3.3 | | | | |
| | | | 5 | | | | |
| $R_{ON\_FLAT\_MIPI\_LP}$ | On Resistance Flatness for LP MIPI Signals (Note 4) | $I_{ON}$ = −8 mA, /OE = 0 V, SEL = $V_{CC}$ or 0 V, CLKA, CLKB, $DB_N$ or $DA_N$ = 0 to 1.3 V | 1.5 | | 0.9 | | Ω |
| | | | 2.5 | | | | |
| | | | 3.3 | | | | |
| | | | 5 | | | | |
| $I_{CC}$ | Quiescent Supply Current (Includes Change Pump) | $V_{SEL}$ = 0 or $V_{CC}$, $I_{OUT}$ = 0, /OE = 0 V | 5 | | | 30 | μA |
| $I_{CCZ}$ | Quiescent Supply Current (High Impedance) | $V_{SEL}$ = 0 or $V_{CC}$, $I_{OUT}$ = 0, /OE = 0 V | 5 | | | 1 | μA |
| $I_{CCT}$ | Increase in $I_{CC}$ Current Per Control Voltage and $V_{CC}$ | $V_{SEL}$ = 0 or $V_{CC}$, /OE = 1.5 V | 5 | | 1 | | μA |

4. Measured by the voltage drop at the indicated current through the switch.

**AC ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 3.3 V and $T_A$ = 25°C unless otherwise specified)

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = −40 to +85°C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $t_{INIT}$ | Initialization Time $V_{CC}$ to Output (Note 5) | $R_L$ = 50 Ω, $C_L$ = 0 pF, $V_{SW}$ = 0.6 V | 1.5 to 5 | | 60 | | μs |
| $t_{EN}$ | Enable Time /OE to Output | $R_L$ = 50 Ω, $C_L$ = 0 pF, $V_{SW}$ = 0.6 V | 1.5 to 5 | | 60 | 150 | μs |
| $t_{DIS}$ | Disable Time /OE to Output | $R_L$ = 50 Ω, $C_L$ = 0 pF, $V_{SW}$ = 0.6 V | 1.5 to 5 | | 35 | 250 | ns |
| $t_{ON}$ | Turn−On Time SEL to Output | $R_L$ = 50 Ω, $C_L$ = 0 pF, $V_{SW}$ = 0.6 V | 1.5 to 5 | | 350 | 1100 | ns |
| $t_{OFF}$ | Turn−Off Time SEL to Output | $R_L$ = 50 Ω, $C_L$ = 0 pF, $V_{SW}$ = 0.6 V | 1.5 to 5 | | 125 | 800 | ns |
| $t_{BBM}$ | Break−Before−Make Time | $R_L$ = 50 Ω, $C_L$ = 0 pF, $V_{SW}$ = 0.6 V | 1.5 to 5 | 50 | | 450 | ns |
| $t_{PD}$ | Propagation Delay (Note 5) | $C_L$ = 0 pF, $R_L$ = 50 Ω | 1.5 to 5 | 30 | 67 | 100 | ps |
| $O_{IRR}$ | Off Isolation for MIPI (Note 5) | $R_L$ = 50 Ω, f = 2250 MHz, /OE = HIGH, $V_{SW}$ = 0.2 $V_{PP}$ | 1.5 to 5 | | −24 | | dB |
| $X_{TALK}$ | Crosstalk for MIPI (Note 5) | $R_L$ = 50 Ω, f = 2250 MHz, SEL = High, $V_{SW}$ = 0.2 $V_{PP}$ | 1.5 to 5 | | −30 | −25 | dB |
| | | $R_L$ = 50 Ω, f = 2250 MHz, SEL = Low, $V_{SW}$ = 0.2 $V_{PP}$ | | | −30 | −25 | |
| BW | −3 db Bandwidth (Note 5) | $R_L$ = 50 Ω, $C_L$ = 0 pF, $V_{SW}$ = 0.2 $V_{PP}$ | 1.5 to 5 | | 4.7 | | GHz |
| IL | Insertion Loss at 750 MHz (Note 5) | $R_L$ = 50 Ω, $C_L$ = 0 pF, $V_{SW}$ = 0.2 $V_{PP}$ | 1.5 to 5 | | −0.7 | | dB |

5. Guaranteed by characterization.

## HIGH−SPEED−RELATED AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = −40 to +85°C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $t_{SK(P)}$ | HS Mode Skew of Opposite Transitions of the Same Output (Note 6) | $R_L$ = 50 Ω, $C_L$ = 0 pF, $V_{SW}$ = 0.3 V | 1.5 to 5 | | 6 | | ps |
| $t_{SK(O)}$ | HS Mode Skew of Channel−to−Channel Single−Ended Skew (Note 6) | $R_L$ = 50 Ω, $C_L$ = 0 pF, $V_{SW}$ = 0.3 V | 1.5 to 5 | | 6 | | ps |

6. Guaranteed by characterization.

## CAPACITANCE

| Symbol | Parameter | Conditions | $T_A$ = −40 to +85°C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $C_{IN}$ | Control Pin Input Capacitance (Note 7) | $V_{CC}$ = 0 V, f = 1 MHz | | 2.1 | | pF |
| $C_{ON}$ | On Capacitance (Note 7) | $V_{CC}$ = 3.3 V, /OE = 0 V, f = 2250 MHz (in HS common value) | | 1.4 | | |
| $C_{OFF}$ | On Capacitance (Note 7) | $V_{CC}$ and /OE = 3.3 V, f = 2250 MHz (both sides in HS common value) | | 0.9 | | |

7. Guaranteed by characterization.

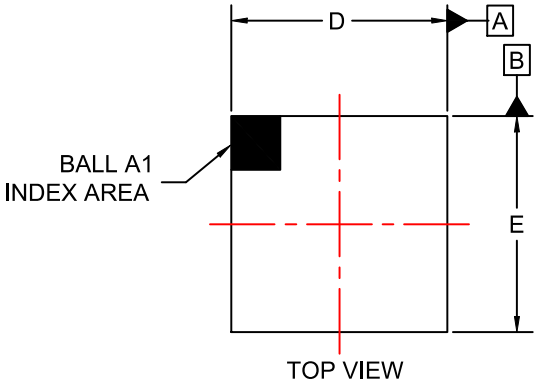
The table below pertains to the Packaging information on the following page.

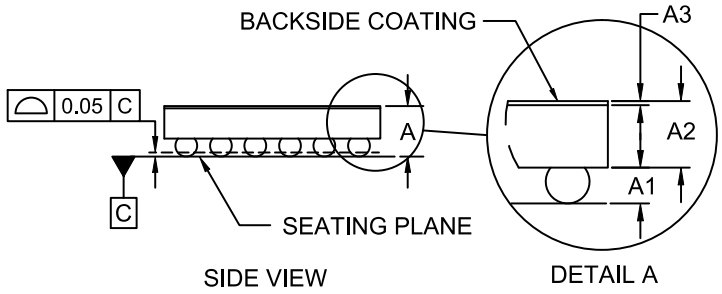
## ORDERING INFORMATION

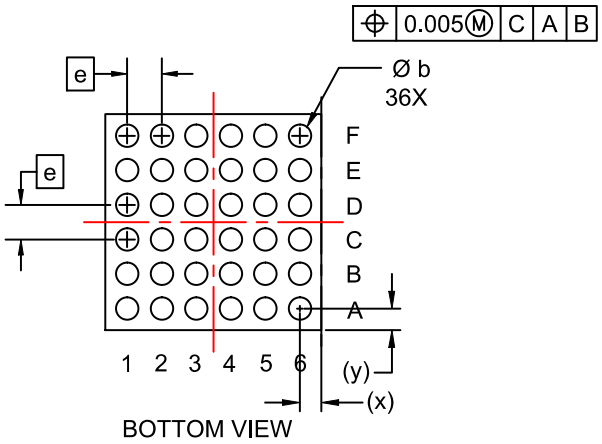
| Part Number | Top Marking | Temperature Range | Package |
|---|---|---|---|
| FSA646AUCX | GQ | −40 to +85°C | 36−Ball WLCSP, Non−JEDEC 2.43 x 2.43 mm, 0.4 mm Pitch |

## PACKAGE DIMENSIONS

**WLCSP36 2.43x2.43x0.599**
CASE 567XH
ISSUE O



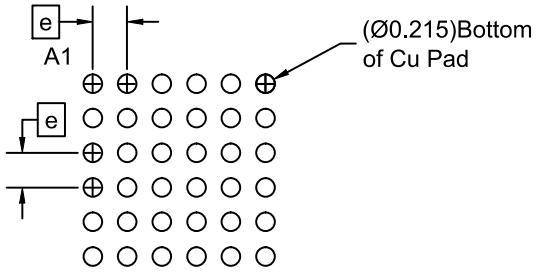




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.561 | 0.599 | 0.637 |
| A1 | 0.174 | 0.194 | 0.214 |
| A2 | 0.362 | 0.380 | 0.398 |
| A3 | 0.022 | 0.025 | 0.028 |
| b | 0.240 | 0.260 | 0.280 |
| D | 2.400 | 2.430 | 2.460 |
| E | 2.400 | 2.430 | 2.460 |
| e | 0.40 BSC | | |
| x | 0.200 | 0.215 | 0.230 |
| y | 0.200 | 0.215 | 0.230 |




RECOMMENDED MOUNTING FOOTPRINT
(NSMD PAD TYPE)



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