ON Semiconductor®

FSDL0165RN
Green-Mode Power Switch

Features

- Internal Avalanche-Rugged SenseFET
- Consumes only 0.65W at 240V$_{AC}$ and 0.3W Load with Advanced Burst-Mode Operation
- Frequency Modulation for EMI Reduction
- Precision Fixed Operating Frequency
- Internal Startup Circuit
- Pulse-by-Pulse Current Limiting
- Abnormal Over-Current Protection (AOCP)
- Over-Voltage Protection (OVP)
- Overload Protection (OLP)
- Internal Thermal Shutdown Function (TSD)
- Auto-Restart Mode
- Under-Voltage Lockout (UVLO)
- Low Operating Current: 3mA
- Adjustable Peak Current Limit
- Built-in Soft-Start

Applications

- SMPS for VCR, SVR, STB, DVD, & DVCD Players
- SMPS for Printers, Facsimiles, & Scanners
- Adapter for Camcorders

Description

The FSDL0165RN consists of an integrated Pulse Width Modulator (PWM) and SenseFET, specifically designed for high-performance offline Switch-Mode Power Supplies (SMPS) with minimal external components. This device is an integrated high-voltage power switching regulator that combines an avalanche-rugged SenseFET with a Current-Mode PWM control block. The integrated PWM controller features include a fixed oscillator with frequency modulation for reduced EMI, Under-Voltage Lockout (UVLO) protection, Leading-Edge Blanking (LEB), an optimized gate turn-on/turn-off driver, Thermal Shutdown (TSD) protection, Abnormal Over-Current Protection (AOCP), and temperature-compensated precision current sources for loop compensation and fault protection circuitry.

Compared to a discrete MOSFET and controller or RCC switching converter solution, the FSDL0165RN reduces total component count, design size, and weight while increasing efficiency, productivity, and system reliability. This device provides a basic platform for design of cost-effective flyback converters.

Related Resources

- *https://www.onsemi.com/pub/Collateral/AN-4134.PDF*
- *http://www.onsemi.com/pub/Collateral/AN-4137.pdf.pdf*
- *http://www.onsemi.com/pub/Collateral/AN-4140.pdf.pdf*
- *http://www.onsemi.com/pub/Collateral/AN-4141.pdf.pdf*
- *http://www.onsemi.com/pub/Collateral/AN-4148.pdf.pdf*

Ordering Information

Part Number	Package	Marking Code	BV_{DSS}	f_{OSC}	$R_{DS(ON)(MAX)}$
FSDL0165RN	8-Lead, Dual Inline Package (DIP)	DL0165R	650V	50KHz	8.0Ω

October-2017, Rev. 2

Publication Order Number:
FSDL0165RN/D

Application Circuit

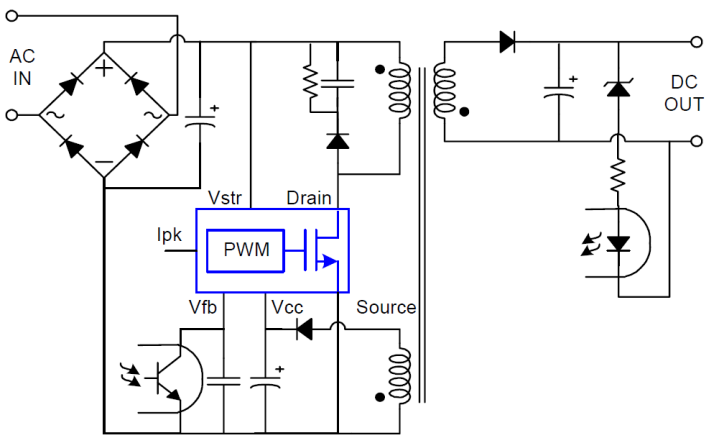


Figure 1. Typical Application Circuit

Table 1. Output Power Table

Product	230V$_{AC}$ ±15%[1]		85-265V$_{AC}$	
	Adapter[1]	Open Frame[2]	Adapter[1]	Open Frame[2]
FSDL321	11W	17W	8W	12W
FSDH321	11W	17W	8W	12W
FSDH321L	11W	17W	8W	12W
FSDL0165RN	13W	23W	11W	17W
FSDH0265RN	16W	27W	13W	20W

Notes:

1. Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sink, measured at 50°C ambient temperature.
2. Maximum practical continuous power in an open-frame design with sufficient drain pattern as a heat sink, measured at 50°C ambient temperature.
3. 230V$_{AC}$ or 100/115V$_{AC}$ with voltage doubler.

Internal Block Diagram

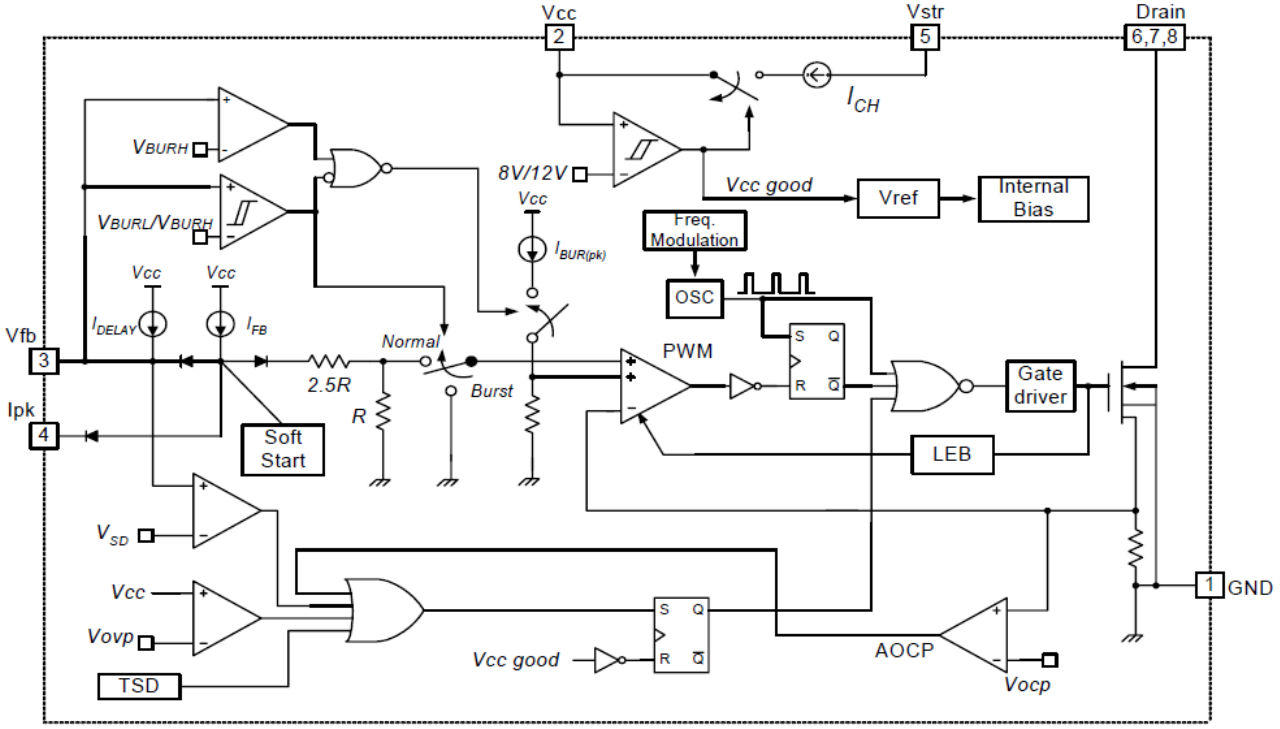


Figure 2. Internal Block Diagram

Pin Configuration

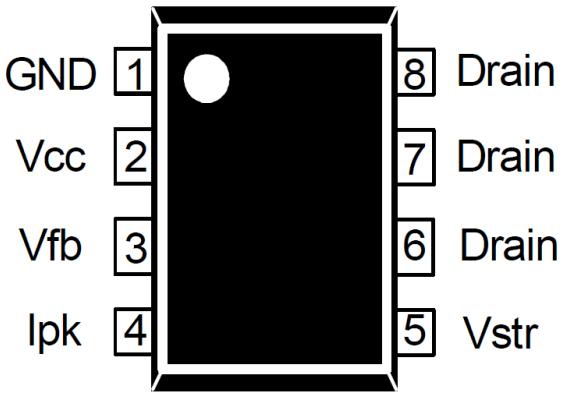


Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	GND	SenseFET source terminal on primary side and internal control ground.
2	Vcc	Positive Supply Voltage Input. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (Vstr) via an internal switch during startup (*see Figure 2*). When V_{CC} reaches the UVLO upper threshold (12V), the internal startup switch opens and device power is supplied via the auxiliary transformer winding.
3	Vfb	The feedback voltage pin is the non-inverting input to the PWM comparator. It has a 0.9mA current source connected internally, while a capacitor and optocoupler are typically connected externally. A feedback voltage of 6V triggers overload protection. There is a delay while charging external capacitor C_{fb} from 3V to 6V using an internal 5μA current source. This delay prevents false triggering under transient conditions, but allows the protection mechanism to operate under true overload conditions.
4	Ipk	This pin adjusts the peak current limit of the SenseFET. The feedback 0.9mA current source is diverted to the parallel combination of an internal 2.8kΩ resistor and any external resistor to GND on this pin to determine the peak current limit. If this pin is tied to V_{CC} or left floating, the typical peak current limit is 1.2A.
5	Vstr	This pin connects directly to the rectified AC line voltage source. At startup, the internal switch supplies internal bias and charges an external storage capacitor placed between the Vcc pin and ground. Once the V_{CC} reaches 12V, the internal switch is opened.
6, 7, 8	Drain	The drain pins are designed to connect directly to the primary lead of the transformer and are capable of switching a maximum of 650V. Minimizing the length of the trace connecting these pins to the transformer decreases leakage inductance.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{DS}	Drain Pin Voltage		650	V
V_{STR}	V_{STR} Pin Voltage		650	V
I_{DM}	Drain Current Pulsed[4]		4	A
E_{AS}	Single Pulsed Avalanche Energy[5]		95	mJ
V_{CC}	Supply Voltage		20	V
V_{FB}	Feedback Pin Voltage	-0.3	V_{CC}	V
P_D	Total Power Dissipation (T_C=25°C)		1.5	W
T_J	Operating Junction Temperature		Internally Limited	°C
T_A	Operating Ambient Temperature	-25	+85	°C
T_{STG}	Storage Temperature	-55	+150	°C

Notes:

4. Repetitive rating: pulse width is limited by maximum junction temperature.
5. L=51mH, starting T_J=25°C.

Thermal Impedance

T_A=25°C unless otherwise specified.

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Impedance[6,9]	83.33	°C/W
θ_{JC}	Junction-to-Case Thermal[7,9]	17.80	°C/W
Ψ_{JT}	Junction-to-Top Thermal Impedance[8,9]	36.57	°C/W

Notes:

6. Free standing with no heatsink; without copper clad. Measurement condition; just before junction temperature T_J enters into OTP.
7. Measured on the DRAIN pin close to plastic interface.
8. Measured on the package top surface.
9. Test standards: JESD 51-2 and 51-10 (DIP).

Electrical Characteristics

T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SenseFET Section						
I_{DSS}	Zero-Gate-Voltage Drain Current	V_{DS}=650V, V_{GS}=0V			50	μA
		V_{DS}=520V, V_{GS}=0V, T_C=125°C			200	
$R_{DS(ON)}$	Drain-Source On-State Resistance[10]	V_{GS}=10V, I_D=0.5A		8	10	Ω
C_{ISS}	Input Capacitance	V_{GS}=0V, V_{DS}=25V, f=1MHz		250		pF
C_{OSS}	Output Capacitance	V_{GS}=0V, V_{DS}=25V, f=1MHz		25		pF
C_{RSS}	Reverse Transfer Capacitance	V_{GS}=0V, V_{DS}=25V, f=1MHz		10		pF
t_r	Rise Time	V_{DS}=325V, I_D=1.0A		4		ns
t_f	Fall Time	V_{DS}=325V, I_D=1.0A		10		ns
$t_{d(on)}$	Turn-On Delay	V_{DS}=325V, I_D=1.0A		12		ns
$t_{d(off)}$	Turn-Off Delay	V_{DS}=325V, I_D=1.0A		30		ns
Control Section						
f_{OSC}	Switching Frequency		45	50	55	kHz
Δf_{ODM}	Switching Frequency Modulation		±1.0	±1.5	±2.0	kHz
Δf_{OSC}	Switching Frequency Variation[11]	−25°C < T_A < 85°C		±5	±10	%
D_{MAX}	Maximum Duty Cycle		71	77	83	%
D_{MIN}	Minimum Duty Cycle		0	0	0	%
V_{START}	UVLO Threshold Voltage	V_{FB}=GND	11	12	13	V
V_{STOP}			7	8	9	V
I_{FB}	Feedback Source Current	V_{FB}=GND	0.7	0.9	1.1	A
t_{SS}	Internal Soft-Start Time	V_{STR}=4V	10	15	20	ms
Burst-Mode Section						
V_{BURH}	Burst-Mode Voltage		0.5	0.6	0.7	V
V_{BURL}			0.25	0.35	0.45	V
Protection Section						
I_{LIM}	Peak Drain Current Limit	Maximum Inductor Current	1.06	1.20	1.35	A
t_{CLD}	Current Limit Delay[12]			500		ns
TSD	Thermal Shutdown Temperature		125	140		°C
V_{SD}	Shutdown Feedback Voltage		5.5	6.0	6.5	V
V_{OVP}	Over-Voltage Protection		18	19		V
I_{DELAY}	Shutdown Delay Current	V_{FB}=4V	3.5	5.0	6.5	μA
t_{LEB}	Leading-Edge Blanking Time		200			ns
Total Device Section						
I_{OP}	Operating Supply Current, (Control Part)	V_{CC}=14V	1	3	5	mA
I_{CH}	Startup Charging Current	V_{CC}=0V, R_{STR} < 100kohm[13]	0.70	0.85	1.00	mA
V_{STR}	V_{STR} Supply Voltage	V_{CC}=0V	35			mA

Notes:

10. Pulse test: pulse width ≤ 300us, duty ≤ 2%
11. These parameters, although guaranteed, are tested in EDS (wafer test) process
12. These parameters, although guaranteed, are not 100% tested in production.
13. R_{STR} is connected between the rectified AC line voltage source and V_{STR} pin.

Comparison of KA5x0165RN and FSDL0165RN

Function	KA5x0165RN	FSDL0165RN	FSDL0165RN Advantages
Soft-Start	Not Applicable	15ms	▪ Gradually increasing current limit during soft-start further reduces peak current and voltage stresses ▪ Eliminates external components used for soft-start in most applications ▪ Reduces or eliminates output overshoot
External Current Limit	Not Applicable	Programmable of Default Current Limit	▪ Smaller transformer ▪ Allows power limiting (constant overload power) ▪ Allows use of larger device for lower losses and higher efficiency
Frequency Modulation	Not Applicable	±1.5KHz at 50KHz	▪ Reduces conducted EMI
Bust Mode Operation	Not Applicable	Built into Controller	▪ Improves light load efficiency ▪ Reduces power consumption at no load ▪ Transformer audible noise reduction
Drain Creepage at Package	1.02mm	7.62mm	▪ Greater immunity to arcing provoked by dust, debris, and other contaminants

Typical Performance Characteristics (Control Part)

Characteristic graphs are normalized at T_A=25°C.

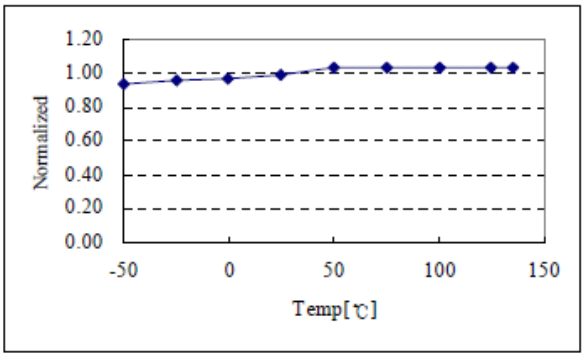


Figure 4. Operating Frequency (f_{OSC}) vs. T_A

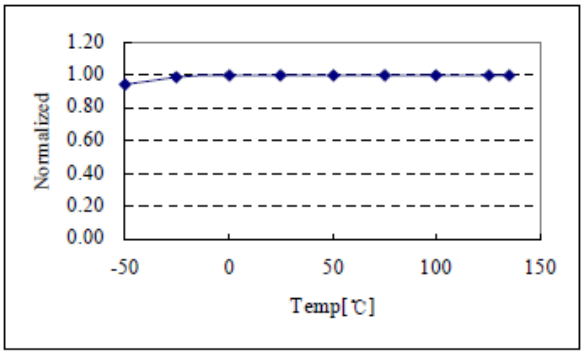


Figure 5. Frequency Modulation (Δf_{MOD}) vs. T_A

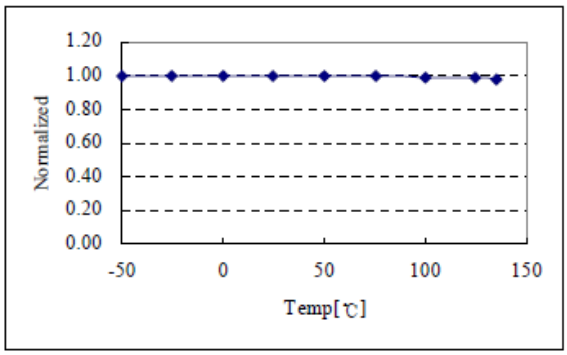


Figure 6. Maximum Duty Cycle (D_{MAX}) vs. T_A

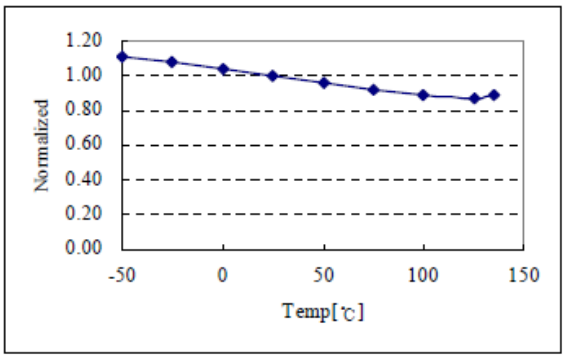


Figure 7. Operating Supply Current (I_{OP}) vs. T_A

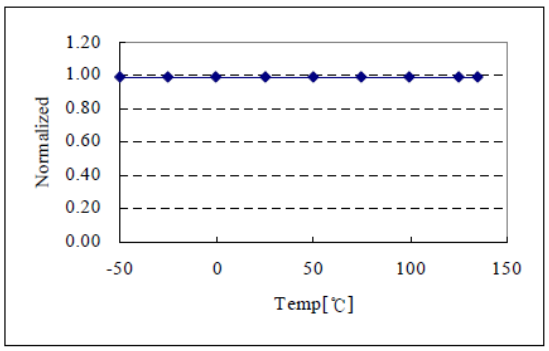


Figure 8. Start Threshold Voltage (V_{START}) vs. T_A

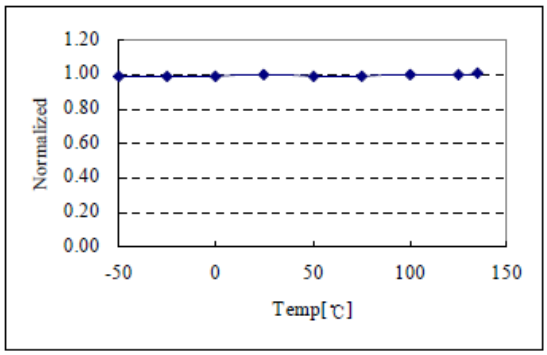


Figure 9. Stop Threshold Voltage (V_{STOP}) vs. T_A

Typical Performance Characteristics (Control Part)

Characteristic graphs are normalized at T_A=25°C.

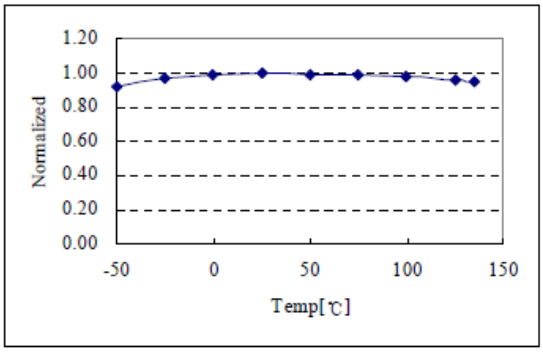


Figure 10. Feedback Source Current (I_{FB}) vs. T_A

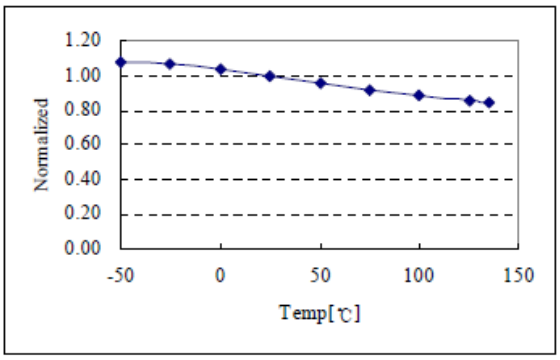


Figure 11. Startup Charging Current (I_{CH}) vs. T_A

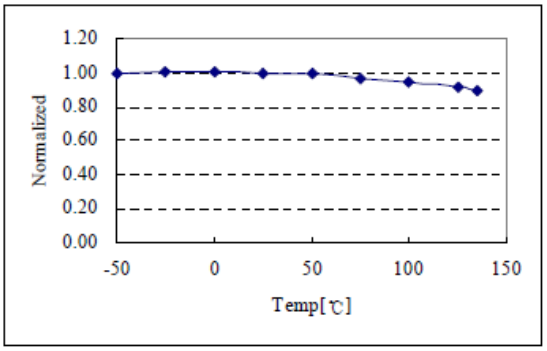


Figure 12. Peak Current Limit (I_{LIM}) vs. T_A

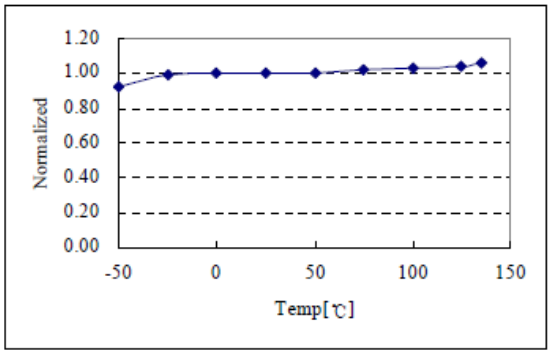


Figure 13. Burst Peak Current ($I_{BUR(pk)}$) vs. T_A

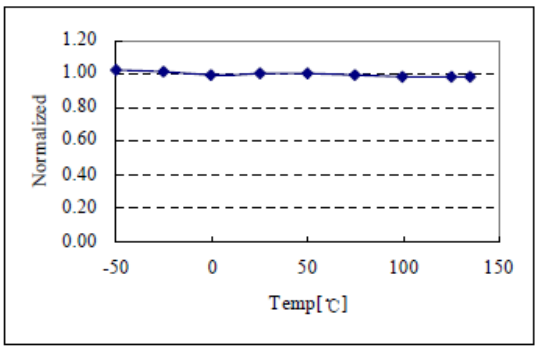


Figure 14. Over-Voltage Protection (V_{OVP}) vs. T_A

Functional Description

1. Startup: In previous generations of Power Switches, the Vstr pin had an external resistor to the DC input voltage line. In this generation, the startup resistor is replaced by an internal high-voltage current source and a switch that shuts off when 15ms goes by after the supply voltage, V_{CC}, gets above 12V. The source turns back on if V_{CC} drops below 8V.

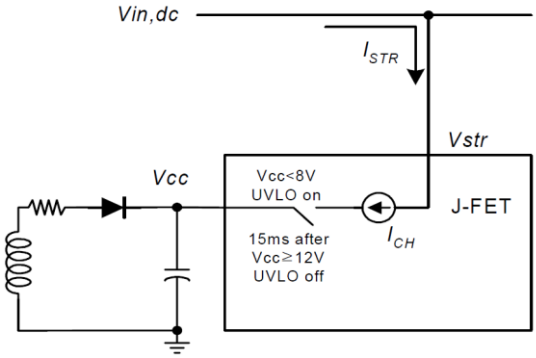


Figure 15. High-Voltage Current Source

2. Feedback Control: The FSDL0165RN employs Current-Mode control, as shown in Figure 16. An opto-coupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{SENSE} resistor, plus an offset voltage, makes it possible to control the switching duty cycle. When the shunt regulator reference pin voltage exceeds the internal reference voltage of 2.5V; the opto-coupler LED current increases, the feedback voltage V_{FB} is pulled down, and it reduces the duty cycle. This event typically occurs when the input voltage is increased or the output load is decreased.

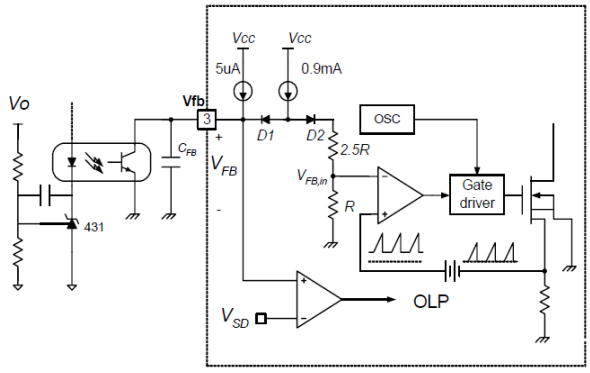
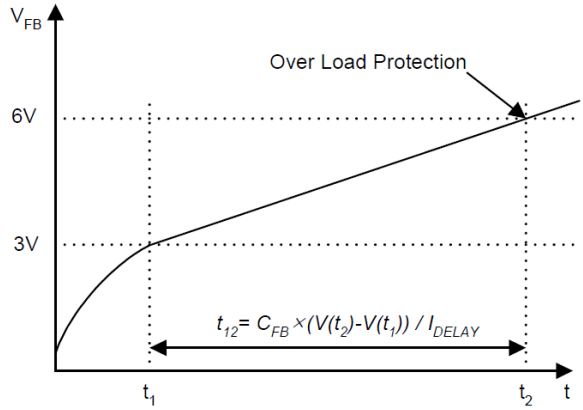


Figure 16. Pulse Width Modulation (PWM) Circuit

3. Leading-Edge Blanking (LEB): At the instant the internal SenseFET is turned on, the primary-side capacitance and secondary-side rectifier diode reverse recovery typically cause a high-current spike through the SenseFET. Excessive voltage across the R_{SENSE} resistor leads to incorrect feedback operation in the Current-Mode PWM control. To counter this effect, the power switch employs a Leading-Edge Blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (t_{LEB}) after the SenseFET is turned on.

4. Protection Circuits: The Power Switch several protective functions includes Overload Protection (OLP), Over-Voltage Protection (OVP), Abnormal Over-Current Protection (AOCP), Under-Voltage Lockout (UVLO), and Thermal Shutdown (TSD). Because these protection circuits are fully integrated inside the IC without external components, reliability is improved without increasing cost. Once a fault condition occurs, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} reaches the UVLO stop voltage V_{STOP} (8V), the protection is reset and the internal high-voltage current source charges the V_{CC} capacitor via the Vstr pin. When V_{CC} reaches the UVLO start voltage, V_{START} (12V); the Power Switch resumes normal operation. In this manner, the auto-restart alternately enables and disables the switching of the power SenseFET until the fault condition is eliminated.

4.1 Overload Protection (OLP): Overload is defined as the load current exceeding a pre-set level due to an unexpected event. In this situation, the protection circuit activates to protect the SMPS. However, when the SMPS is operating normally, the OLP circuit can be activated during the load transition. To avoid this undesired operation, the OLP circuit is designed to be activated after a specified time to determine transient situation or true overload situations. In conjunction with the IPK current limit pin (if used), the Current-Mode feedback path would limit the current in the SenseFET when the maximum PWM duty cycle is attained. If the output consumes more than this maximum power, the output voltage (V_O) decreases below its rated voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 3V, the feedback input diode is blocked and the 5μA current source (I_{DELAY}) starts to charge C_{fb} slowly up to V_{CC}. In this condition, V_{FB} increases until it reaches 6V, when the switching operation is terminated, as shown in Figure 17. The shutdown delay is the time required to charge C_{fb} from 3V to 6V with 5μA current source.



$$t_{12} = C_{FB}\frac{V(t_2)-V(t_1)}{I_{DELAY}};\quad I_{DELAY} = 5\mu A, V(t_1) = 3V, V(t_2) = 6V$$

Figure 17. Overload Protection

4.2 Thermal Shutdown (TSD): The SenseFET and the control IC are integrated, making it easier for the control IC to detect the temperature of the SenseFET. When the temperature exceeds approximately 140°C, thermal shutdown is activated.

4.3 Abnormal Over-Current Protection (AOCP): Even though the power switch has overload protection and Current-Mode PWM feedback, these are not enough to protect the power switch when a secondary-side diode short or a transformer pin short occurs. In addition to startup, soft-start is also activated at each restart attempt during auto-restart and when restarting after latch mode is activated. The power switch has an internal Abnormal Over-Current Protection (AOCP) circuit, as shown in Figure 18. When the gate turn-on signal is applied to the power SenseFET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is then compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, pulse-by-pulse AOCP is triggered regardless of uncontrollable LEB time. Pulse-by-pulse AOCP stops the SenseFET within 350ns after it is activated.

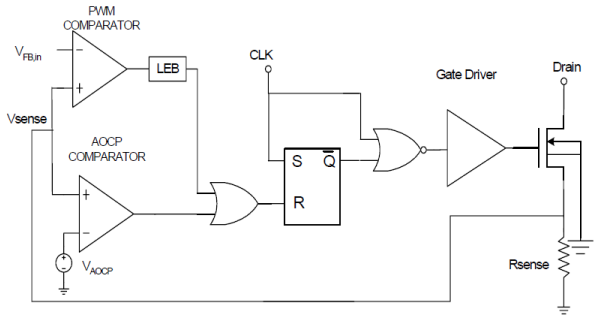


Figure 18. Abnormal Over-Current Protection

4.4 Over Voltage Protection (OVP): In the event of a malfunction in the secondary-side feedback circuit or an open feedback loop caused by a soldering defect, the current through the opto-coupler transistor becomes almost zero (*refer to Figure 16*). Then V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection is activated. Because excess energy is provided to the output, the output voltage may exceed the rated voltage before the overload protection is activated, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an over-voltage protection (OVP) circuit is employed. In general, V_{CC} is proportional to the output voltage and the power switch uses V_{CC} instead of directly monitoring the output voltage. If V_{CC} exceeds 19V, the OVP circuit is activated, resulting in termination of the switching operation. To avoid undesired activation of OVP during normal operation, V_{CC} should be properly designed to be below 19V.

5. Soft-Start: The power switch has an internal soft-start circuit that slowly increases the feedback voltage, together with the SenseFET current, after it starts. The typical soft-start time is 15ms, as shown in Figure 19, where progressive increments of the SenseFET current are allowed during the startup phase. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps prevent transformer saturation and reduce the stress on the secondary diode.

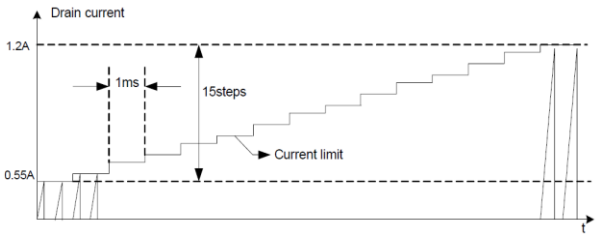


Figure 19. Soft-Start Function

6. Burst Mode Operation: To minimize power dissipation in Standby Mode, the power switch enters Burst Mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 20, the device automatically enters Burst Mode when the feedback voltage drops below V_{BURH} (600mV). Switching continues, but the current limit is set to a fixed limit internally to minimize flux density in the transformer. The fixed current limit is larger than that defined by $V_{FB} = V_{BURH}$ and, therefore, V_{FB} is driven down further. Switching continues until the feedback voltage drops below V_{BURL} (350mV). At this point, switching stops and the output voltages start to drop at a rate dependent on the standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (600mV), switching resumes. The feedback voltage then falls and the process repeats. Burst Mode alternately enables and disables switching of the power SenseFET, reducing switching loss in Standby Mode.

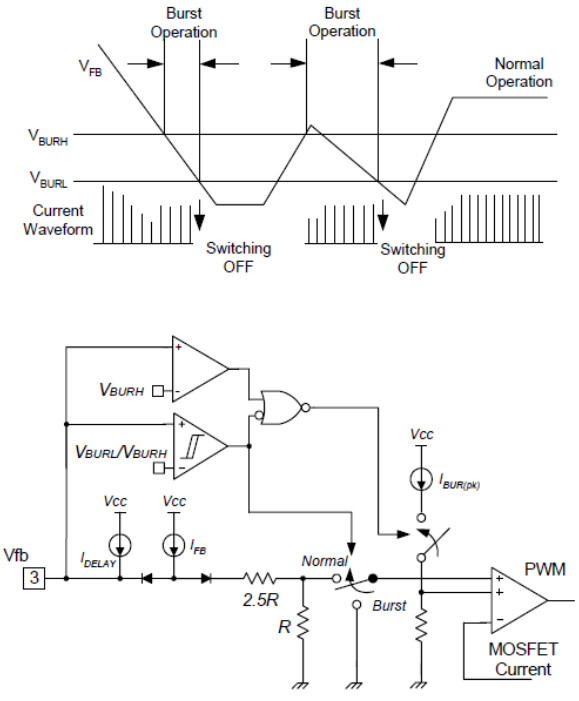


Figure 20. Burst Mode Operation

7. Frequency Modulation: Modulating the switching frequency of a SMPS can reduce EMI by spreading the energy over a wider frequency range than the bandwidth measured by EMI test equipment. The amount of EMI reduction is directly related to the depth of the reference frequency. As can be seen in Figure 21, the frequency changes from 48.5KHz to 51.5KHz in 4ms for the FSDL0165RN. Frequency modulation allows the use of a cost effective inductor instead of an AC input mode choke to satisfy the requirements of worldwide EMI limits.

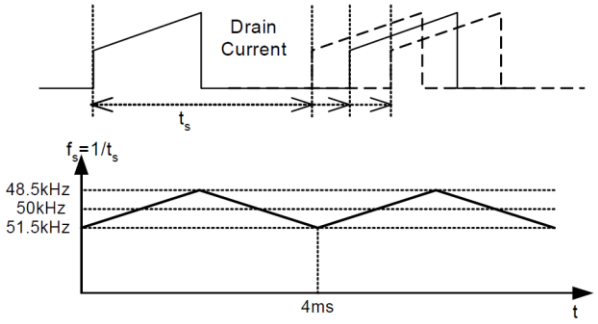


Figure 21. Frequency Modulation Waveform

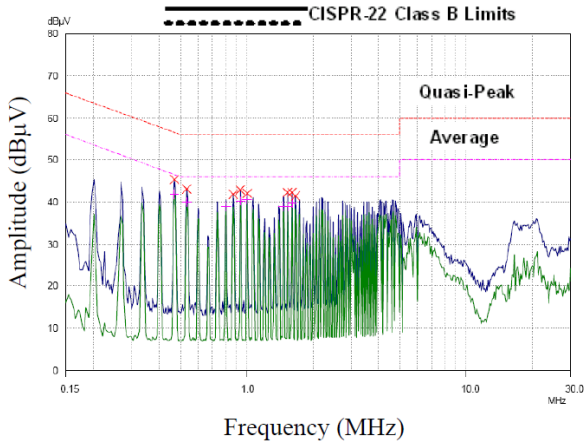


Figure 22. KA5-Series Power Switch Full-Range EMI Scan (67KHz, No Frequency Modulation) with DVD Player SET

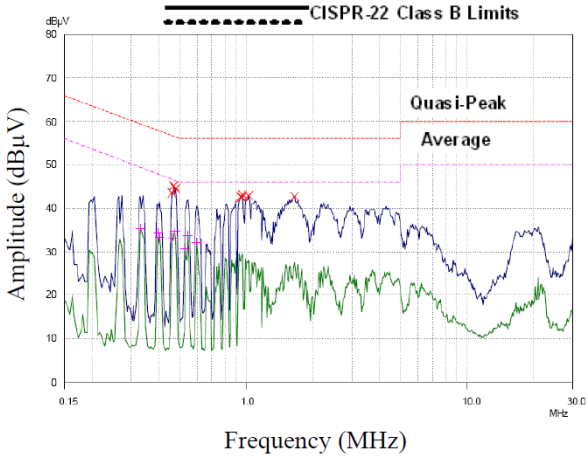


Figure 23. FSDX-Series Power Switch Full-Range EMI Scan (67KHz, with Frequency Modulation) with DVD Player SET

8. Adjusting Peak Current Limit: As shown in Figure 24, a combined 2.8kΩ internal resistance is connected to the non-inverting lead on the PWM comparator. A external resistance of R_X on the current limit pin forms a parallel resistance with the 2.8kΩ when the internal diodes are biased by the main current source of 900µA.

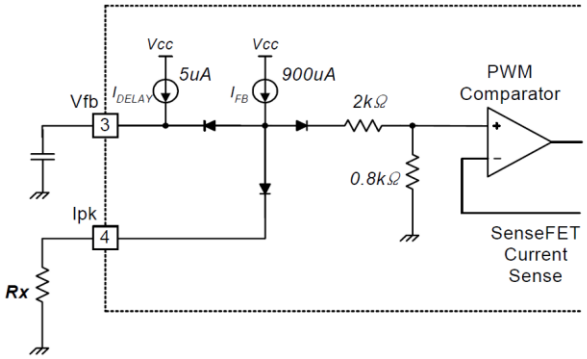


Figure 24. Peak Current Limit Adjustment

For example, FSDL0165RN has a typical SenseFET peak current limit (I_{LIM}) of 1.2A. I_{LIM} can be adjusted to 1A by inserting R_X between the Ipk pin and the ground. The value of the R_X can be estimated by:

$$1.2A : 1A = 2.8k\Omega : Xk\Omega \quad (1)$$

$$X = R_X \parallel 2.8k\Omega \quad (2)$$

where X represents the resistance of the parallel network.

Application Information

Methods of Reducing Audible Noise

Switching mode power converters have electronic and magnetic components that generate audible noises when the operating frequency is in the range of 20~20,000Hz. Even though they operate above 20kHz, they can make noise, depending on the load condition. Designers can employ several methods to reduce noise. Below are three methods.

Glue or Varnish

The most common method involves using glue or varnish to tighten magnetic components. The motion of core, bobbin, and coil and the chattering or magnetostriction of core can cause the transformer to produce audible noise. Rigid glue and varnish help reduce the transformer noise, but can also crack the core. This is because sudden changes in the ambient temperature cause the core and the glue to expand or shrink in a different ratio according to the temperature.

Ceramic Capacitor

Using a film capacitor instead of a ceramic capacitor as a snubber capacitor is another noise-reduction solution. Some dielectric materials show a piezoelectric effect, depending on the electric field intensity. Hence, a snubber capacitor becomes one of the most significant sources of audible noise. It is possible to use a Zener clamp circuit instead of an RCD snubber for higher efficiency and lower audible noise.

Adjusting Sound Frequency

Moving the fundamental frequency of noise out of 2~4kHz range is the third method. Generally, humans are more sensitive to noise in the range of 2~4kHz. When the fundamental frequency of noise is located in this range, the noise is perceived as louder although the noise intensity level is identical (*refer to Figure 16)*.

When the power switch is in Burst Mode and the burst operation is suspected to be a source of noise, this method may be helpful. If the frequency of Burst Mode lies in the range of 2~4kHz, adjusting the feedback loop can shift the burst operation frequency. To reduce the burst operation frequency, increase a feedback gain capacitor (C_F), opto-coupler supply resistor (R_D), and feedback capacitor (C_B) and decrease feedback gain resistor (R_F), as shown in Figure 26.

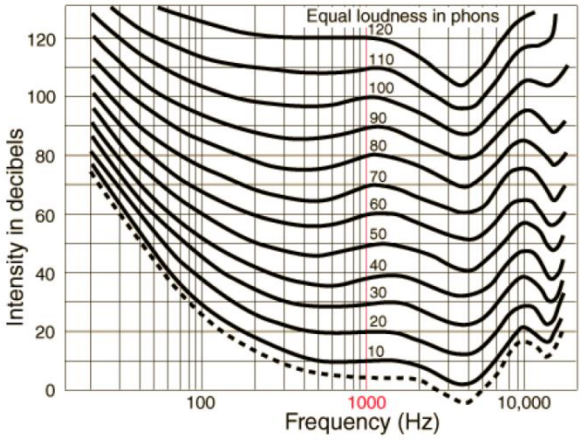


Figure 25. Equal Loudness Curves

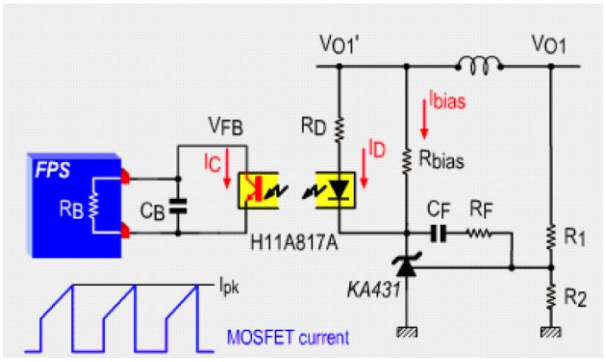


Figure 26. Typical Feedback Network of Power Switch

Reference Materials

- https://www.onsemi.com/pub/Collateral/AN-4134.PDF
- http://www.onsemi.com/pub/Collateral/AN-4137.pdf.pdf
- http://www.onsemi.com/pub/Collateral/AN-4140.pdf.pdf
- http://www.onsemi.com/pub/Collateral/AN-4141.pdf.pdf
- http://www.onsemi.com/pub/Collateral/AN-4148.pdf.pdf

Typical Application Circuit

Application	Output Power	Input Voltage	Output Voltage (Maximum Current)
DVD Player	9.3W	Universal Input (85-256V_{AC})	3.3V (0.5A) 5.1V (0.4A) 12V (0.2A) 16V (0.2A)

Features

- High Efficiency (>76% at Universal Input)
- Low Standby Mode Power Consumption (<1W at 230V_{AC} input and 0.6W Load)
- Low Component Count
- Enhanced System Reliability through Various Protection Functions
- Low EMI through Frequency Modulation
- Internal Soft-Start: 15ms

Key Design Notes

- The delay for overload protection is designed to be about 30ms with C106 (47nF). If faster/slower triggering of OLP is required, C106 can be changed to a smaller/larger value (eg. 100nF for about 60ms).
- Using a resistor R104 (15KΩ) on the Ipk pin (#4), the pulse-by-pulse peak current limit level (I_{LIM}) is adjusted to about 1A.
- The branch formed by D103, C108, and R106 provides another I_{LIM} adjustment; having a negative slope to the input. The I_{LIM} value decreases as the input voltage level increases.

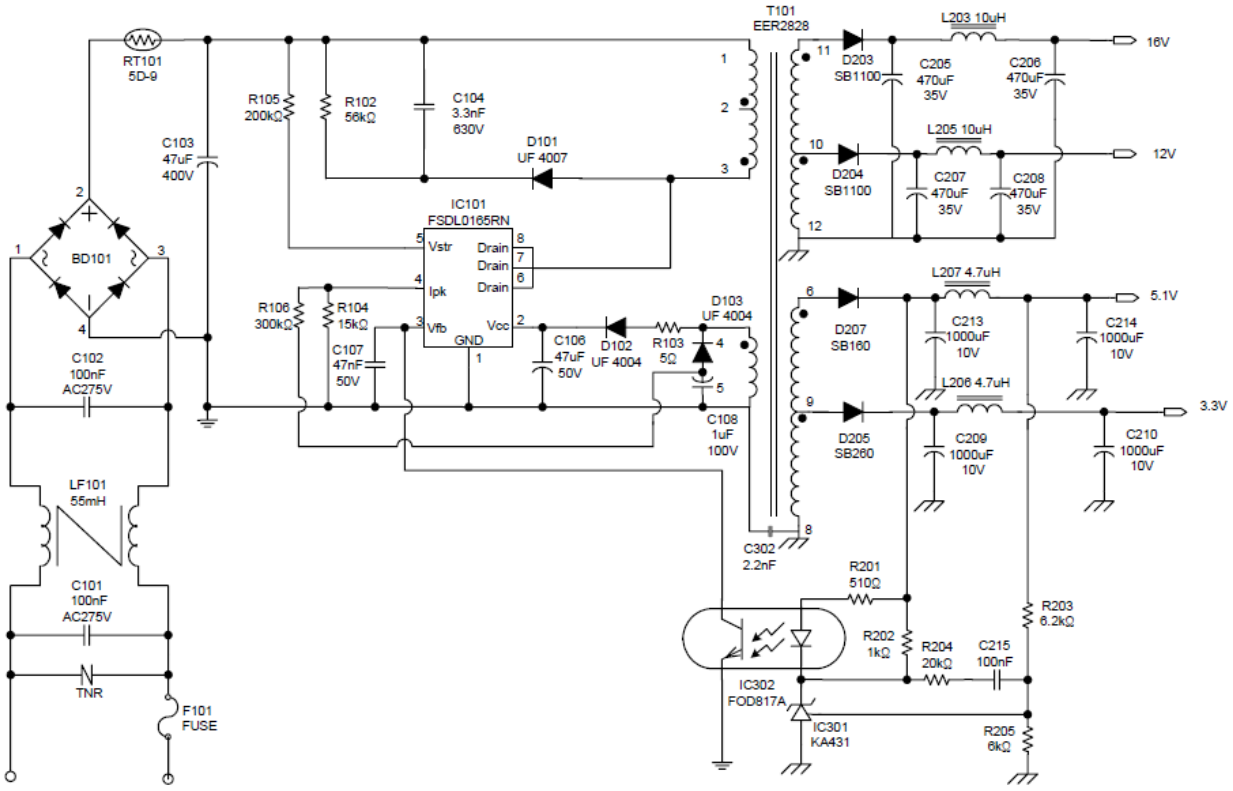


Figure 27. Schematic

Transformer

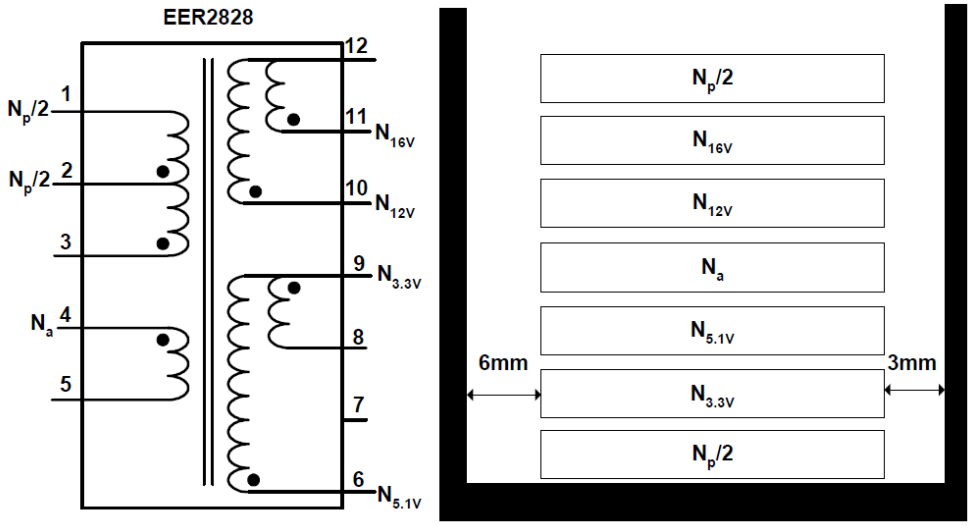


Figure 28. Schematic of Transformer

Winding Specification

	Pin(S → F)	Wire	Turns	Winding Method
N_p /2	3 → 2	0.25φ×1	50	Center Solenoid Winding
Insulation: Polyester Tape t=0.050mm, 2 Layers				
$N_{3.3V}$	9 → 8	0.33φ×2	4	Center Solenoid Winding
Insulation: Polyester Tape t=0.050mm, 2 Layers				
$N_{5.1V}$	6 → 9	0.33φ×1	2	Center Solenoid Winding
Insulation: Polyester Tape t=0.050mm, 2 Layers				
N_a	4 → 5	0.25φ×1	16	Center Solenoid Winding
Insulation: Polyester Tape t=0.050mm, 2 Layers				
N_{12V}	10 → 12	0.33φ×1	14	Center Solenoid Winding
Insulation: Polyester Tape t=0.050mm, 3 Layers				
N_{16V}	11 → 12	0.33φ×1	18	Center Solenoid Winding
Insulation: Polyester Tape t=0.050mm, 2 Layers				
$N_p/2$	2 → 1	0.25φ×1	50	Center Solenoid Winding
Insulation: Polyester Tape t=0.050mm, 2 Layers				

Electrical Characteristics

	Pin	Specification	Remark
Inductance	1−3	1.4mH ±10%	100kHz, 1V
Leakage	1−3	25μH Maximum	Short all other pins

Core & Bobbin

- Core: EER2828 (Ae=86.66mm^2)
- Bobbin: EER2828

Bill of Materials

Part #	Value	Note	Part #	Value	Note
Resistor			**Inductor**		
R102	56kΩ	1W	L203	10μH	
R103	5Ω	1/4W	L205	10μH	
R104	15KΩ	1/4W	L206	4.7μH	
R105	200KΩ	1/4W	L207	4.7μH	
R106	300KΩ	1/4W	**Diode**		
R201	510Ω	1/4W	D101	UF4007	PN Ultra Fast
R202	1KΩ	1/4W	D102	UF4004	PN Ultra Fast
R203	6.2KΩ	1/4W	D103	UF4004	PN Ultra Fast
R204	20KΩ	1/4W	D203	SB1100	Schottky
R205	6KΩ	1/4W	D204	SB1100	Schottky
Capacitor			D205	SB260	Schottky
C101	100nF/275AC	Box	D207	SB160	Schottky
C102	100nF/275AC	Box	**IC**		
C103	47μF/400V	Electrolytic	IC101	FSDL0165RN	Power Switch
C104	3.3nF/630V	Film	IC301	KA431(TL431)	Voltage Reference
C106	47μF/50V	Electrolytic	IC302	FOD817A	Opto-Coupler
C107	47nF/50V	Ceramic			
C108	1μF/100V	Electrolytic	**Fuse**		
C205	470μF/35V	Electrolytic	FUSE	2A/250V	
C206	470μF/35V	Electrolytic	**NTC**		
C207	470μF/35V	Electrolytic			
C208	470μF/35V	Electrolytic	RT101	5D-9	
C209	1000μF/10V	Electrolytic			
C210	1000μF/10V	Electrolytic	**Bridge Diode**		
C213	1000μF/10V	Electrolytic	BD101	2KBP06M 2N257	Bridge Diode
C214	1000μF/10V	Electrolytic			
C215	100nF/50V	Ceramic	**Line Filter**		
C302	2.2nF	AC Ceramic	LF101	55mH	

Layout

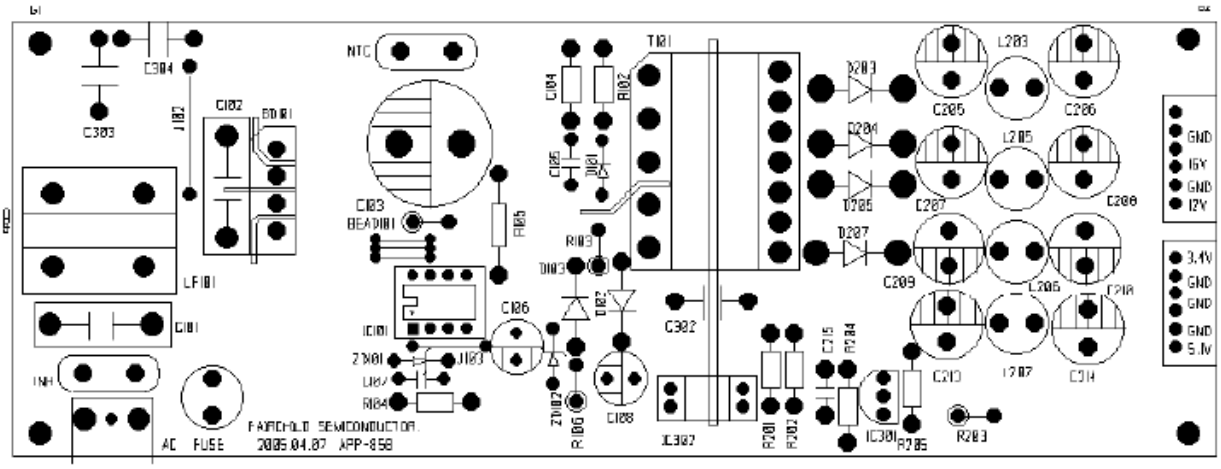


Figure 29. PCB Image (Top)

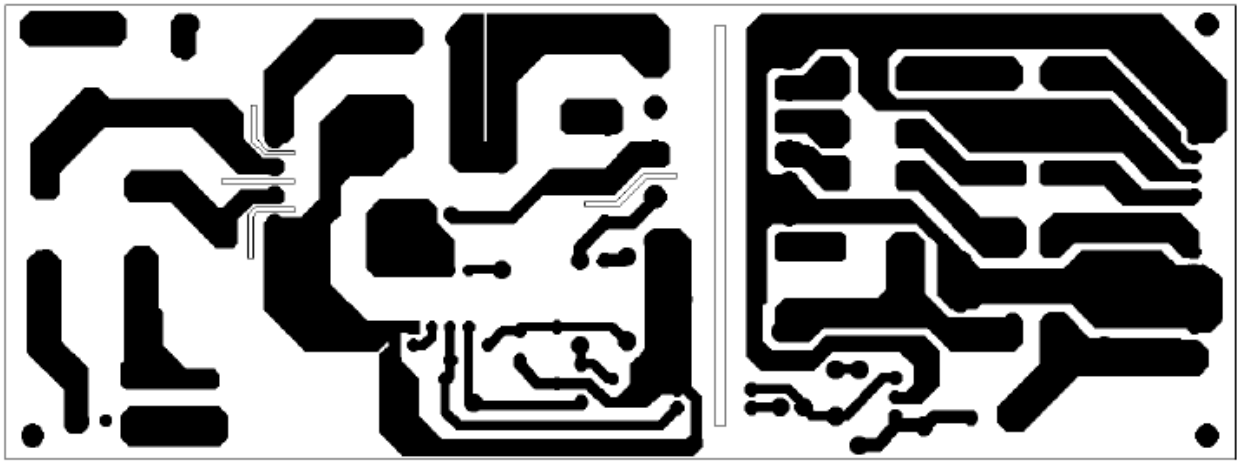
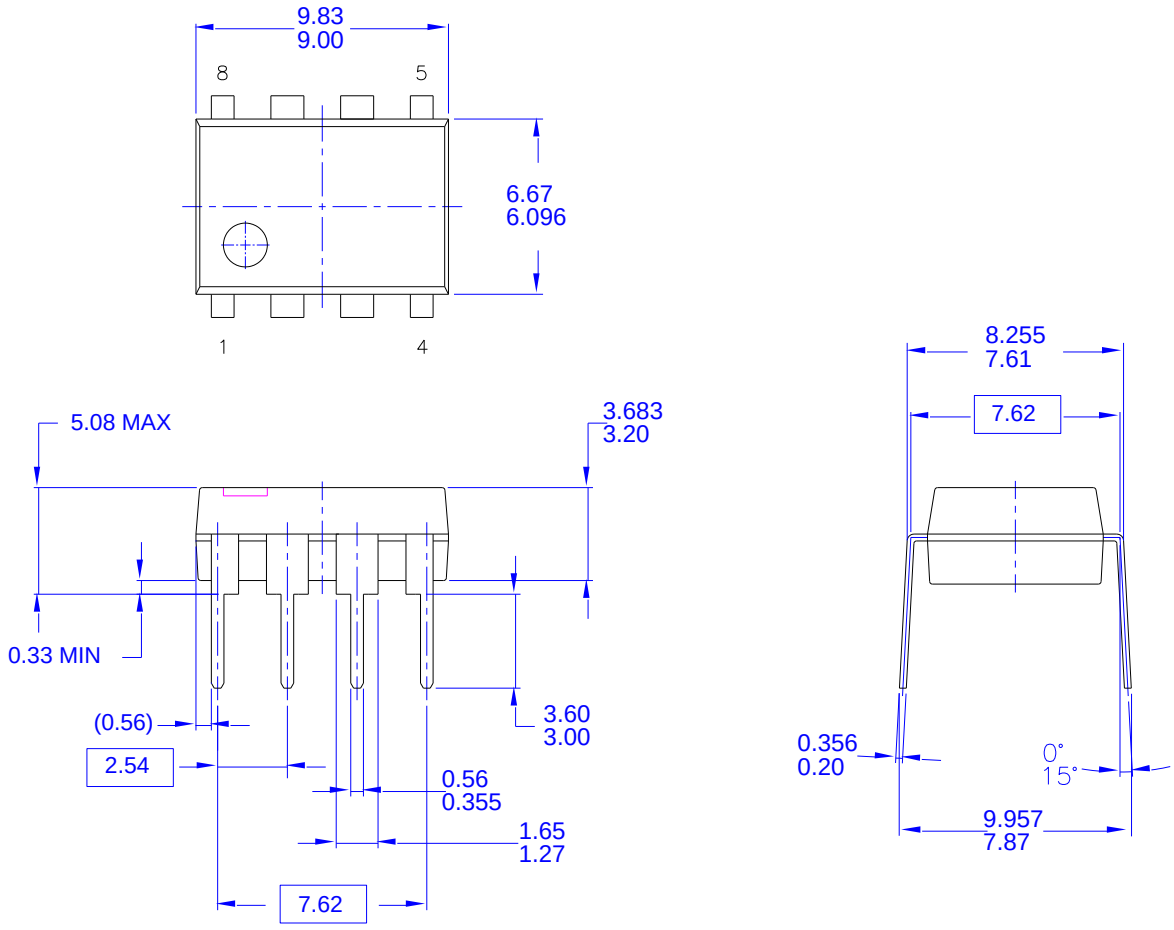


Figure 30. PCB Image (Bottom)

Package Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

E) DRAWING FILENAME AND REVSION: MKT-N08FREV2.

Figure 31. 8-Lead, MDIP, JEDEC MS-001, .300" Wide

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