FSDM0265RNB

Green Mode Power Switch

Description

The FSDM0265RNB of integrated Pulse Width Modulator (PWM) and Sense FET are specifically designed for high performance offline Switch Mode Power Supplies (SMPS) with minimal external components. This devices is an integrated high voltage power switching regulator which combines an avalanche rugged Sense FET with a current mode PWM control block. The integrated PWM controller features include: a fixed oscillator with frequency modulation for reduced EMI, Under Voltage Lock Out (UVLO) protection, Leading Edge Blanking (LEB), an optimized gate turn−on/turn−off driver, Thermal Shut Down (TSD) protection and temperature compensated precision current sources for loop compensation and fault protection circuitry. The FSDM0265RNB offers better performance in Soft Start than FSDM0265RN. When compared to a discrete MOSFET and controller or RCC switching converter solution, the FSDM0265RNB reduces total component count, design size, weight while increasing efficiency, productivity and system reliability. This device provides a basic platform that is well suited for the design of cost−effective flyback converters.

Features

- Internal Avalanche Rugged Sense FET
- Consumes only 0.65 W at 240 VAC & 0.3 W load with Advanced Burst−Mode Operation
- Frequency Modulation for EMI Reduction
- Precision Fixed Operating Frequency
- Internal Start−up Circuit
- Pulse−by−Pulse Current Limiting
- Over Voltage Protection (OVP)
- Over Load Protection (OLP)
- Internal Thermal Shutdown Function (TSD)
- Auto−Restart Mode
- Under Voltage Lockout (UVLO)
- Low Operating Current (3 mA)
- Adjustable Peak Current Limit
- Built−in Soft Start

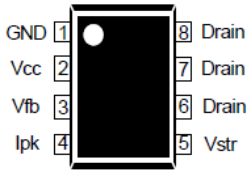
Applications

- SMPS for VCR, SVR, STB, DVD & DVCD
- SMPS for Printer, Facsimile & Scanner
- Adapter for Camcorder

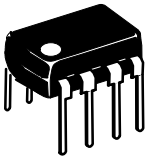
ON Semiconductor®

www.onsemi.com

8DIP

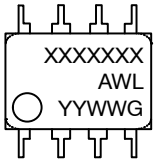


PIN CONFIGURATION



PDIP8
(9.42x6.38, 2.54P)
CASE 646CM

MARKING DIAGRAM



DM0265R	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

ORDERING INFORMATION

Product Number	Package	Marking Code	BV_{DSS}	f_{OSC}	$R_{DS(ON)}$
FSDM0265RNB	8DIP	DM0265R	650 V	67 KHz	5.0 Ω

Table 1. OUTPUT POWER TABLE

Product	230VAC±15% (Note 3)		85−265VAC	
	Adapter (Note 1)	Open Frame (Note 2)	Adapter (Note 1)	Open Frame (Note 2)
FSDM0265RNB	16 W	27 W	13 W	20 W
FSDL0365RNB	19 W	30 W	16 W	24 W
FSDM0365RNB	19 W	30 W	16 W	24 W

1. Typical continuous power in a non−ventilated enclosed adapter with sufficient drain pattern as a heat sinker, at 50_C ambient.
2. Maximum practical continuous power in an open frame design with sufficient drain pattern as a heat sinker, at 50_C ambient.
3. 230 VAC or 100/115 VAC with doubler.

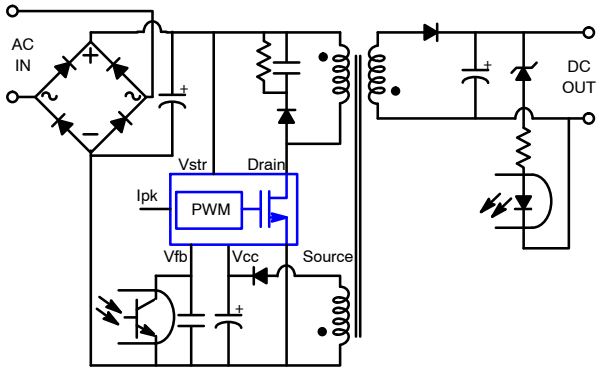


Figure 1. Typical Flyback Application

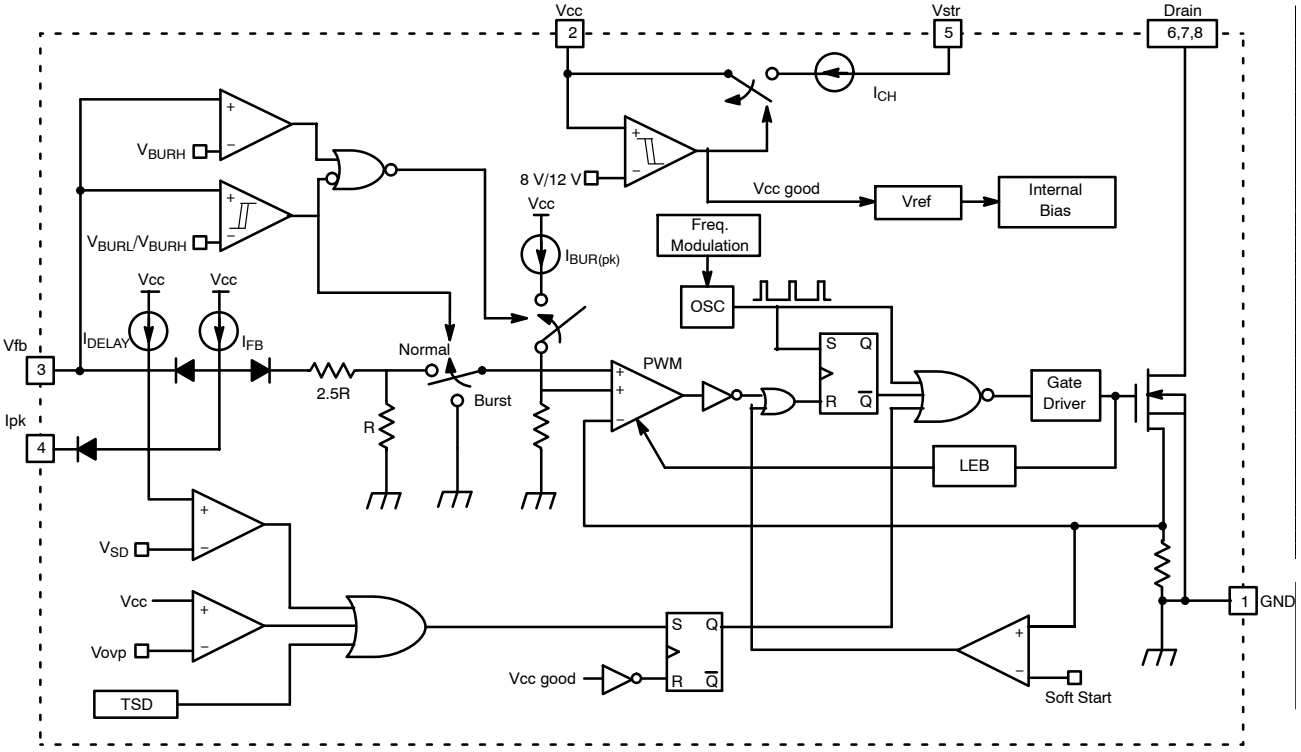


Figure 2. Functional Block Diagram of FSDM0265RNB

Table 2. PIN DEFINITIONS

Pin Number	Pin Name	Pin Function Description
1	GND	Sense FET source terminal on primary side and internal control ground.
2	Vcc	Positive supply voltage input. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (Vstr) via an internal switch during startup (see Internal Block Diagram section). It is not until Vcc reaches the UVLO upper threshold (12 V) that the internal start−up switch opens and devicepower is supplied via the auxiliary transformer winding.
3	Vfb	The feedback voltage pin is the non−inverting input to the PWM comparator. It has a 0.9mA current source connected internally while a capacitor and optocoupler are typically connected externally. A feedback voltage of 6V triggers over load protection (OLP). There is a time delay while charging external capacitor Cfb from 3 V to 6 V using an internal 5uA current source. This time delay prevents false triggering under transient conditions, but still allows the protection mechanism to operate under true overload conditions.
4	Ipk	This pin adjusts the peak current limit of the Sense FET. The feedback 0.9 mA current source is diverted to the parallel combination of an internal 2.8kW resistor and any external resistor to GND on this pin to determine the peak current limit. If this pin is tied to Vcc or left floating, the typical peak current limit will be 1.5 A.
5	Vstr	This pin connects directly to the rectified AC line voltage source. At start up the internal switch supplies internal bias and charges an external storage capacitor placed between the Vcc pin and ground. Once the Vcc reaches 12 V, the internal switch is opened.
6	Drain	The drain pins are designed to connect directly to the primary lead of the transformer and are capable of switching a maximum of 650V. Minimizing the length of the trace connecting these pins to the transformer will decrease leakage inductance.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C, unless otherwise specified)

Symbol	Parameter	Ratings	Unit
V_{DRAIN}	Drain Pin Voltage	650	V
V_{STR}	Vstr Pin Voltage	650	V
I_{DM}	Drain Current Pulsed (Note 4)	8.0	A
E_{AS}	Single Pulse Avalanche Energy (Note 5)	68	mJ
V_{CC}	Supply Voltage	20	V
V_{FB}	Feedback Voltage Range	−0.3 to V_{CC}	V
P_D	Total Power Dissipation	1.56	W
T_J	Operating Junction Temperature	Internally limited	°C
T_A	Operating Ambient Temperature	−25 to +85	°C
T_{STG}	Storage Temperature	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. Repetitive rating: Pulse width is limited by maximum junction temperature
5. L = 51 mH, T_J = 25°C.

THERMAL CHARACTERISTICS (Ta = 25°C, unless otherwise specified)

Symbol	Parameter	Ratings	Unit
8DIP			
θ_{JA}	Junction−to−Ambient Thermal (Note 6)	79.64	°C/W
θ_{JC}	Junction−to−Case Thermal (Note 7)	18.20	°C/W
ψ_{JT}	Junction−to−Top Thermal (Note 8)	34.30	°C/W

6. Free standing with no heatsink; without copper clad
7. Measured on the DRAIN pin close to plastic interface
8. Measured on the PKG top surface

NOTE: All items are tested with the standards JESD 51−2 and 51−10 (DIP).

ELECTRICAL CHARACTERISTICS (Ta = 25°C unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
SENSE FET SECTION						
I_{DSS}	Zero−Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	–	–	50	μA
		V_{DS} = 520 V, V_{GS} = 0 V, T_C = 125°C	–	–	200	μA
$R_{DS(ON)}$	Drain−Source On−State Resistance (Note 9)	V_{GS} = 10 V, I_D = 0.5 A	–	5.0	6.0	Ω
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	–	550	–	pF
C_{OSS}	Output Capacitance		–	38	–	pF
C_{RSS}	Reverse Transfer Capacitance		–	17	–	pF
$t_{d(on)}$	Turn−On Delay Time	V_{DS} = 325 V, I_D = 1.0 A	–	20	–	ns
t_r	Rise Time		–	15	–	ns
$t_{d(off)}$	Turn−Off Delay Time		–	55	–	ns
t_f	Fall Time		–	25	–	ns
CONTROL SECTION						
f_{OSC}	Switching Frequency		61	67	73	KHz
Δf_{MOD}	Switching Frequency Modulation		±1.5	±2.0	±2.5	KHz
Δf_{OSC}	Switching Frequency Variation (Note 10)	−25°C ≤ Ta ≤ 85°C	–	±5	±10	%
D_{MAX}	Maximum Duty Cycle		62	67	72	%
D_{MIN}	Minimum Duty Cycle		0	0	0	%
V_{START}	UVLO Threshold Voltage	V_{FB} = GND	11	12	13	V
V_{STOP}		V_{FB} = GND	7	8	9	V
I_{FB}	Feedback Source Current	V_{FB} = GND	0.7	0.9	1.1	mA
$t_{S/S}$	Internal Soft Start Time	V_{FB} = 4 V	10	15	20	ms
BURST MODE SECTION						
V_{BURH}	Burst Mode Voltage	–	0.4	0.5	0.6	V
V_{BURL}		–	0.25	0.35	0.45	V
PROTECTION SECTION						
I_{LIM}	Peak Current Limit	Max. inductor current	1.3	1.5	1.7	A
t_{CLD}	Current Limit Delay Time (Note 11)		–	500	–	ns
T_{SD}	Thermal Shutdown Temperature	–	125	140	–	°C
V_{SD}	Shutdown Feedback Voltage		5.5	6.0	6.5	V
V_{OVP}	Over Voltage Protection	V_{FB} = 4 V	18	19	–	V
I_{DELAY}	Shutdown Delay Current		3.5	5.0	6.5	μA
t_{LEB}	Leading Edge Blanking Time		200	–	–	ns
TOTAL DEVICE SECTION						
I_{OP}	Operating Supply Current (control part only)	V_{CC} = 14 V	1	3	5	mA
I_{CH}	Start−Up Charging Current	V_{CC} = 0 V	0.7	0.85	1.0	mA
V_{STR}	Vstr Supply Voltage	V_{CC} = 0 V	35	–	–	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9. Pulse test: Pulse width ≤ 300us, duty ≤ 2%
10. These parameters, although guaranteed, are tested in EDS (wafer test) process
11. These parameters, although guaranteed, are not 100% tested in production

Table 3. COMPARISON BETWEEN KA5x0265RN AND FSDM0265RNB

Function	KA5x0265RN	FSDM0265RNB	FSDM0265RNB Advantage
Soft−Start	not applicable	15 ms	• Gradually increasing current limit during soft−start further reduces peak current and voltage stresses • Eliminates external components used for soft−start in most applications • Reduces or eliminates output overshoot
External Current Limit	not applicable	Programmable of default current limit	• Smaller transformer • Allows power limiting (constant over− load power) • Allows use of larger device for lower losses an higher efficiency
Frequency Modulation	not applicable	±2.0 KHz @67 KHz	• Reduces conducted EMI
Burst Mode Operation	not applicable	Built into controller	• Improves light load efficiency • Reduces power consumption at no−load • Transformer audible noise reduction
Drain Creepage at Package	1.02 mm	7.62 mm	• Greater immunity to arcing provoked by dust, debris and other contaminants

Typical Performance Characteristics (Control Part)

(These characteristic graphs are normalized at Ta = 25°C)

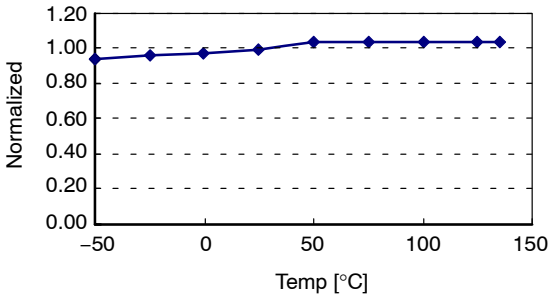


Figure 3. Operating Frequency (Fosc) vs. Ta

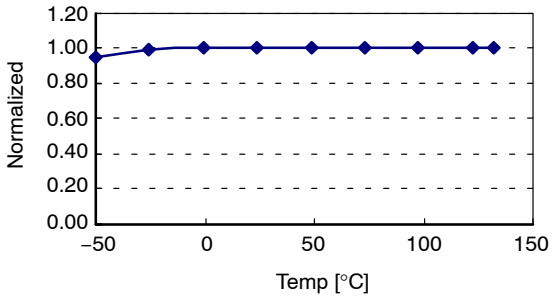


Figure 4. Frequency Modulation (ΔF_{MOD}) vs. Ta

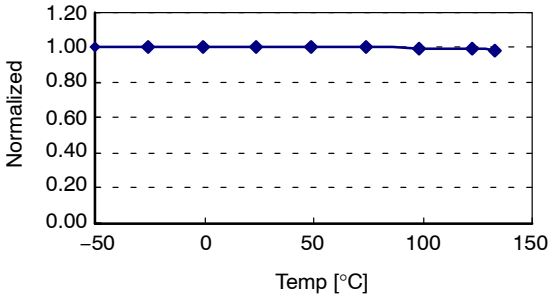


Figure 5. Maximum Duty Cycle (D_{MAX}) vs. Ta

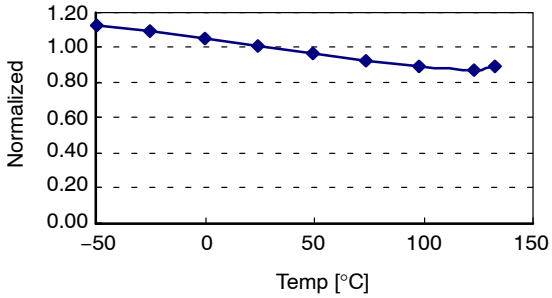


Figure 6. Operating Supply Current (I_{OP}) vs. Ta

Typical Performance Characteristics (Control Part) (continued)

(These characteristic graphs are normalized at Ta = 25°C)

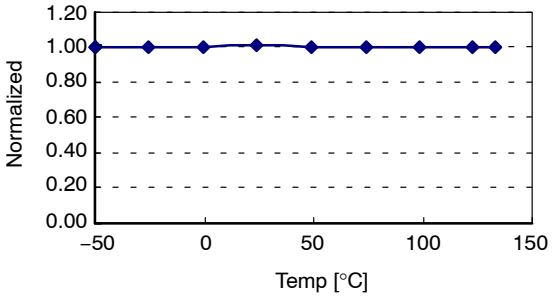


Figure 7. Start Threshold Voltage (V_{START}) vs. Ta

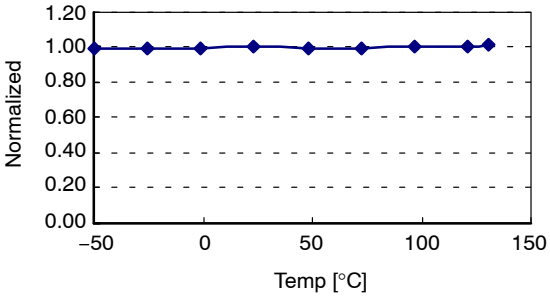


Figure 8. Stop Threshold Voltage (V_{STOP}) vs. Ta

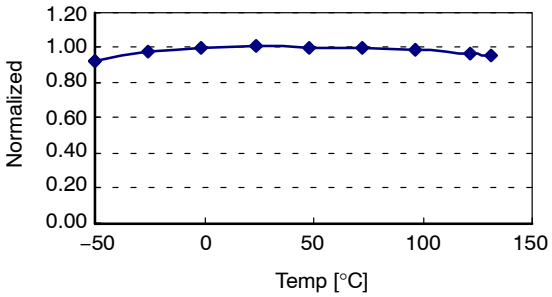


Figure 9. Feedback Source Current (I_{FB}) vs. Ta

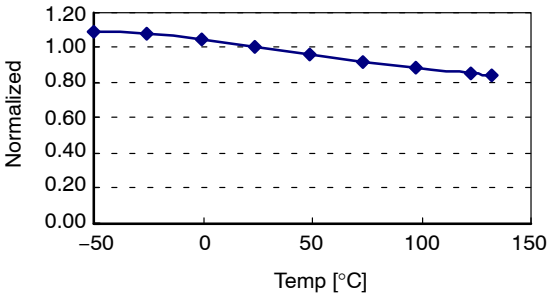


Figure 10. Start Up Charging Current (I_{CH}) vs. Ta

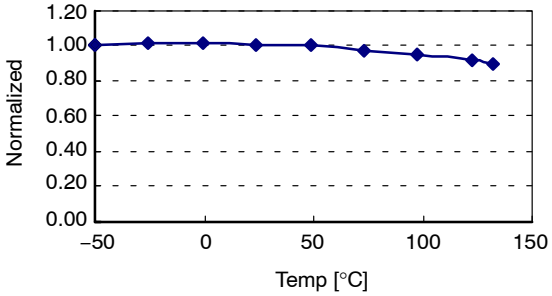


Figure 11. Peak Current Limit (I_{LIM}) vs. Ta

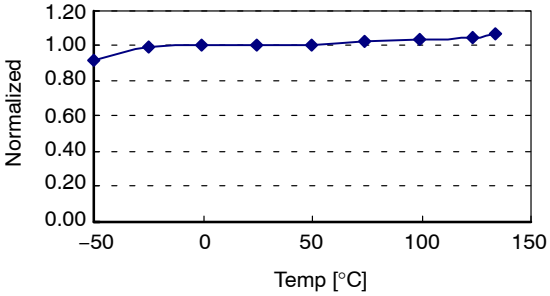


Figure 12. Burst Peak Current ($I_{BUR(pk)}$) vs. Ta

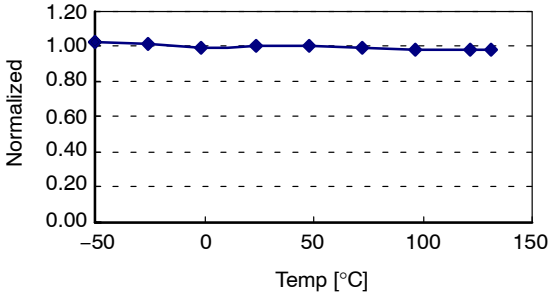


Figure 13. Over Voltage Protection (V_{OVP}) vs. Ta

FUNCTIONAL DESCRIPTION

Startup

In previous generations of Power Switches the Vstr pin had an external resistor to the DC input voltage line. In this generation the startup resistor is replaced by an internal high voltage current source and a switch that shuts off when 15 ms goes by after the supply voltage, Vcc, gets above 12 V. The source turns back on if Vcc drops below 8 V.

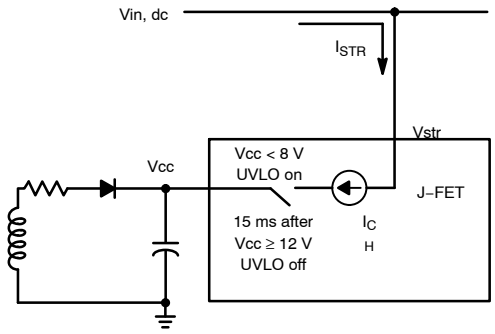


Figure 14. High Voltage Current Source

Feedback Control

The FSDM0265RNB employs current mode control, as shown in Figure 15. An opto−coupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the Rsense resistor plus an offset voltage makes it possible to control the switching duty cycle. When the KA431 reference pin voltage exceeds the internal reference voltage of 2.5 V, the optocoupler LED current increases, the feedback voltage Vfb is pulled down and it reduces the duty cycle. This event typically happens when the input voltage is increased or the output load is decreased.

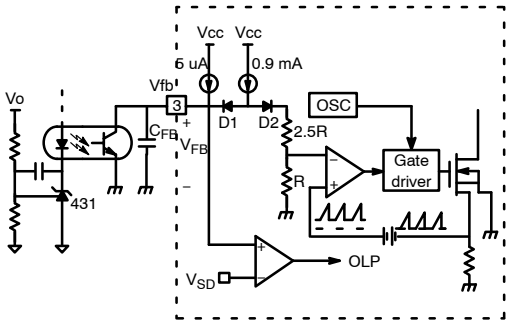


Figure 15. Pulse Width Modulation (PWM) Circuit

Leading Edge Blanking (LEB)

At the instant the internal Sense FET is turned on, the primary side capacitance and secondary side rectifier diode reverse recovery typically cause a high current spike through the Sense FET. Excessive voltage across the Rsense resistor leads to incorrect feedback operation in the current mode PWM control. To counter this effect, the power switch employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (tLEB) after the Sense FET is turned on.

Protection Circuits

The power switch has several protective functions such as over load protection (OLP), over voltage protection (OVP), under voltage lock out (UVLO) and thermal shutdown (TSD). Because these protection circuits are fully integrated inside the IC without external components, the reliability is improved without increasing cost. Once a fault condition occurs, switching is terminated and the Sense FET remains off. This causes Vcc to fall. When Vcc reaches the UVLO stop voltage V_{STOP} (8 V), the protection is reset and the internal high voltage current source charges the Vcc capacitor via the Vstr pin. When Vcc reaches the UVLO start voltage V_{START} (12 V), the power switch resumes its normal operation. In this manner, the auto−restart can alternately enable and disable the switching of the power Sense FET until the fault condition is eliminated.

Over Load Protection (OLP)

Overload is defined as the load current exceeding a pre−set level due to an unexpected event. In this situation, the protection circuit should be activated in order to protect the SMPS. However, even when the SMPS is operating normally, the over load protection (OLP) circuit can be activated during the load transition. In order to avoid this undesired operation, the OLP circuit is designed to be activated after a specified time to determine whether it is a transient situation or an overload situation. In conjunction with the Ipk current limit pin (if used) the current mode feedback path would limit the current in the Sense FET when the maximum PWM duty cycle is attained. If the output consumes more than this maximum power, the output voltage (Vo) decreases below its rating voltage. This reduces the current through the opto−coupler LED, which also reduces the opto−coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 3 V, the feedback input diode is blocked and the 5 uA current source (I_{DELAY}) starts to charge Cfb slowly up to Vcc. In this condition, V_{FB} increases until it reaches 6 V, when the switching operation is terminated as shown in Figure 16. The shutdown delay time is the time required to charge Cfb from 3 V to 6 V with 5 uA current source.

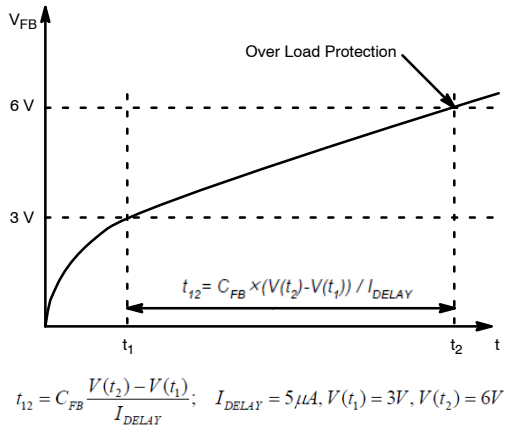


Figure 16. Over Load Protection (OLP)

Thermal Shutdown (TSD)

The Sense FET and the control IC are integrated, making it easier for the control IC to detect the temperature of the Sense FET. When the temperature exceeds approximately 140°C, thermal shutdown is activated.

Over Voltage Protection (OVP)

In the event of a malfunction in the secondary side feedback circuit, or an open feedback loop caused by a soldering defect, the current through the opto−coupler transistor becomes almost zero (refer to Figure 15). Then, VFB climbs up in a similar manner to the over load situation, forcing the preset maximum current to be supplied to the SMPS until the over load protection is activated. Because excess energy is provided to the output, the output voltage may exceed the rated voltage before the over load protection is activated, resulting in the breakdown of the devices in the secondary side. In order to prevent this situation, an over voltage protection (OVP) circuit is employed. In general, Vcc is proportional to the output voltage and the power switch uses Vcc instead of directly monitoring the output voltage. If VCC exceeds 19 V, OVP circuit is activated resulting in termination of the switching operation. In order to avoid undesired activation of OVP during normal operation, Vcc should be properly designed to be below 19 V.

Soft Start

The power switch has an internal soft start circuit that slowly increases the feedback voltage together with the Sense FET current after it starts up. The typical soft start time is 15msec, as shown in Figure 17, where progressive increments of the Sense FET current are allowed during the start−up phase. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps to prevent transformer saturation and reduce the stress on the secondary diode.

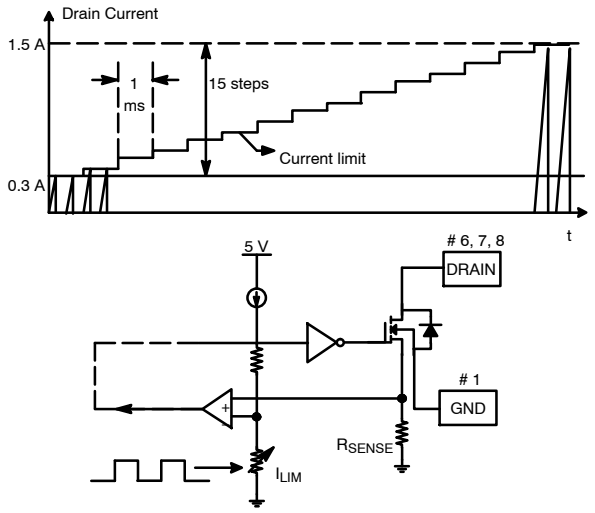


Figure 17. Soft Start Function

Burst Operation

In order to minimize power dissipation in standby mode, the power switch enters burst mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 18, the device automatically enters burst mode when the feedback voltage drops below V_{BURH} (500 mV). Switching still continues but the current limit is set to a fixed limit internally to minimize flux density in the transformer. The fixed current limit is larger than that defined by VFB = VBURH and therefore, V_{FB} is driven down further. Switching continues until the feedback voltage drops below V_{BURL} (350 mV). At this point switching stops and the output voltages start to drop at a rate dependent on the standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH}, switching resumes. The feedback voltage then falls and the process repeats. Burst mode operation alternately enables and disables switching of the Sense FET and reduces switching loss in Standby mode.

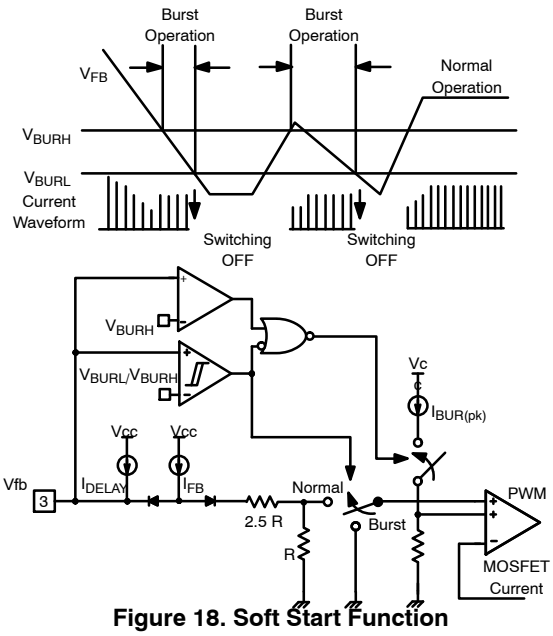


Figure 18. Soft Start Function

Frequency Modulation

Modulating the switching frequency of a switched power supply can reduce EMI. Frequency modulation can reduce EMI by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. The amount of EMI reduction is directly related to the depth of the reference frequency. As can be seen in Figure 19, the frequency changes from 65 KHz to 69 KHz in 4 ms for the FSDM0265RNB. Frequency modulation allows the use of a cost effective inductor instead of an AC input mode choke to satisfy the requirements of world wide EMI limits.

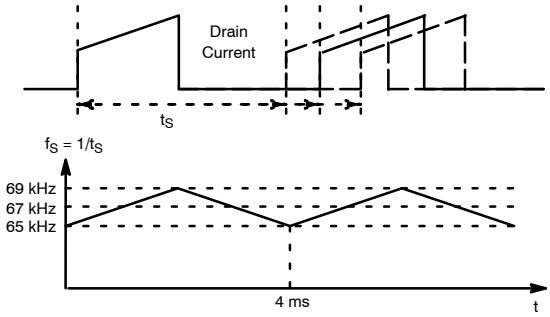


Figure 19. Frequency Modulation Waveform

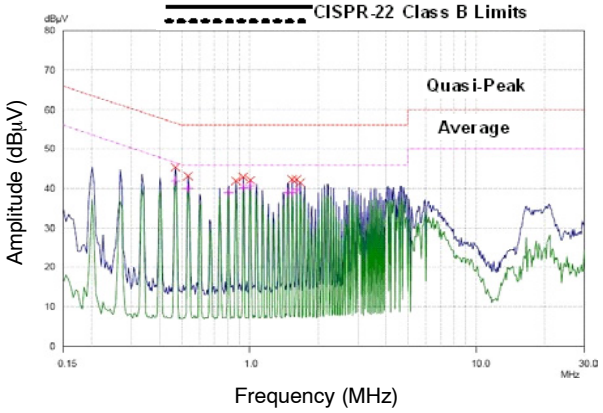


Figure 20. KA5−series Power Switch Full Range EMI scan (67 KHz, no Frequency Modulation) with DVD Player SET

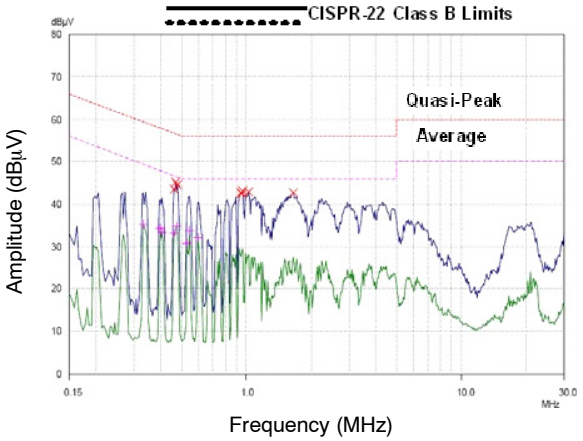


Figure 21. FSDX−series Power Switch Full Range EMI Scan (67 KHz, with Frequency Modulation) with DVD Player SET

Adjusting Peak Current Limit

As shown in Figure 22, a combined 2.8 kΩ internal resistance is connected to the non−inverting lead on the PWM comparator. A external resistance of Rx on the current limit pin forms a parallel resistance with the 2.8 kΩ when the internal diodes are biased by the main current source of 900 uA.

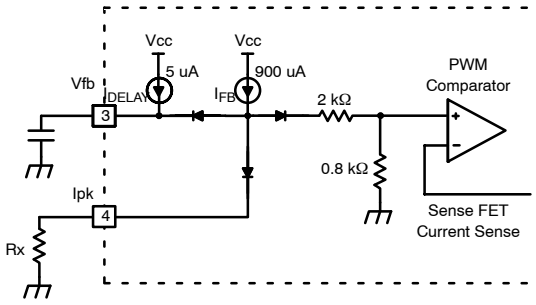


Figure 22. Peak Current Limit Adjustment

For example, FSDM0265RNB has a typical Sense FET peak current limit (I_{LIM}) of 1.5 A. ILIM can be adjusted to 1 A by inserting Rx between the Ipk pin and the ground. The value of the Rx can be estimated by the following equations:

$$1.5\ A : 1\ A = 2.8\ k\Omega : X\ k\Omega \quad \text{(eq. 1)}$$

$$X = Rx \parallel 2.8\ k\Omega \quad \text{(eq. 2)}$$

(X represents the resistance of the parallel network)

Table 4. TYPICAL APPLICATION CIRCUIT

Application	Output Power	Input Voltage	Output Voltage (Max Current)
DVD Player	13 W	Universal Input (85−265 Vac)	3.3 V (0.8 A) 5.1 V (0.4 A) 12 V (0.3 A) 16 V (0.3 A)

Features

- High efficiency (> 76% at universal input)
- Low standby mode power consumption (< 1 W at 230 Vac input and 0.5 W load)
- Low component count
- Enhanced system reliability through various protection functions
- Low EMI through frequency modulation
- Internal soft−start (15 ms)

Key Design Notes

- The delay time for over load protection is designed to be about 30 ms with C106 of 47 nF. If faster/slower triggering of OLP is required, C106 can be changed to a smaller/larger value (eg. 100 nF for about 60 ms).
- Using a resistor R104 (3.3 Ω) on Ipk pin (#4), the pule−by−pulse peak current limit level(I_{LIM}) is adjusted to about 0.8 A.
- The branch formed by D103, C108 and R106 provides another I_{LIM} adjustment having a negative slope to the input voltage. The I_{LIM} value decreases as the input voltage level increases.

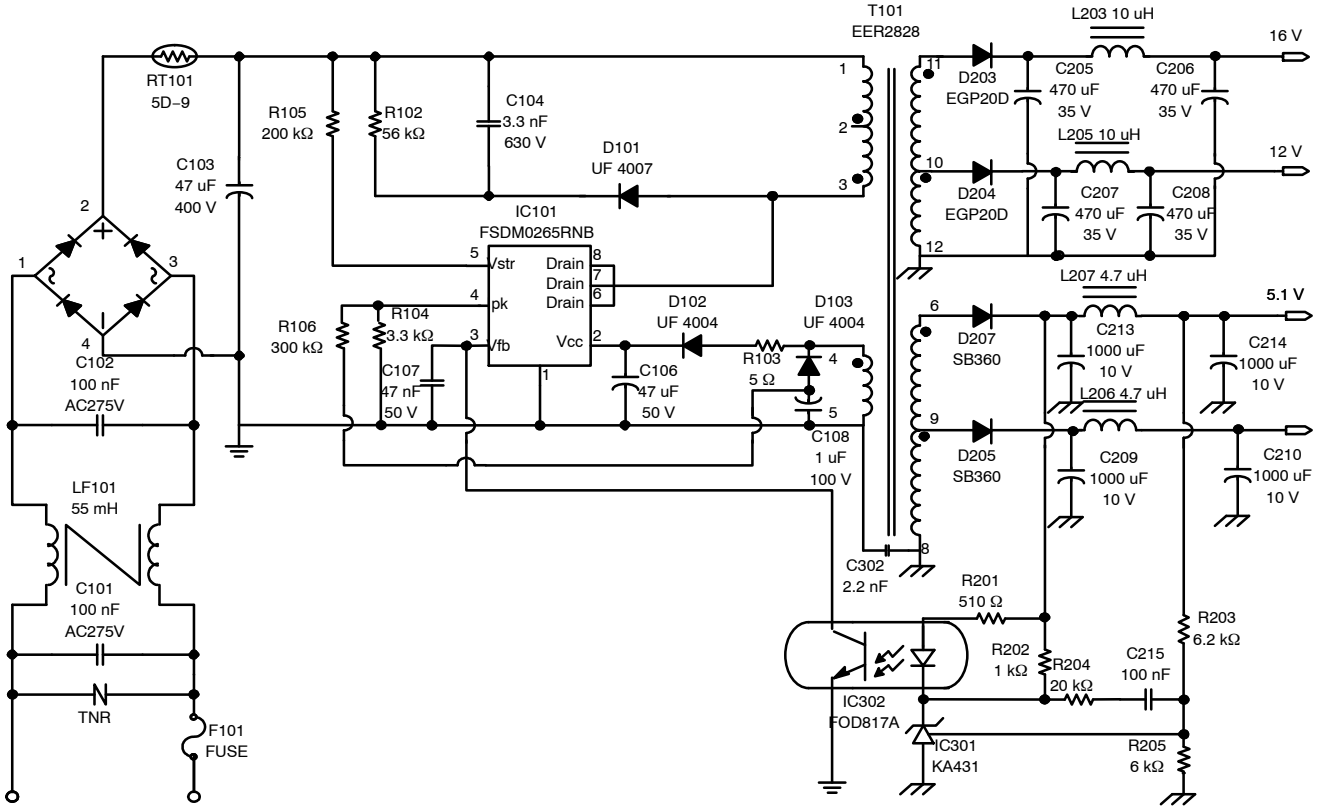


Figure 23. Schematic

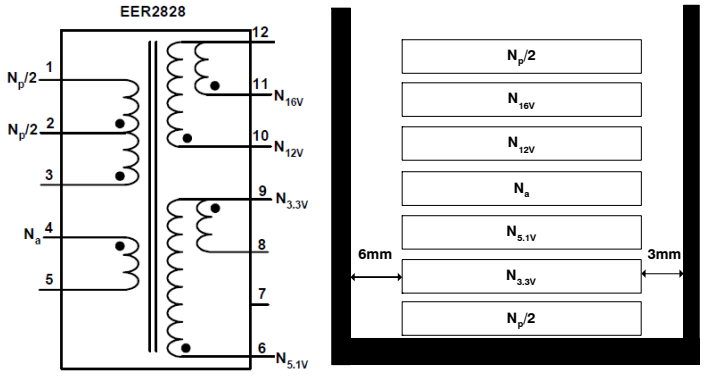


Figure 24. Transformer Schematic Diagram

Table 5. WINDING SPECIFICATION

	Pin (S→F)	Wire	Turns	Winding Method
$N_p/2$	3→2	0.25 φ × 1	50	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050 mm, 2 Layers				
$N_{3.3V}$	9→8	0.33 φ × 2	4	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050 mm, 2 Layers				
$N_{5.1V}$	6→9	0.33 φ × 1	2	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050 mm, 2 Layers				
N_a	4→5	0.25 φ × 1	16	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050 mm, 2 Layers				
N_{12V}	10→12	0.33 φ × 1	14	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050 mm, 3 Layers				
N_{16V}	11→12	0.33 φ × 1	18	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050 mm, 2 Layers				
$N_p/2$	2→1	0.25 φ × 1	50	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050 mm, 2 Layers				

Table 6. ELECTRICAL CHARACTERISTICS

	Pin	Spec.	Remark
Inductance	1–3	1.4 mH ± 10%	100 kHz, 1 V
Leakage	1–3	25 uH Max.	Short all other pins

Core & Bobbin

Core: EER2828 (Ae = 86.66 mm^2)
Bobbin: EER2828

Table 7. DEMO CIRCUIT PART LIST

Part	Value	Note	Part	Value	Note
Resistor			**Inductor**		
R102	56 K	1 W	L203	10 uH	–
R103	5	1/4 W	L205	10 uH	–
R104	3.3 K	1/4 W	L206	4.7 uH	–
R105	200 K	1/4 W	L207	4.7 uH	–
R106	300 K	1/4 W	Diode		
R201	510	1/4 W	D101	UF4007	PN Ultra Fast
R202	1 K	1/4 W	D102	UF4004	PN Ultra Fast
R203	6.2 K	1/4 W	D103	UF4004	PN Ultra Fast
R204	20 K	1/4 W	D203	EGP20D	PN Ultra Fast
R205	6 K	1/4 W	D204	EGP20D	PN Ultra Fast
Capacitor			D205	SB360	Schottky
C101	100 nF/275 AC	Box	D207	SB360	Schottky
C102	100 nF/275 AC	Box	IC		
C103	47 uF/400 V	Electrolytic	IC101	FSDM0265RNB	Power Switch
C104	3.3 nF/630 V	Film	IC301	KA431 (TL431)	Voltage reference
C106	47 uF/50 V	Electrolytic	IC302	FOD817A	Opto−Coupler
C107	47 nF/50 V	Ceramic			
C108	1 uF/100 V	Electrolytic	Fuse		

Table 7. DEMO CIRCUIT PART LIST (continued)

Part	Value	Note	Part	Value	Note
Resistor			**Inductor**		
C205	470 uF/35 V	Electrolytic	FUSE	2 A/250 V	
C206	470 uF/35 V	Electrolytic			
C207	470 uF/35 V	Electrolytic	NTC		
C208	470 uF/35 V	Electrolytic	RT101	5D−9	
C209	1000 uF/10 V	Electrolytic			
C210	1000 uF/10 V	Electrolytic	Bridge Diode		
C213	1000 uF/10 V	Electrolytic	BD101	2KBP06M 2N257	Bridge Diode
C214	1000 uF/10 V	Electrolytic			
C215	100 nF/50 V	Ceramic	Line Filter		
C302	2.2 nF	AC Ceramic	LF101	55 mH	–

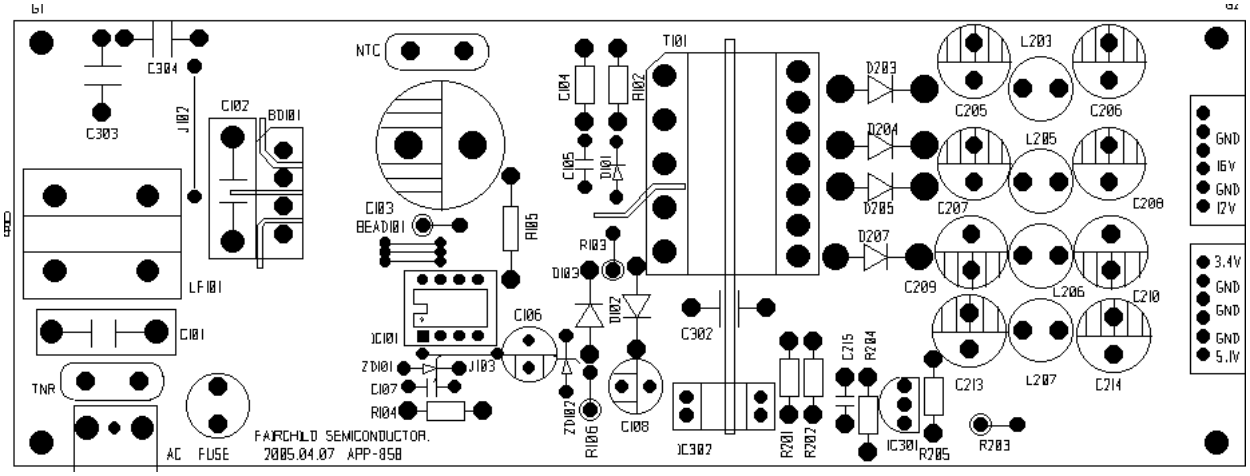


Figure 25. Top Image of PCB

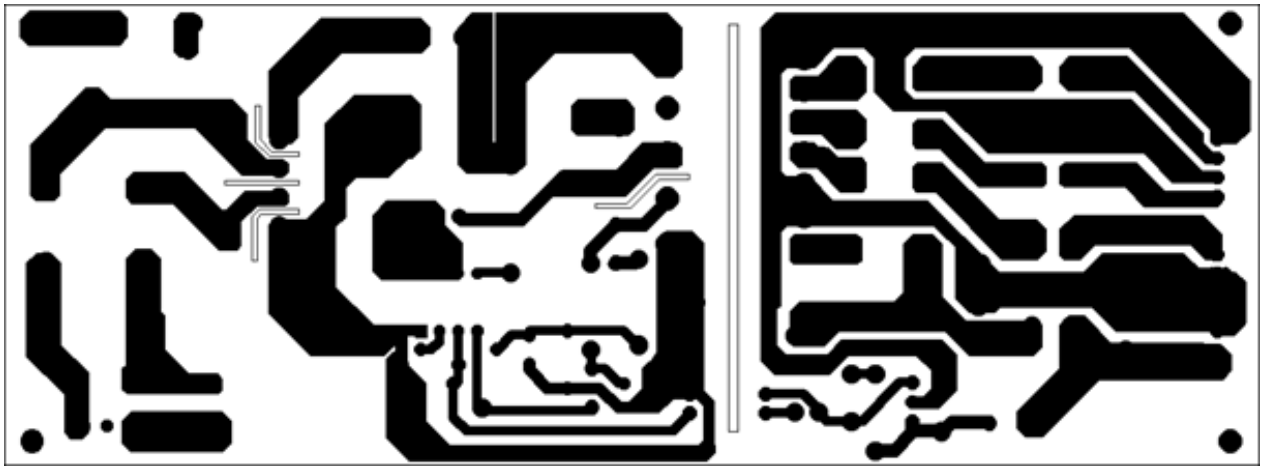
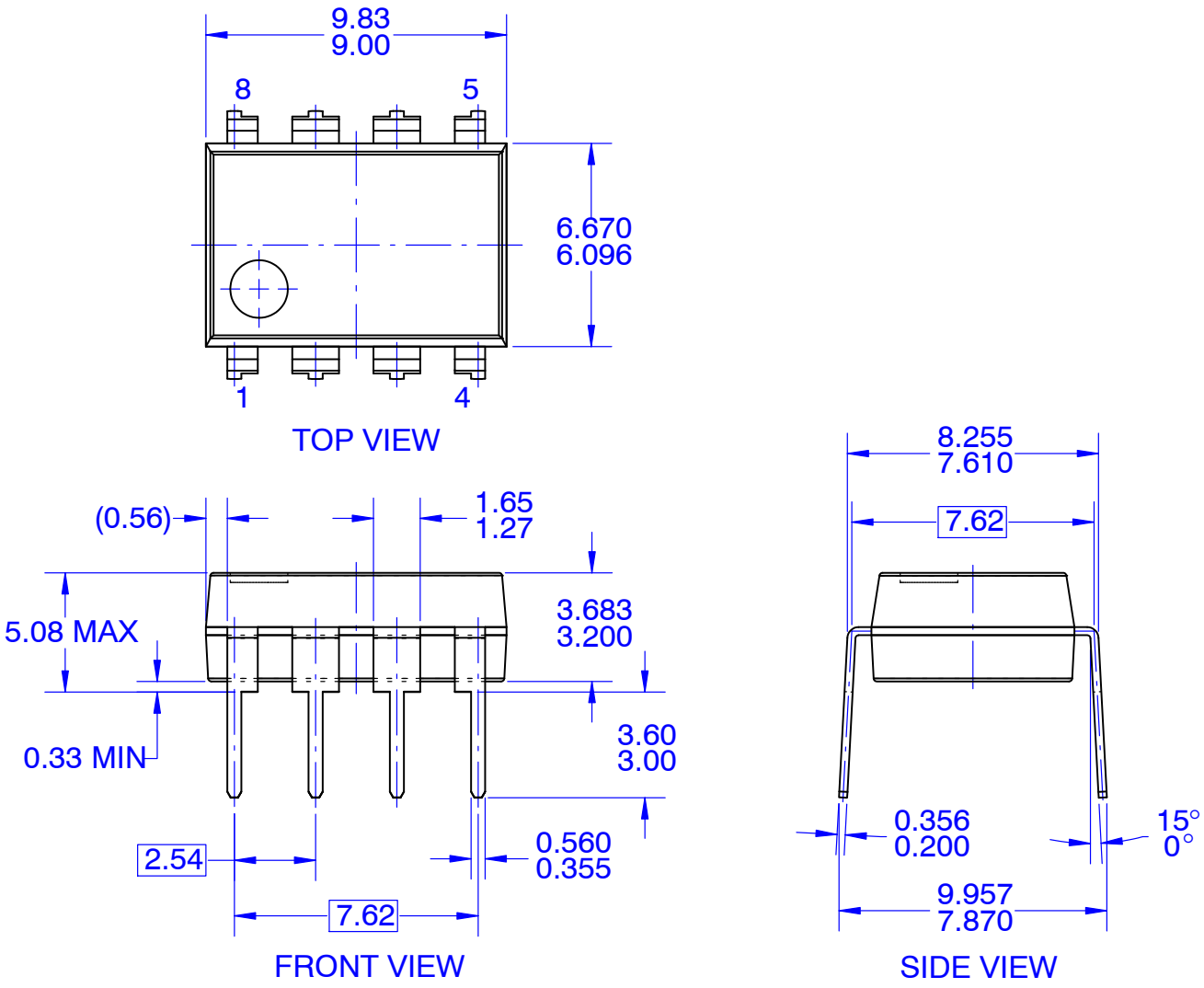


Figure 26. Bottom Image of PCB

PACKAGE DIMENSIONS

PDIP8 9.42x6.38, 2.54P
CASE 646CM
ISSUE O



NOTES:
A. CONFORMS TO JEDEC MS−001, VARIATION BA
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M−2009

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative