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FAIRCHILD SEMICONDUCTOR®

February 2016

FSL137H
Green Mode Fairchild Power Switch (FPS™)

Features

- Built-in 5ms Soft-Start Function
- Internal Avalanche Rugged 700V SenseFET
- Low Audio Noise
- High-Voltage Startup
- Fixed PWM Frequency at 100KHz
- Linearly Decreasing PWM Frequency to 18KHz
- Peak-Current-Mode Control
- Cycle-by-Cycle Current Limiting
- Leading-Edge Blanking (LEB)
- Synchronized Slope Compensation
- Internal Open-loop Protection (OLP)
- V_{DD} Under-Voltage Lockout (UVLO)
- V_{DD} Over-Voltage Protection (OVP)
- Constant Power Limit (Full AC Input Range)
- Internal OTP Sensor with Hysteresis

Applications

General-purpose switch-mode power supplies and flyback power converters, including:

- SMPS for VCR, SVR, STB, DVD & VCD Player, Printer, Facsimile, & Scanner
- Adapter for Camcorder

Description

The highly integrated FSL137H consists of an integrated current mode Pulse Width Modulator (PWM) and an avalanche-rugged 700V SenseFET. It is specifically designed for high-performance offline Switch Mode Power Supplies (SMPS) with minimal external components.

The integrated PWM controller features include a proprietary green-mode function that provides off-time modulation to linearly decrease the switching frequency at light-load conditions to minimize standby power consumption. To avoid acoustic noise problems, the minimum PWM frequency is set above 18KHz. The green-mode function enables the power supply to meet international power conservation requirements. With the internal high-voltage startup circuitry, the power loss due to bleeding resistors is also eliminated. To further reduce power consumption, the PWM controller is manufactured using the BiCMOS process, which allows an operating current of only 3.5mA.

The FSL137H built-in synchronized slope compensation achieves stable peak-current-mode control. The proprietary external line compensation ensures constant output power limit over a wide AC input voltage range, from $90V_{AC}$ to $264V_{AC}$.

The FSL137H provides many protection functions. In addition to cycle-by-cycle current limiting, the internal open-loop protection circuit ensures safety when an open-loop or output short-circuit failure occurs. PWM output is disabled until V_{DD} drops below the UVLO lower limit, when the controller starts up again. As long as V_{DD} exceeds ~28V, the internal OVP circuit is triggered.

Compared to a discrete MOSFET and controller or RCC switching converter solution, the FSL137H reduces total component count, design size, and weight while increasing efficiency, productivity, and system reliability. These devices provide a basic platform well suited for design of cost-effective flyback converters.

Ordering Information

Part Number	SenseFET	Operating Temperature Range	Package	Packing Method
FSL137HNY	3.0A 700V	-40°C to +105°C	8-Pin Dual In-Line Package (DIP)	Tube

Application Diagram

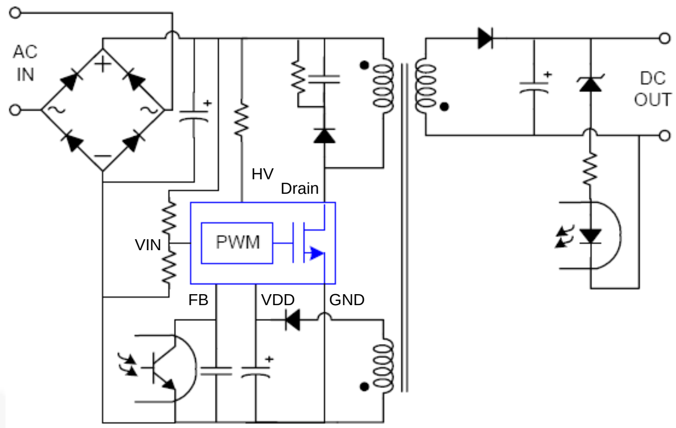


Figure 1. Typical Flyback Application

Output Power Table[1]

Product	$230V_{AC} \pm 15\%$[2]		$85\text{-}265V_{AC}$	
	Adapter[3]	Open Frame[4]	Adapter[3]	Open Frame[4]
FSL137H	17.5W	25W	13W	19W

Notes:

1. The maximum output power can be limited by junction temperature.
2. 230 V_{AC} or 100/115 V_{AC} with doublers.
3. Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sink, at T_A=50°C ambient.
4. Maximum practical continuous power in an open-frame design with sufficient drain pattern as a heat sink, at T_A=50°C ambient.

Internal Block Diagram

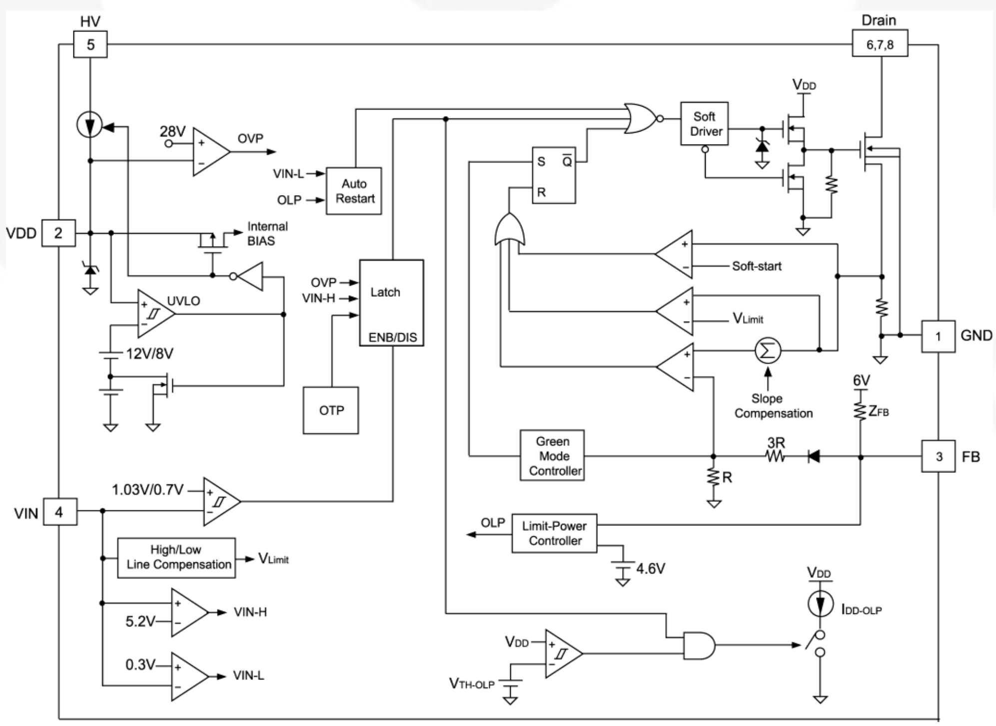
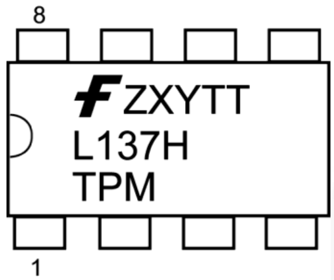


Figure 2. Internal Block Diagram

Pin Configuration



F – Fairchild Logo
Z – Plant Code
X – 1-Digit Year Code
Y – 1-Digit Week Code
TT – 2-Digit Die Run Code
T – Package Type (N: DIP)
P – Y: Green Package
M – Manufacture Flow Code

Figure 3. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	GND	**Ground**. SenseFET source terminal on primary side and internal controller ground.
2	VDD	**Power Supply**. The internal protection circuit disables PWM output as long as V_{DD} exceeds the OVP trigger point.
3	FB	**Feedback**. The signal from the external compensation circuit is fed into this pin. The PWM duty cycle is determined in response to the signal on this pin and the internal current-sense signal.
4	VIN	**Line-Voltage Detection**. The line-voltage detection is used for brownout protection with hysteresis and constant output power limit over universal AC input range. This pin has additional protections that are pull-HIGH latch and pull-low auto recovery, depending on the application.
5	HV	**Startup**. For startup, this pin is pulled HIGH to the line input or bulk capacitor via resistors.
6	Drain	**SenseFET Drain**. High-voltage power SenseFET drain connection.
7	Drain	**SenseFET Drain**. High-voltage power SenseFET drain connection.
8	Drain	**SenseFET Drain**. High-voltage power SenseFET drain connection.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DRAIN}	Drain Pin Voltage(5, 6)			700	V
I_{DM}	Drain Current Pulsed(7)			12	A
E_{AS}	Single Pulsed Avalanche Energy(8)			230	mJ
V_{VDD}	DC Supply Voltage			30	V
V_{FB}	FB Pin Input Voltage		-0.3	7.0	V
V_{VIN}	VIN Pin Input Voltage		-0.3	7.0	V
V_{HV}	HV Pin Input Voltage			700	V
P_D	Power Dissipation ($T_A < 50°C$)			1.5	W
θ_{JA}	Junction-to-Air Thermal Resistance			80	°C/W
Ψ_{JT}	Junction-to-Top Thermal Resistance(9)			35	°C/W
T_J	Operating Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range		-55	150	°C
T_L	Lead Temperature (Wave Soldering or IR, 10 Seconds)			+260	°C
ESD	Electrostatic Discharge Capability, All Pins Except HV Pin(10)	Human Body Model: JESD22-A114		4.5	kV
		Charged Device Model: JESD22-C101		1.5	

Notes:
5. All voltage values, except differential voltages, are given with respect to the network ground terminal.
6. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
7. Non-repetitive rating: Pulse width is limited by maximum junction temperature.
8. L = 51mH, starting T_J = 25°C.
9. Measured on the package top surface.
10. All pins including HV pin: HBM=1kV, CDM=1.25kV

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_A	Operating Ambient Temperature		-40		+105	°C

Electrical Characteristics

V_{DD}=15V, T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SenseFET Section(11)						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V	700			V
I_{DSS}	Zero-Gate-Voltage Drain Current	V_{DS} = 700V, V_{GS} = 0V		0.5	50.0	µA
		V_{DS} = 560V, V_{GS} = 0V, T_A = 125°C		1	200	
$R_{DS(ON)}$	Drain-Source On-State Resistance(12)	V_{GS} = 10V, I_D = 0.5A		4.00	4.75	Ω
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		315	410	pF
C_{OSS}	Output Capacitance	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		47	61	pF
C_{RSS}	Reverse Transfer Capacitance	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		9	14	pF
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = 350V, I_D = 1.0A		11.2	33.0	ns
t_r	Rise Time	V_{DS} = 350V, I_D = 1.0A		34	78	ns
$t_{d(off)}$	Turn-Off Delay Time	V_{DS} = 350V, I_D = 1.0A		28.2	67.0	ns
t_f	Fall Time	V_{DS} = 350V, I_D = 1.0A		32	74	ns
V_{DD} Section						
V_{OP}	Continuously Operating Voltage				22	V
V_{DD-ON}	Start Threshold Voltage		11	12	13	V
V_{DD-OFF}	Minimum Operating Voltage		7	8	9	V
I_{DD-ST}	Startup Current	V_{DD-ON} – 0.16V			30	µA
I_{DD-OP}	Operating Supply Current	V_{DD} = 15V, V_{FB} = 3V	3.0	3.5	4.0	mA
I_{DD-BM}	Green-Mode Operating Supply Current	V_{FB} = V_{FB-G}		2		mA
I_{DD-OLP}	Internal Sink Current	V_{TH-OLP}+0.1V	30	60	90	µA
V_{TH-OLP}	I_{DD-OLP} Off Voltage		5	6	7	V
V_{DD-OVP}	V_{DD} Over-Voltage Protection		27	28	29	V
$t_{D-VDDOVP}$	V_{DD} Over-Voltage Protection Debounce Time		75	130	200	µs
HV Section						
I_{HV}	Maximum Current Drawn from HV Pin	HV 120V_{DC}, V_{DD} = 0V with 10µF	1.5	3.5	5.0	mA
I_{HV-LC}	Leakage Current After Startup	HV = 700V, V_{DD} = V_{DD-OFF}+1V		1	20	µA
Oscillator Section						
f_{OSC}	Frequency in Nominal Mode	Center Frequency	94	100	106	kHz
f_{OSC-G}	Green-Mode Frequency		14	18	22	kHz
D_{MAX}	Maximum Duty Cycle			85		%
f_{DV}	Frequency Variation vs. V_{DD} Deviation	V_{DD} = 9V to 22V			5	%
f_{DT}	Frequency Variation vs. Temperature Deviation(11)	T_A = -40 to +105°C			5	%

Continued on the following page…

Electrical Characteristics (Continued)

V_{DD}=15V, T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IN} Section						
V_{IN-ON}	PWM Turn-on Threshold Voltage		0.98	1.03	1.08	V
V_{IN-RL}	Release Latch Voltage		0.65	0.70	0.75	V
V_{IN-H}	Pull HIGH Latch Trigger Level		4.9	5.2	5.5	V
t_{IN-H}	Pull HIGH Latch Debounce Time			100		µs
V_{IN-L}	Pull LOW Auto Recovery Trigger Level		0.2	0.3	0.4	V
Feedback Input Section						
A_V	FB Voltage to Current-Sense Attenuation			1/4.0		V/V
Z_{FB}	Input Impedance			9.5		kΩ
$V_{FB-OPEN}$	Output High Voltage		5			V
V_{FB-OLP}	FB Open-Loop Trigger Level		4.4	4.6	4.8	V
t_{D-OLP}	Delay Time of FB Pin Open-loop Protection		50	56	59	ms
V_{FB-N}	Green-Mode Entry FB Voltage		2.3	2.5	2.7	V
V_{FB-G}	Green-Mode Ending FB Voltage			V_{FB-N} - 0.1		V
V_{FB-ZDC}	Zero Duty Cycle FB Voltage		1.9	2.1	2.3	V

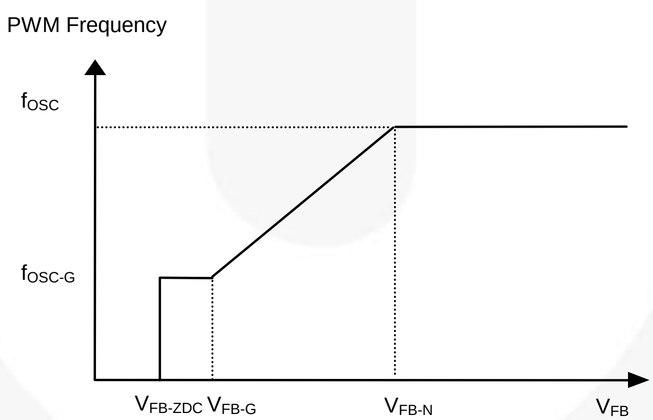


Figure 4. V_{FB} vs. PWM Frequency

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Current-Sense Section						
I_{LIM} at V_{IN} = 1.2V	Peak Current Limit	V_{IN} = 1.2V	0.74	0.84	0.94	A
I_{LIM} at V_{IN} = 3.6V	Peak Current Limit	V_{IN} = 3.6V	0.64	0.74	0.84	A
t_{SS}	Period during Soft Startup Time[11]		4.5	5.0	5.5	ms
Over-Temperature Protection Section (OTP)						
T_{OTP}	Protection Junction Temperature[11,13]			142		°C

Notes:

11. These parameters, although guaranteed, are not 100% tested in production.
12. Pulse test: pulse width ≤ 300µs, duty ≤ 2%.
13. When activated, the output is disabled and the latch is turned off.

Typical Characteristics

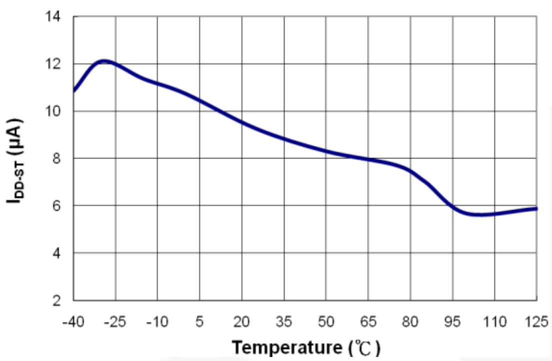


Figure 5. I_{DD-ST} vs. Temperature

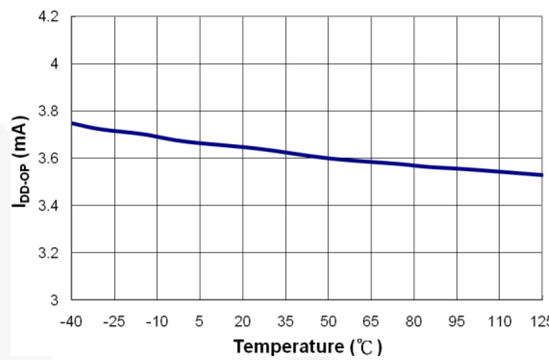


Figure 6. I_{DD-OP} vs. Temperature

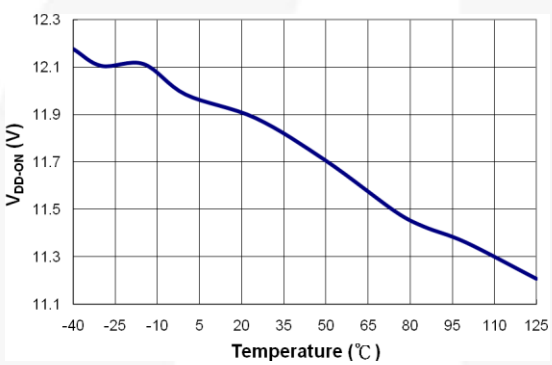


Figure 7. V_{DD-ON} vs. Temperature

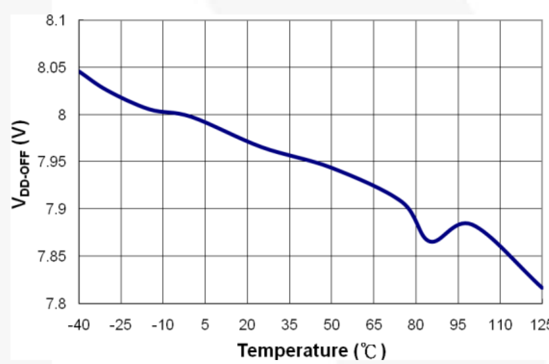


Figure 8. V_{DD-OFF} vs. Temperature

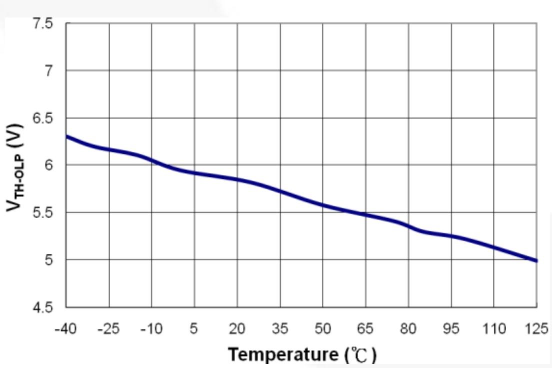


Figure 9. V_{TH-OLP} vs. Temperature

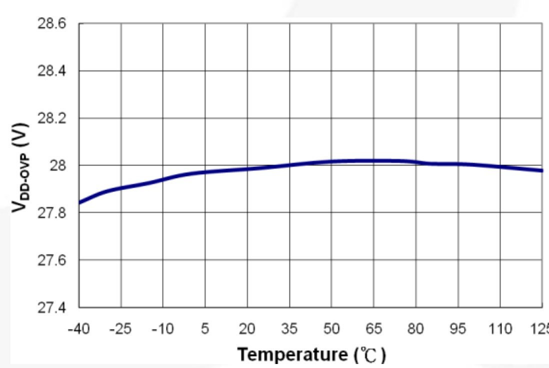


Figure 10. V_{DD-OVP} vs. Temperature

Typical Characteristics

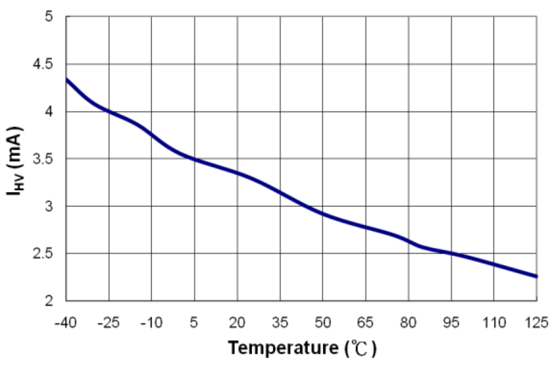


Figure 11. I_{HV} vs. Temperature

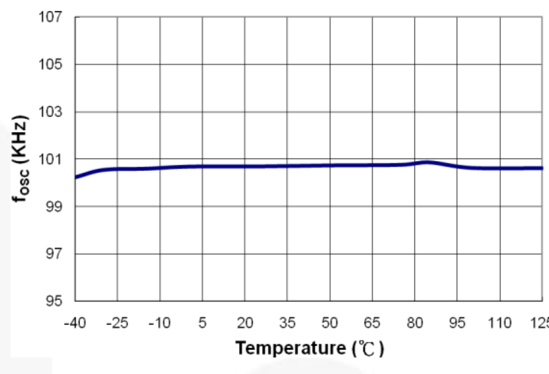


Figure 12. f_{OSC} vs. Temperature

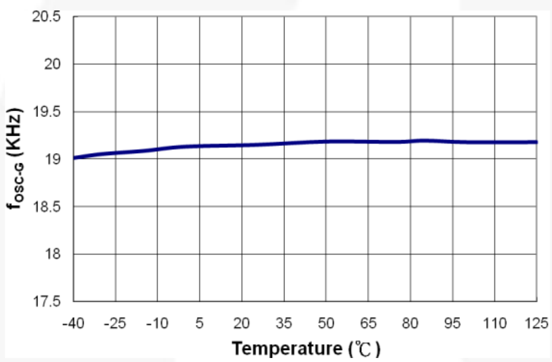


Figure 13. f_{OSC-G} vs. Temperature

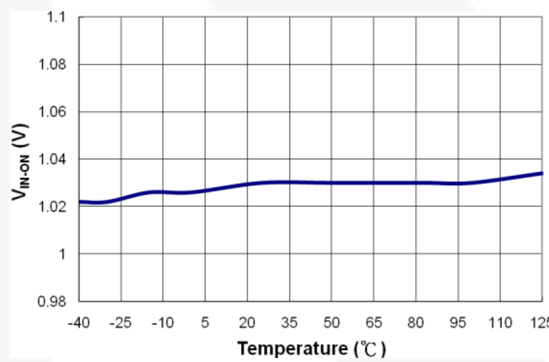


Figure 14. V_{IN-ON} vs. Temperature

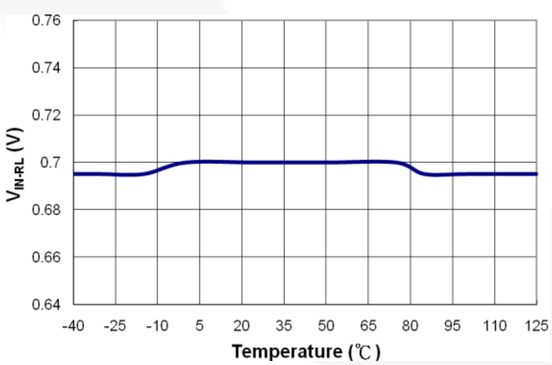


Figure 15. V_{IN-RL} vs. Temperature

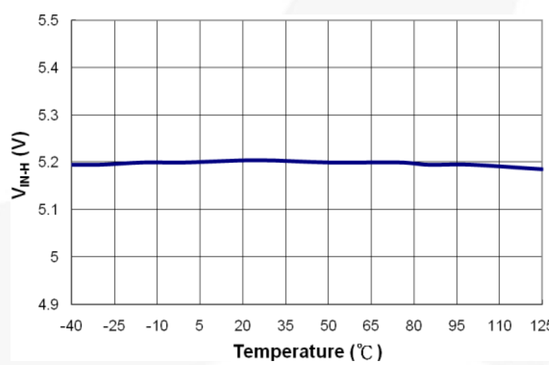


Figure 16. V_{IN-H} vs. Temperature

Typical Characteristics

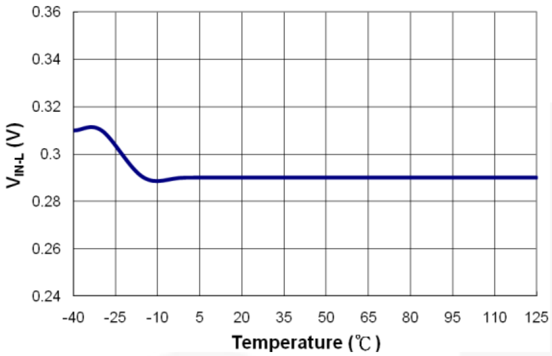


Figure 17. V_{IN-L} vs. Temperature

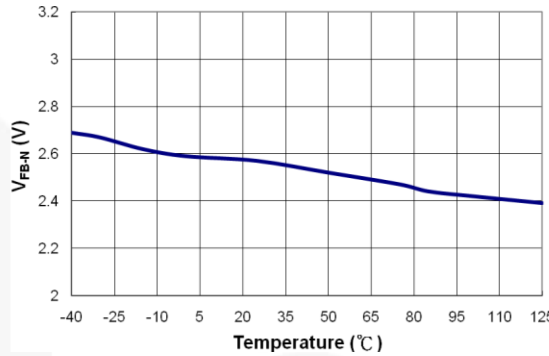


Figure 18. V_{FB-N} vs. Temperature

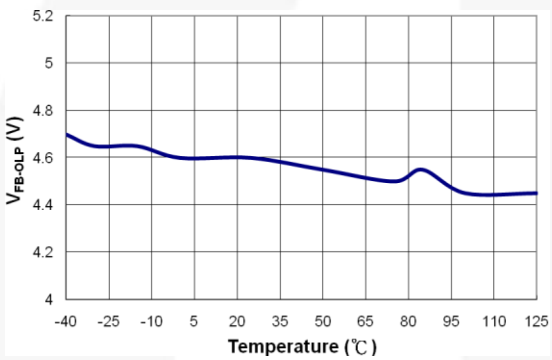


Figure 19. V_{FB-OLP} vs. Temperature

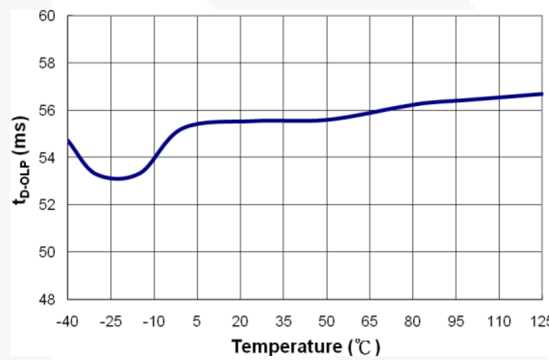


Figure 20. t_{D-OLP} vs. Temperature

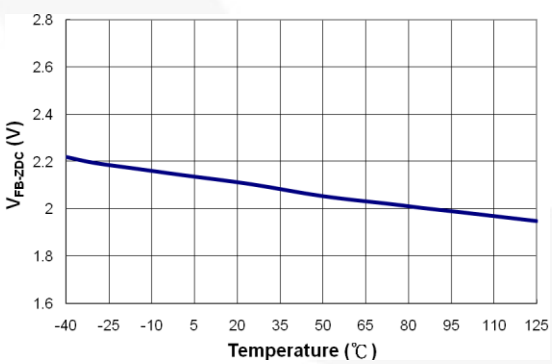


Figure 21. V_{FB-ZDC} vs. Temperature

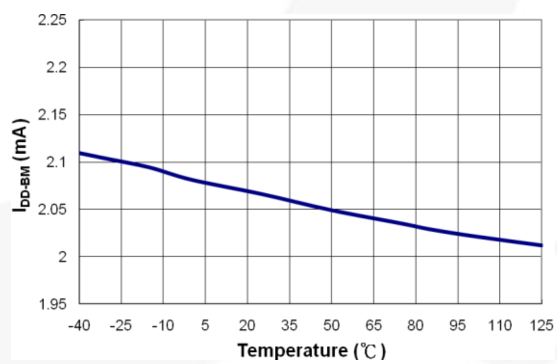


Figure 22. I_{DD-BM} vs. Temperature

Functional Description

Startup Operation

For startup, the HV pin is connected to the line input or bulk capacitor through the external resistor, R_{HV}, as shown in Figure 23. Typical startup current drawn from the HV pin is 3.5mA and it charges the V_{DD} capacitor through the resistor R_{HV}. The startup current turns off when the V_{DD} capacitor voltage reaches V_{DD-ON}. The V_{DD} capacitor maintains V_{DD} until the auxiliary winding of the transformer provides the operating current.

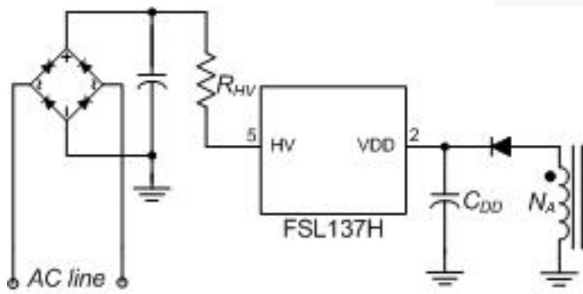


Figure 23. Startup Circuit

Slope Compensation

FSL137H is designed for flyback power converters. The peak-current-mode control is used to optimize system performance. Slope compensation is added to stabilize the current loop. FSL137H inserts a synchronized, positively sloped ramp at each switching cycle.

Soft-Start

The FSL137H has internal soft-start circuit that slowly increases the SenseFET current after startup. The typical soft-start time is 5ms during which the V_{Limit} level is increased in six steps to smoothly establish the required output voltage, as shown in Figure 24. It also helps to prevent transformer saturation and reduce the stress on the secondary diode during startup.

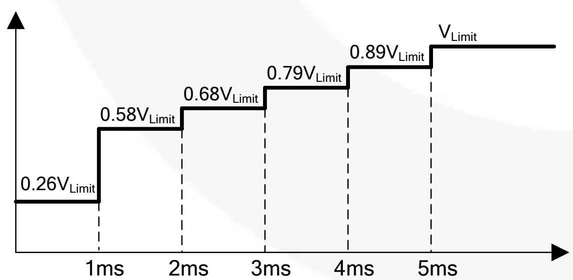


Figure 24. Soft-Start Function

Green-Mode Operation

The FSL137H uses feedback voltage (V_{FB}) as an indicator of the output load and modulates the PWM frequency, as shown in Figure 25, such that the switching frequency decreases as load decreases. In heavy load conditions, the switching frequency is 100kHz. Once V_{FB} decreases below V_{FB-N} (2.5V), the PWM frequency starts to linearly decrease from 100kHz to 18kHz to reduce the switching losses. As V_{FB} decreases below V_{FB-G} (2.4V), the switching frequency is fixed at 18kHz and FSL137H enters into “deep” green mode to reduce the standby power consumption. As V_{FB} decreases below V_{FB-ZDC} (2.1V), FSL137H enters into burst-mode operation. When V_{FB} drops below V_{FB-ZDC}, FSL137H stops switching and the output voltage starts to drop, which causes the feedback voltage to rise. Once V_{FB} rises above V_{FB-ZDC}, switching resumes. Burst mode alternately enables and disables switching, thereby reducing switching loss to improve power saving, as shown in Figure 26.

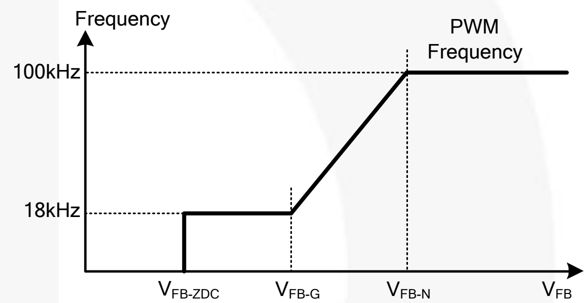


Figure 25. PWM Frequency

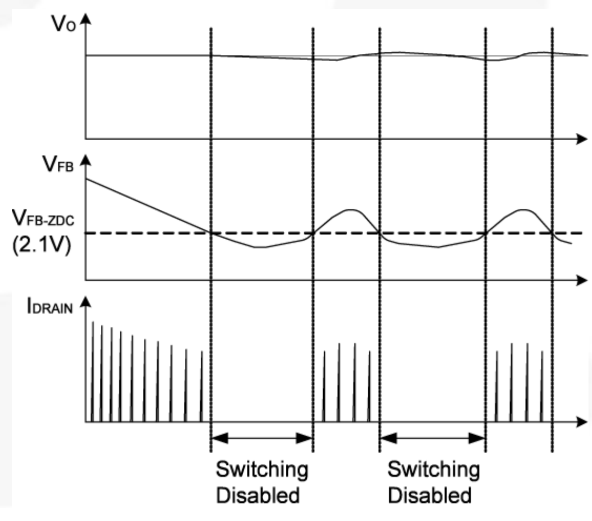


Figure 26. Burst Mode Operation

Constant Power Control

To limit the output power of the converter constantly, high/low line compensation is included. Sensing the converter input voltage through the VIN pin, the high/low line compensation function generates a relative peak-current-limit threshold voltage for constant power control, as shown in Figure 27.

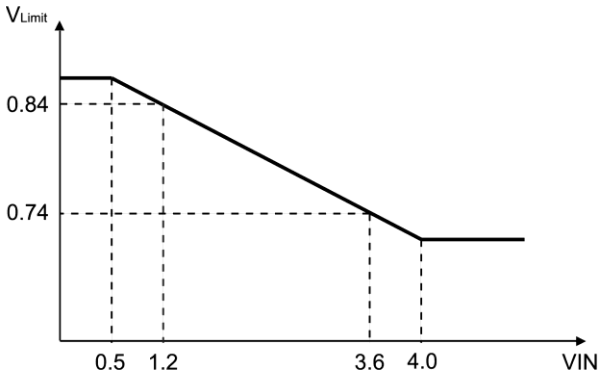


Figure 27. Constant Power Control

Protections

The FSL137H provides full protection functions to prevent the power supply and the load from being damaged. The protection features include:

Latch / Auto Recovery Function

The FSL137H provides additional protections by the VIN pin, such as pull-HIGH latch and pull-LOW auto recovery that depend on the application. As shown in Figure 28, when V_{IN} is higher than 5.2V, FSL137H is latched until the V_{DD} is discharged. FSL137H is in auto recovery when V_{IN} is lower than 0.3V.

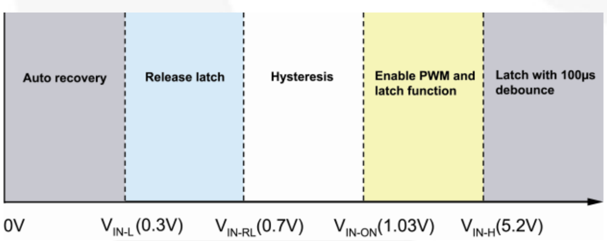


Figure 28. VIN Pin Function

Open-Loop / Overload Protection (OLP)

When the upper branch of the voltage divider for the shunt regulator (KA431 shown) is broken, as shown in Figure 29, or over current or output short occurs. There is no current flowing through the opto-coupler transistor, which pulls up the feedback voltage to 6V. When the feedback voltage is above 4.6V for longer than 56ms, OLP is triggered. This protection is also triggered when the SMPS output drops below the nominal value longer than 56ms due to the overload condition.

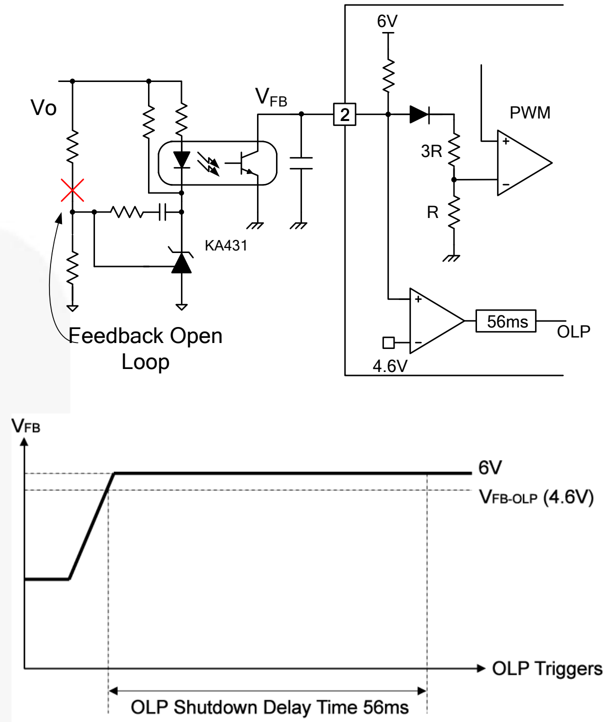


Figure 29. OLP Operation

V_{DD} Over-Voltage Protection (OVP)

V_{DD} over-voltage protection prevents IC damage caused by over voltage on the V_{DD} pin. The OVP is triggered when V_{DD} reaches 28V. It has a debounce time (typically 130µs) to prevent false trigger by switching noise.

Over-Temperature Protection (OTP)

The SenseFET and the control IC are integrated, making it easier to detect the temperature of the SenseFET. When the temperature exceeds approximately 142°C, thermal shutdown is activated.

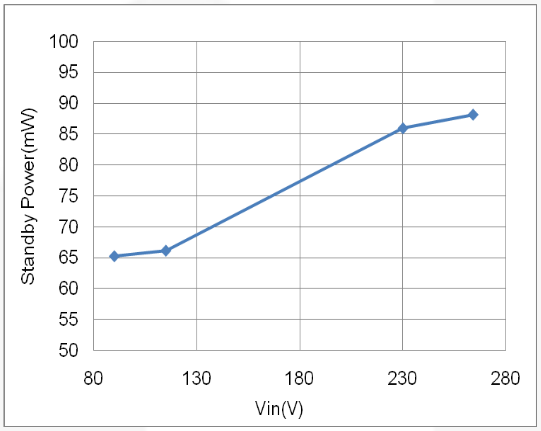
Typical Application Circuit

Application	Fairchild Devices	Input Voltage Range	Output
Adapter	FSL137H	90~264Vac	12V/1A (12W)

Features

- High efficiency (>77.76% at full load) meeting Energy Star V2.0 regulation with enough margin
- Standby power <100mW at no-load condition
- Provides full protection functions:

OVP	OTP	OLP	VIN-H	VIN-L
Latch	Latch	Auto restart	Latch	Auto restart



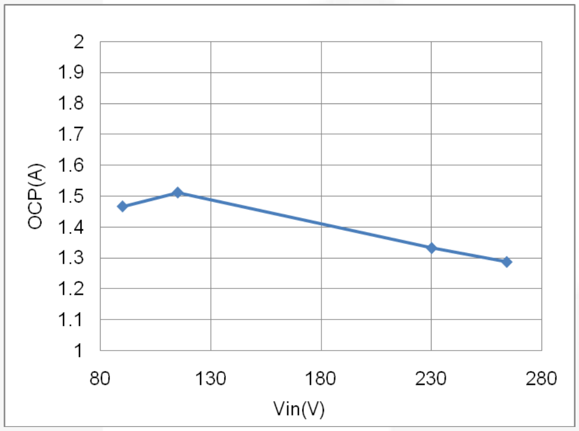


Figure 30. Measured Standby Power and OCP

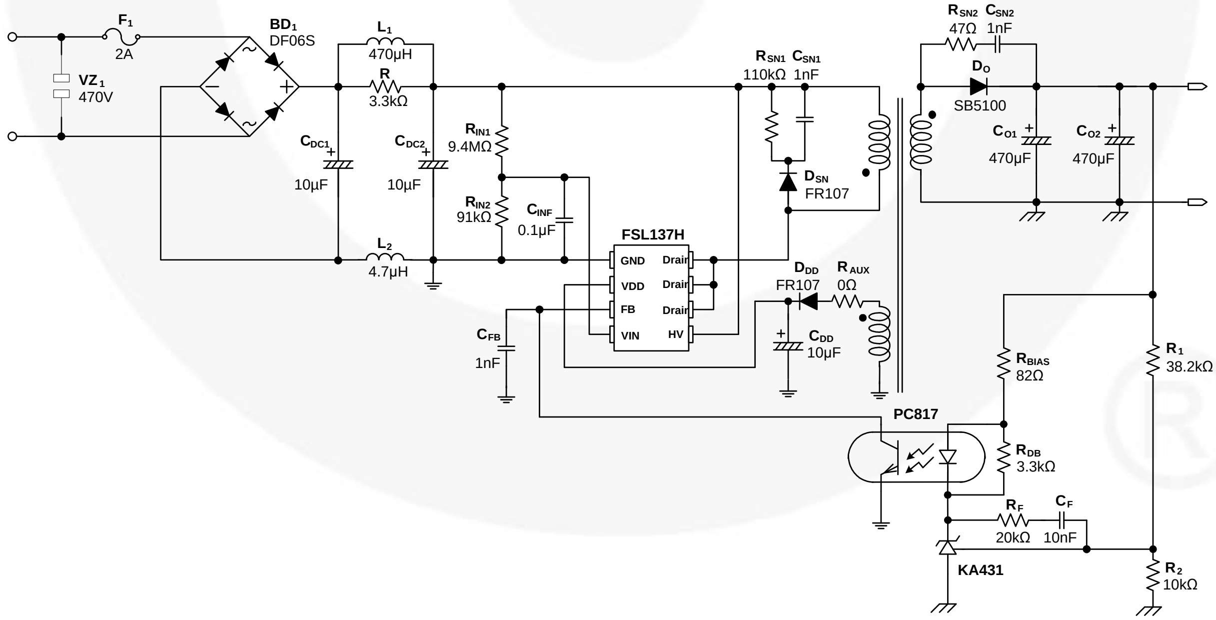


Figure 31. Schematic of Typical Application Circuit

Typical Application Circuit (Continued)

Transformer Specification

- Core: EE16
- Bobbin: EE16

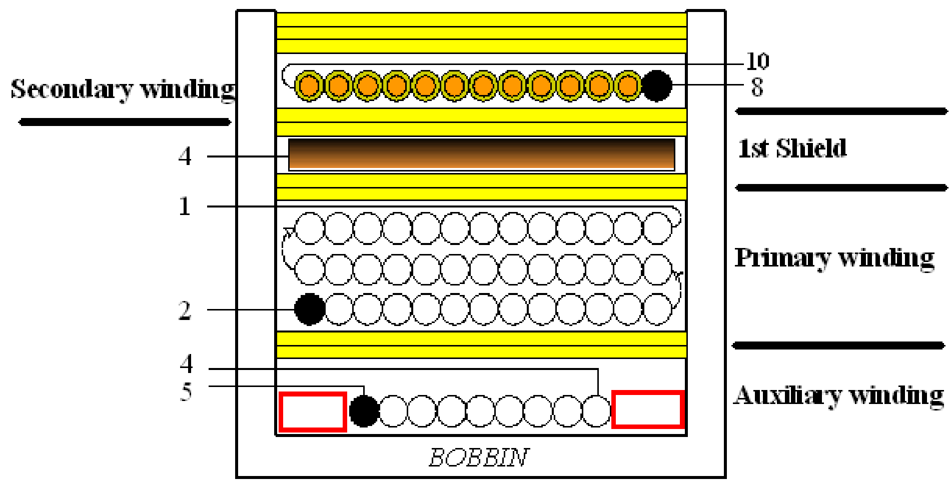
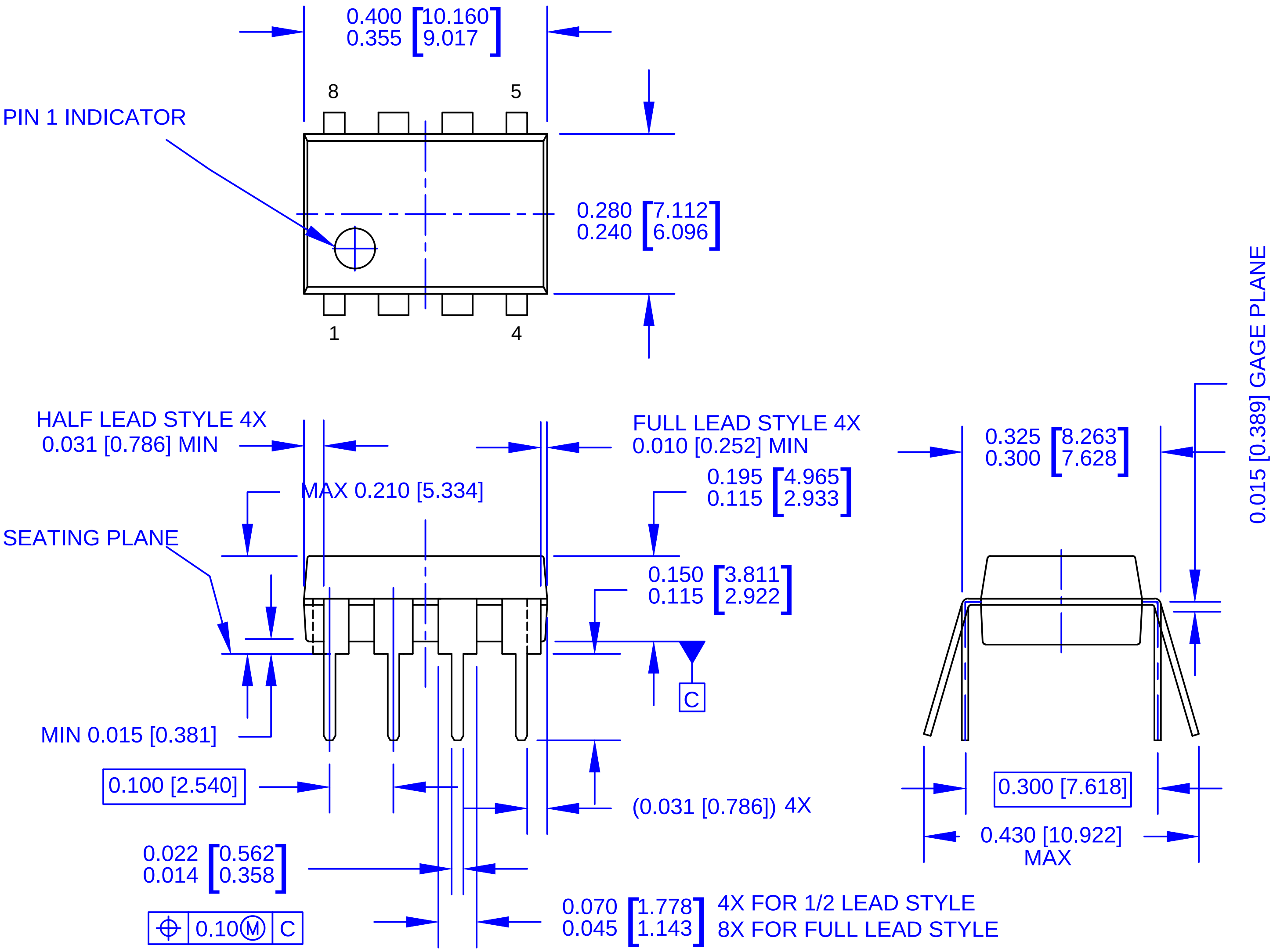


Figure 32. Transformer Diagram

NO.	TERMINAL		WIRE	Ts
	S	F		
W1	5	4	2UEW 0.3*1	13
W2	2	1	2UEW 0.26*1	75
W3	4	-	COPPER SHIELD	1.2
W4	8	10	TEX-E 0.35*1	13
			CORE ROUNDING TAPE	3
Primary-Side Inductance=600μH ± 5%				
Primary-Side Effective Leakage<20μH ± 5%				



NOTES:

A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA WHICH DEFINES 2 VERSIONS OF THE PACKAGE TERMINAL STYLE WHICH ARE SHOWN HERE.

B) CONTROLING DIMS ARE IN INCHES

C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-2009

E) DRAWING FILENAME AND REVSION: MKT-N08MREV2.

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