



ON Semiconductor®

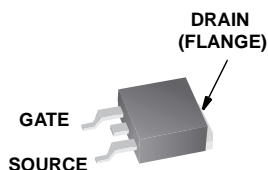
HUF76639S3ST-F085

50A, 100V, 0.026 Ohm, N-Channel, Logic Level UltraFET® Power MOSFET



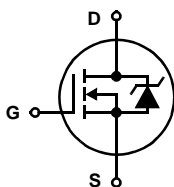
Packaging

JEDEC TO-263AB



HUF76639S3S

Symbol



Features

- Ultra Low On-Resistance
 - $r_{DS(ON)} = 0.026\Omega$, $V_{GS} = 10V$
- Simulation Models
 - Temperature Compensated PSPICE® and SABER™ Electrical Models
 - Spice and SABER Thermal Impedance Models
 - www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Switching Time vs R_{GS} Curves

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF76639S3ST-F085	TO-263AB	76639S

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the variant in tape and reel, e.g., HUF76639S3ST.

Absolute Maximum Ratings $T_C = 25^\circ C$, Unless Otherwise Specified

	HUF76639S3ST_F085	UNITS
Drain to Source Voltage (Note 1)	100	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	100	V
Gate to Source Voltage	± 16	V
Drain Current		
Continuous ($T_C = 25^\circ C$, $V_{GS} = 5V$)	50	A
Continuous ($T_C = 25^\circ C$, $V_{GS} = 10V$) (Figure 2)	51	A
Continuous ($T_C = 100^\circ C$, $V_{GS} = 5V$)	35	A
Continuous ($T_C = 100^\circ C$, $V_{GS} = 4.5V$) (Figure 2)	34	A
Pulsed Drain Current	Figure 4	
Pulsed Avalanche Rating	Figures 6, 17, 18	
Power Dissipation	180	W
Derate Above $25^\circ C$	1.2	W/ $^\circ C$
Operating and Storage Temperature	-55 to 175	$^\circ C$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	300	$^\circ C$
Package Body for 10s, See Techbrief TB334	260	$^\circ C$

NOTES:

1. $T_J = 25^\circ C$ to $150^\circ C$.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

HUF76639S3ST-F085

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$ (Figure 12)	100	-	-	V	
		$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$, $T_C = -40^\circ\text{C}$ (Figure 12)	90	-	-	V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 95\text{V}$, $V_{GS} = 0\text{V}$	-	-	1	μA	
		$V_{DS} = 90\text{V}$, $V_{GS} = 0\text{V}$, $T_C = 150^\circ\text{C}$	-	-	250	μA	
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 16\text{V}$	-	-	± 100	nA	
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$ (Figure 11)	1	-	3	V	
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 51\text{A}$, $V_{GS} = 10\text{V}$ (Figures 9, 10)	-	0.023	0.026	Ω	
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	$R_{\theta JC}$	TO-263	-	-	0.83	$^\circ\text{C/W}$	
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		-	-	62	$^\circ\text{C/W}$	
SWITCHING SPECIFICATIONS ($V_{GS} = 4.5\text{V}$)							
Turn-On Time	t_{ON}	$V_{DD} = 50\text{V}$, $I_D = 34\text{A}$ $V_{GS} = 4.5\text{V}$, $R_{GS} = 12\Omega$ (Figures 15, 21, 22)	-	-	336	ns	
Turn-On Delay Time	$t_{d(ON)}$		-	17	-	ns	
Rise Time	t_r		-	207	-	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	83	-	ns	
Fall Time	t_f		-	136	-	ns	
Turn-Off Time	t_{OFF}		-	-	328	ns	
SWITCHING SPECIFICATIONS ($V_{GS} = 10\text{V}$)							
Turn-On Time	t_{ON}	$V_{DD} = 50\text{V}$, $I_D = 51\text{A}$ $V_{GS} = 10\text{V}$, $R_{GS} = 12\Omega$ (Figures 16, 21, 22)	-	-	96	ns	
Turn-On Delay Time	$t_{d(ON)}$		-	10	-	ns	
Rise Time	t_r		-	55	-	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	151	-	ns	
Fall Time	t_f		-	110	-	ns	
Turn-Off Time	t_{OFF}		-	-	392	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0\text{V}$ to 10V	$V_{DD} = 50\text{V}$, $I_D = 35\text{A}$, $I_{g(REF)} = 1.0\text{mA}$ (Figures 14, 19, 20)	-	71	86	nC
Gate Charge at 5V	$Q_{g(5)}$	$V_{GS} = 0\text{V}$ to 5V		-	39	47	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0\text{V}$ to 1V		-	2.0	2.4	nC
Gate to Source Gate Charge	Q_{gs}			-	6	-	nC
Gate to Drain "Miller" Charge	Q_{gd}			-	19	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$ (Figure 13)	-	2400	-	pF	
Output Capacitance	C_{OSS}		-	520	-	pF	
Reverse Transfer Capacitance	C_{RSS}		-	140	-	pF	

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 35\text{A}$	-	-	1.25	V
		$I_{SD} = 15\text{A}$	-	-	1.0	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 35\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	137	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 35\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	503	nC

Typical Performance Curves

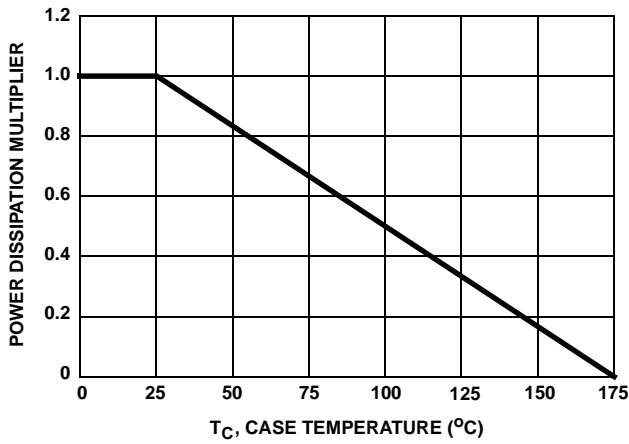


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

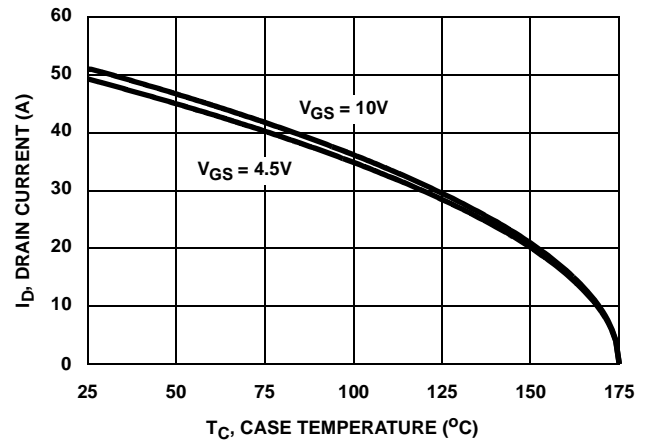


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

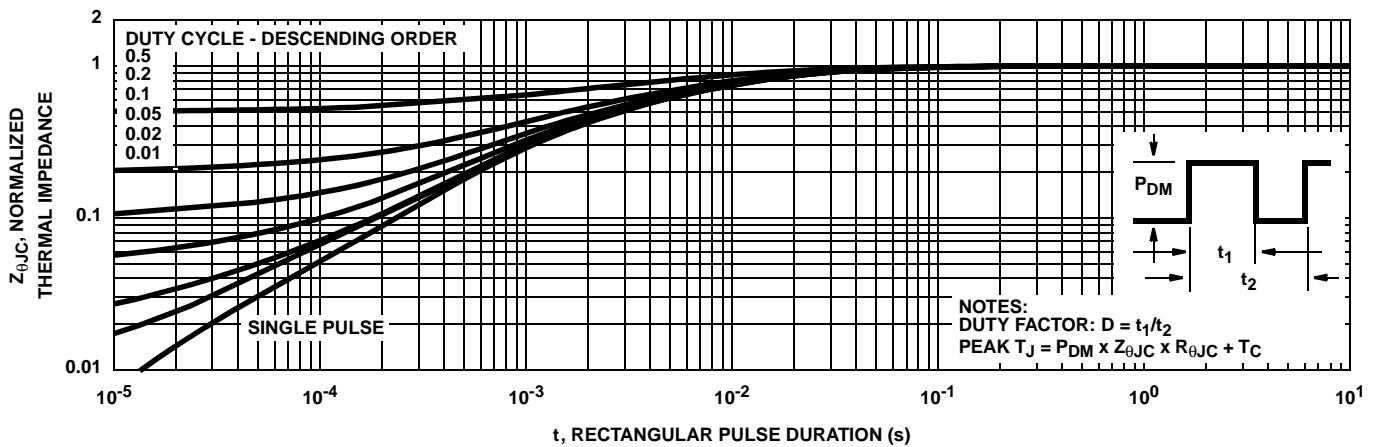


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

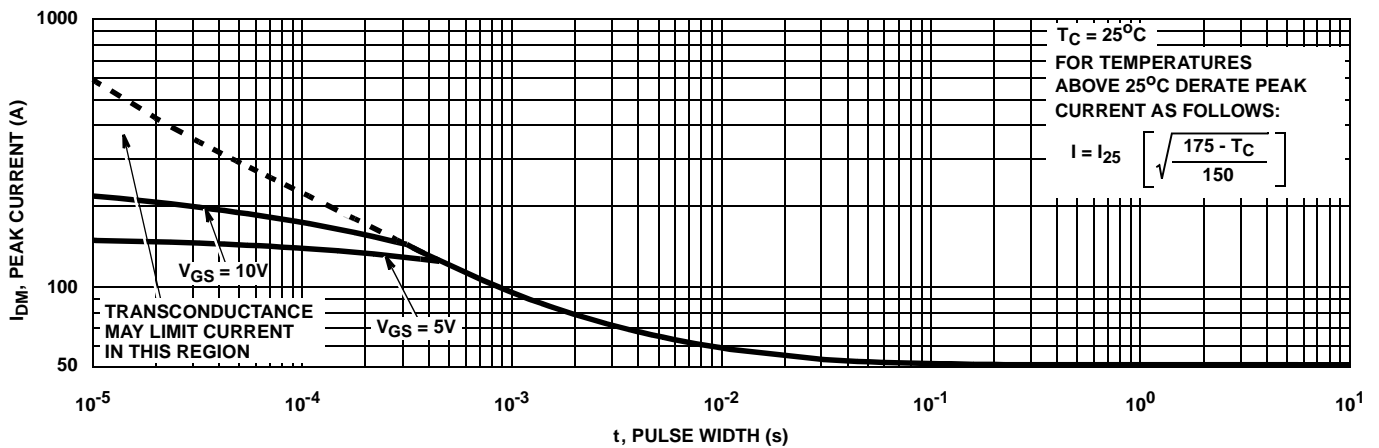


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

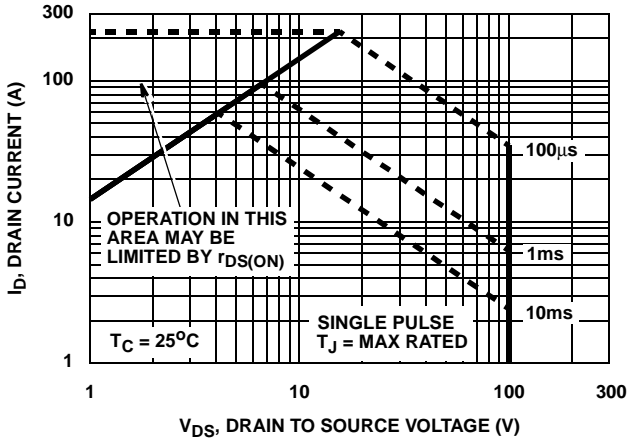


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA

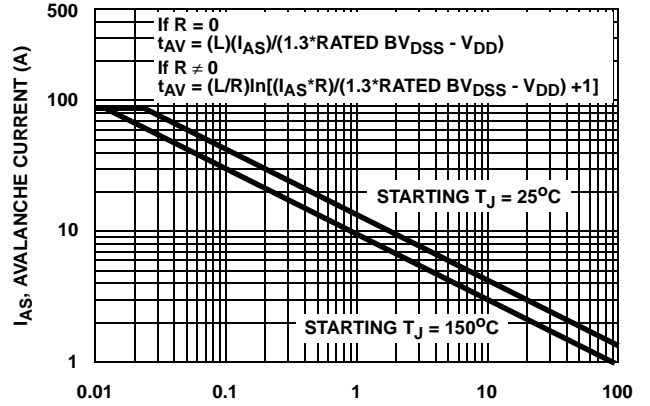


FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

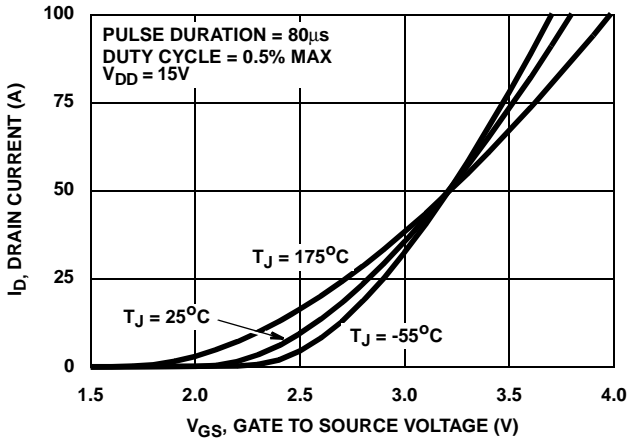


FIGURE 7. TRANSFER CHARACTERISTICS

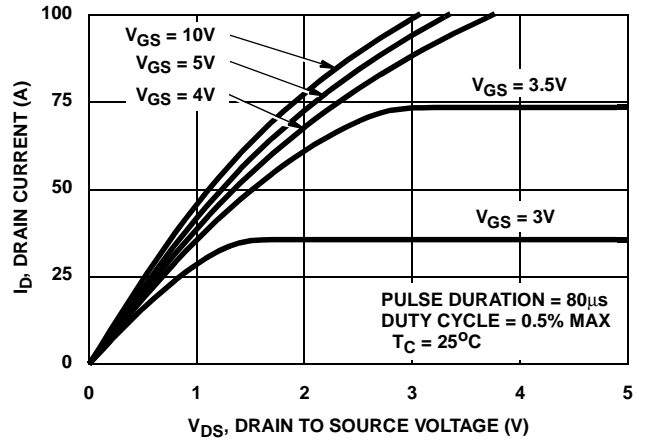


FIGURE 8. SATURATION CHARACTERISTICS

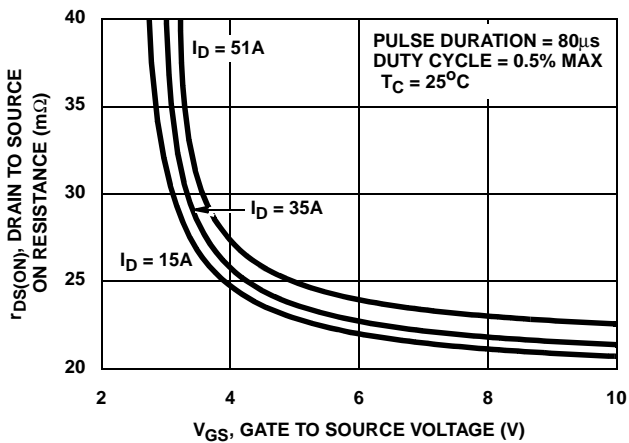


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

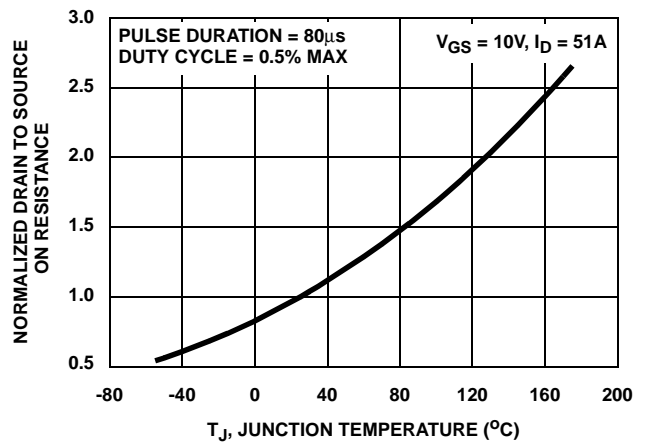


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

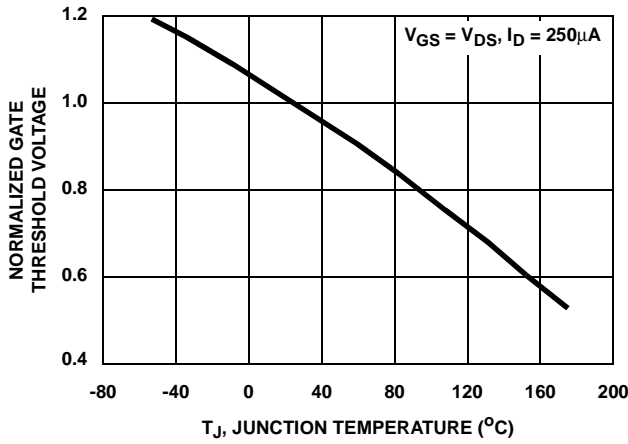


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

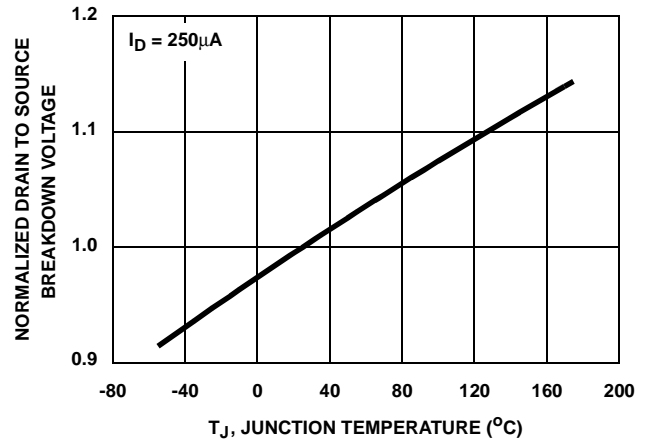


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

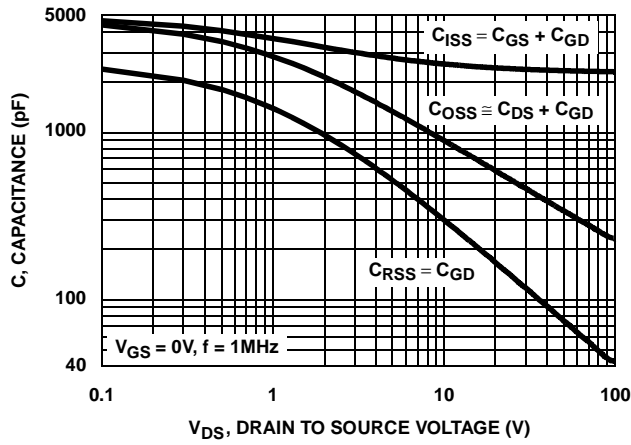


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

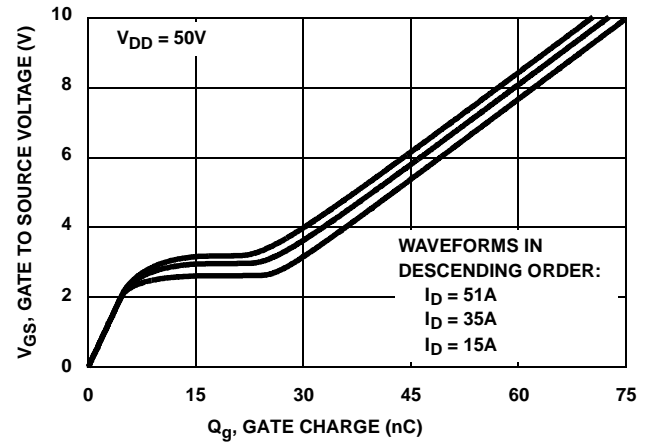


FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

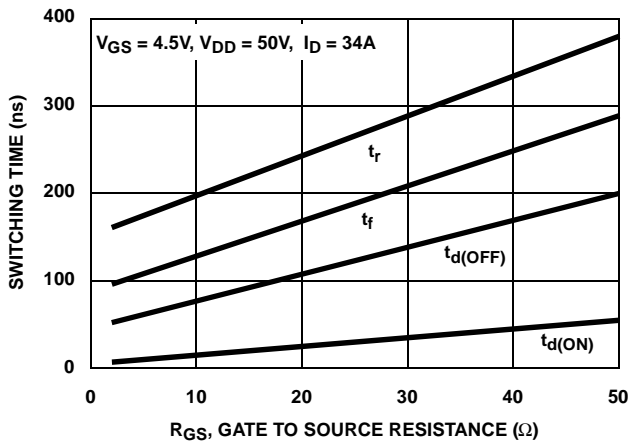


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

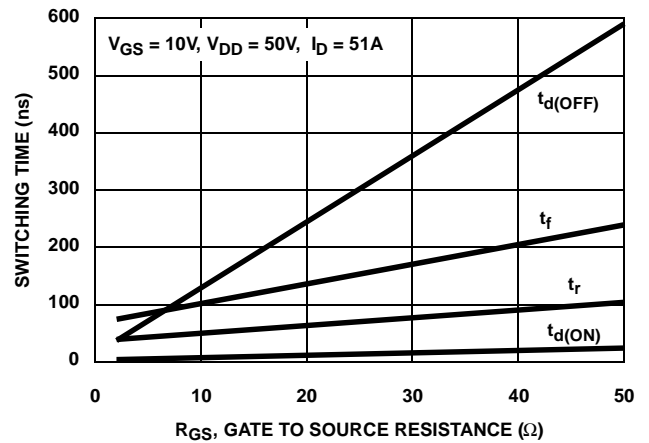


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

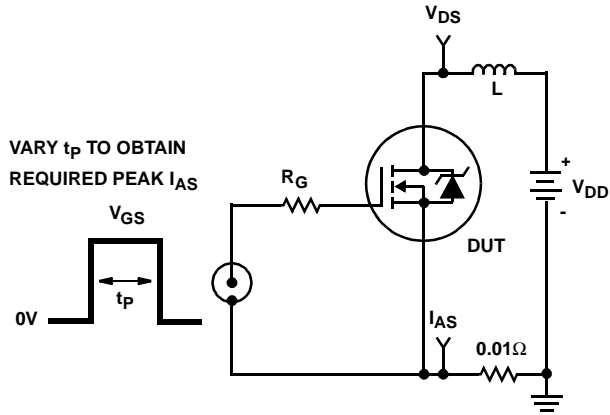


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

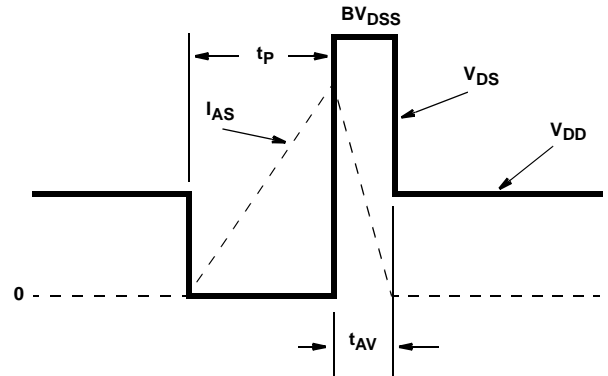


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

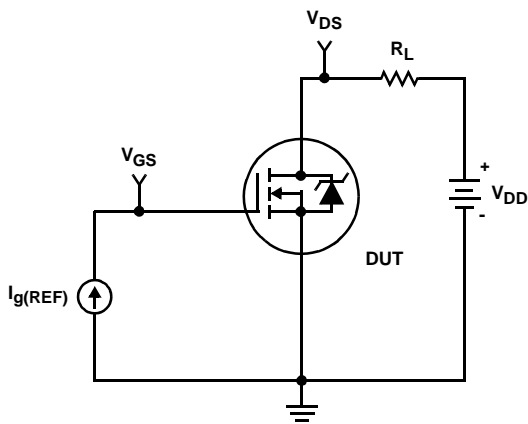


FIGURE 19. GATE CHARGE TEST CIRCUIT

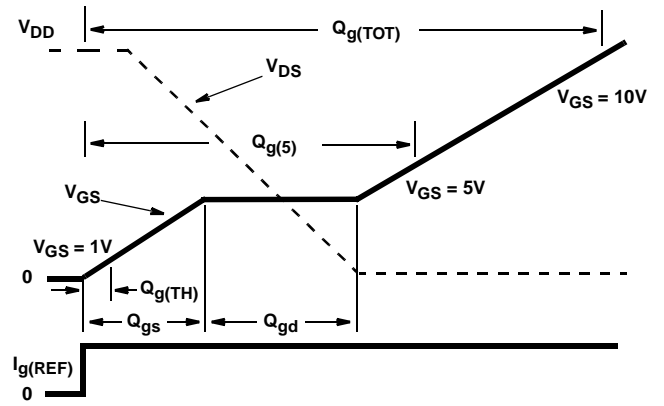


FIGURE 20. GATE CHARGE WAVEFORMS

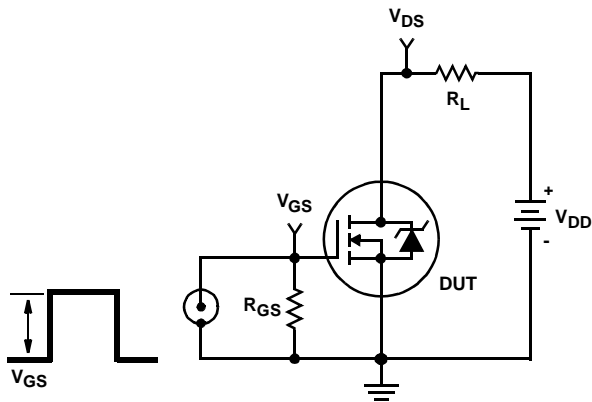


FIGURE 21. SWITCHING TIME TEST CIRCUIT

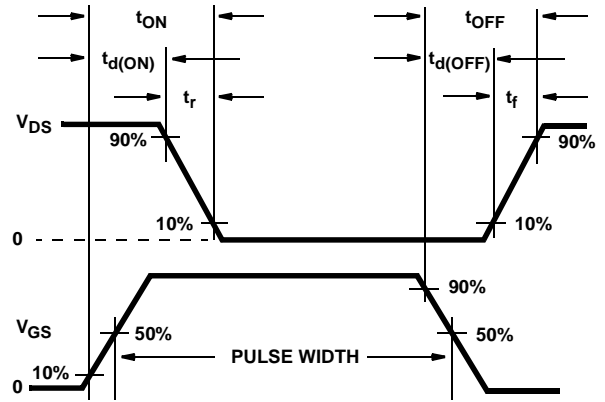


FIGURE 22. SWITCHING TIME WAVEFORM

PSPICE Electrical Model

.SUBCKT HUF76639 2 1 3 ; rev 26 July 1999

CA 12 8 4.2e-9
 CB 15 14 4.2e-9
 CIN 6 8 2.27e-9
 DBODY 7 5 DBODYMOD
 DBREAK 5 11 DBREAKMOD
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 118.2
 EDS 14 8 5 8 1
 EGS 13 8 6 8 1
 ESG 6 10 6 8 1
 EVTHRES 6 21 19 8 1
 EVTEMP 20 6 18 22 1

IT 8 17 1

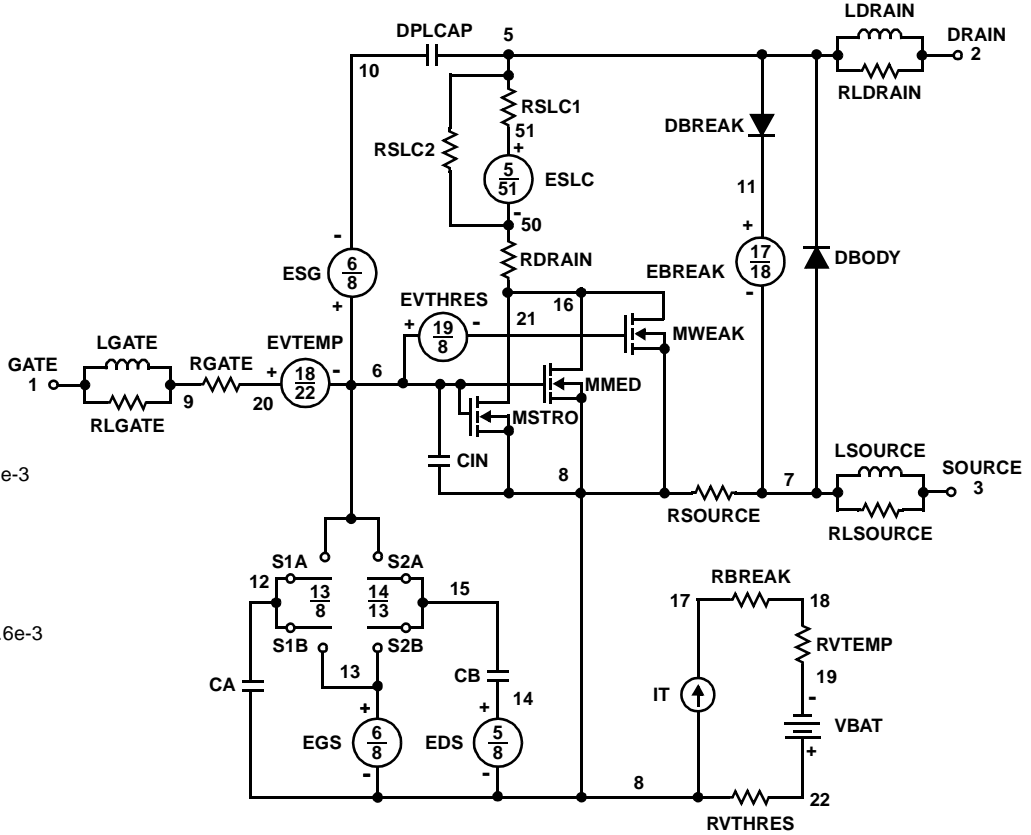
LDRAIN 2 5 1.0e-9
 LGATE 1 9 5.1e-9
 LSOURCE 3 7 3.1e-9

MMED 16 6 8 8 MMEDMOD
 MSTRO 16 6 8 8 MSTROMOD
 MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
 RDRAIN 50 16 RDRAINMOD 15.8e-3
 RGATE 9 20 1.94
 RLDRAIN 2 5 10
 RLGATE 1 9 51
 RLSOURCE 3 7 31
 RSLC1 5 51 RSLCMOD 1e-6
 RSLC2 5 50 1e3
 RSOURCE 8 7 RSOURCEMOD 3.6e-3
 RVTHRES 22 8 RVTHRESMOD 1
 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
 S1B 13 12 13 8 S1BMOD
 S2A 6 15 14 13 S2AMOD
 S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1



ESLC 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*99),3.5))}

.MODEL DBODYMOD D (IS = 2.6e-12 RS = 2.65e-3 IKF = 6 TRS1 = 1.5e-3 TRS2 = 3.5e-6 CJO = 2.1e-9 TT = 5.6e-8 M = 0.52)
 .MODEL DBREAKMOD D (RS = 2.5e-1 TRS1 = 1e-4 TRS2 = -1e-6)
 .MODEL DPLCAPMOD D (CJO = 2.6e-9 IS = 1e-30 M = 0.89 N = 10)
 .MODEL MMEDMOD NMOS (VTO = 1.77 KP = 7 IS = 1e-30 N = 10 TOX = 1 L = 1U W = 1U RG = 1.94)
 .MODEL MSTROMOD NMOS (VTO = 2.06 KP = 95 IS = 1e-30 N = 10 TOX = 1 L = 1U W = 1U)
 .MODEL MWEAKMOD NMOS (VTO = 1.48 KP = 0.12 IS = 1e-30 N = 10 TOX = 1 L = 1U W = 1U RG = 19.4 RS = .1)
 .MODEL RBREAKMOD RES (TC1 = 1.05e-3 TC2 = -5e-7)
 .MODEL RDRAINMOD RES (TC1 = 8.5e-3 TC2 = 2.3e-5)
 .MODEL RSLCMOD RES (TC1 = 3.4e-3 TC2 = 2.5e-6)
 .MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6)
 .MODEL RVTHRESMOD RES (TC1 = -1.9e-3 TC2 = -4.5e-6)
 .MODEL RVTEMPMOD RES (TC1 = -1.7e-3 TC2 = 1.5e-6)
 .MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.5 VOFF = -2.0)
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.0 VOFF = -4.5)
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.5 VOFF = 0.3)
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.3 VOFF = -0.5)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

REV 26 July 1999

template huf76639 n2,n1,n3
electrical n2,n1,n3

```
{
var i iscl
d..model dbodymod = (is = 2.6e-12, cjo = 2.1e-9, tt = 5.6e-8, m = 0.52, n=10)
d..model dbreakmod = ()
d..model dplcapmod = (cjo = 2.6e-9, is = 1e-30, m = 0.89)
m..model mmedmod = (type=_n, vto = 1.77, kp = 7, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 2.06, kp = 95, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 1.48, kp = 0.12, is = 1e-30, tox = 1)
sw_vcsp..model s1amod = (ron = 1e-5, roff = 0.1, von = -4.5, voff = -2.0)
sw_vcsp..model s1bmod = (ron = 1e-5, roff = 0.1, von = -2.0, voff = -4.5)
sw_vcsp..model s2amod = (ron = 1e-5, roff = 0.1, von = -0.5, voff = 0.3)
sw_vcsp..model s2bmod = (ron = 1e-5, roff = 0.1, von = 0.3, voff = -0.5)
```

c.ca n12 n8 = 4.2e-9
c.cb n15 n14 = 4.2e-9
c.cin n6 n8 = 2.27e-9

d.dbody n7 n71 = model = dbodymod
d.dbreak n72 n11 = model = dbreakmod
d.dplcap n10 n5 = model = dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1.0e-9
l.lgate n1 n9 = 5.1e-9
l.lsource n3 n7 = 3.1e-9

m.mmed n16 n6 n8 n8 = model = mmedmod, l = 1u, w = 1u
m.mstrong n16 n6 n8 n8 = model = mstrongmod, l = 1u, w = 1u
m.mweak n16 n21 n8 n8 = model = mweakmod, l = 1u, w = 1u

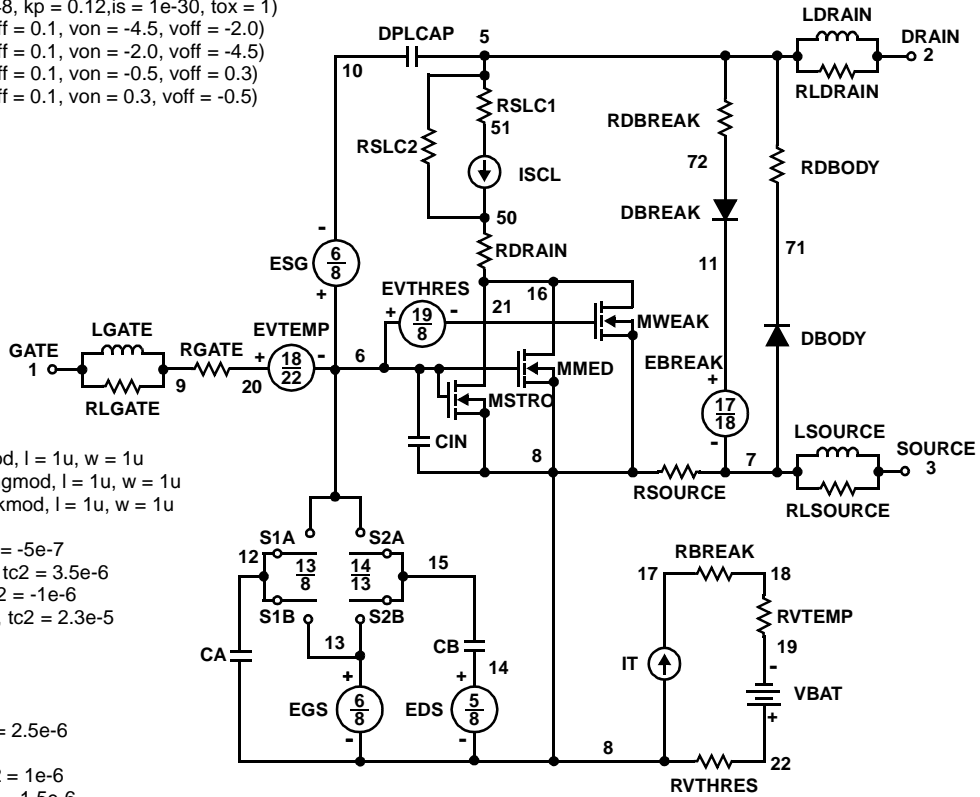
res.rbreak n17 n18 = 1, tc1 = 1.05e-3, tc2 = -5e-7
res.rbody n71 n5 = 2.65e-3, tc1 = 1.5e-3, tc2 = 3.5e-6
res.rdbreak n72 n5 = 2.5e-1, tc1 = 1e-4, tc2 = -1e-6
res.rdrain n50 n16 = 15.8e-3, tc1 = 8.5e-3, tc2 = 2.3e-5
res.rgate n9 n20 = 1.94
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 51
res.rlsource n3 n7 = 31
res.rslc1 n5 n51 = 1e-6, tc1 = 3.4e-3, tc2 = 2.5e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 3.6e-3, tc1 = 1e-3, tc2 = 1e-6
res.rvtemp n18 n19 = 1, tc1 = -1.7e-3, tc2 = 1.5e-6
res.rvthres n22 n8 = 1, tc1 = -1.9e-3, tc2 = -4.5e-6

spe.ebreak n11 n7 n17 n18 = 118.2
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model = s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model = s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model = s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model = s2bmod

v.vbat n22 n19 = dc = 1

```
equations {
i (n51->n50) + = iscl
iscl: v(n51,n50) = (((v(n5,n51))/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51))*1e6/99))** 3.5))
}
}
```



SPICE Thermal Model

REV 26 July 1999

HUF76639T

CTHERM1 th 6 3.2e-3
 CTHERM2 6 5 8.5e-3
 CTHERM3 5 4 1.2e-2
 CTHERM4 4 3 1.6e-2
 CTHERM5 3 2 5.5e-2
 CTHERM6 2 tl 1.5

RTHERM1 th 6 8.0e-3
 RTHERM2 6 5 6.8e-2
 RTHERM3 5 4 9.2e-2
 RTHERM4 4 3 2.0e-1
 RTHERM5 3 2 2.4e-1
 RTHERM6 2 tl 5.2e-2

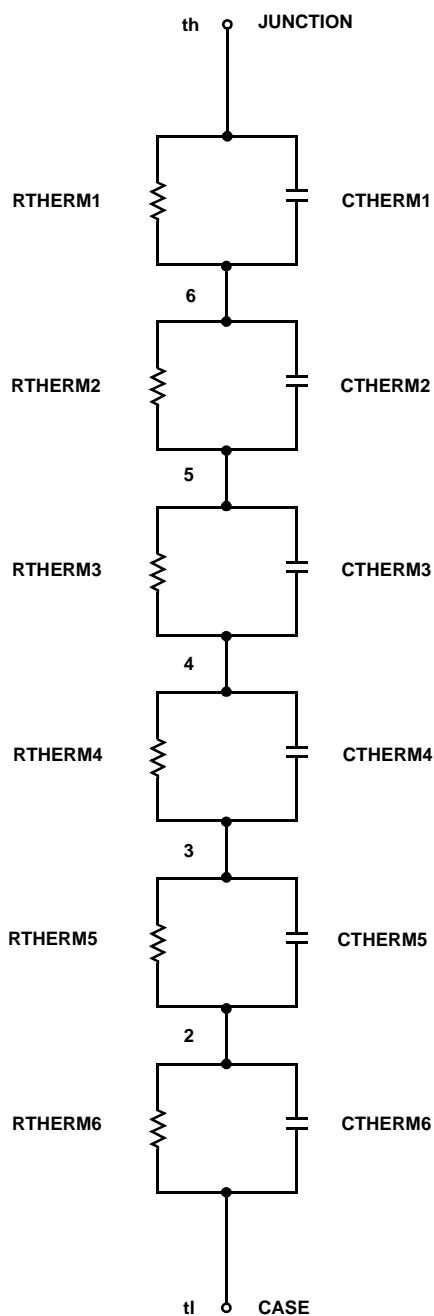
SABER Thermal Model

SABER thermal model HUF76639T

template thermal_model th tl
 thermal_c th, tl

```
{
ctherm.ctherm1 th 6 = 3.2e-3
ctherm.ctherm2 6 5 = 8.5e-3
ctherm.ctherm3 5 4 = 1.2e-2
ctherm.ctherm4 4 3 = 1.6e-2
ctherm.ctherm5 3 2 = 5.5e-2
ctherm.ctherm6 2 tl = 1.5
```

```
rtherm.rtherm1 th 6 = 8.0e-3
rtherm.rtherm2 6 5 = 6.8e-2
rtherm.rtherm3 5 4 = 9.2e-2
rtherm.rtherm4 4 3 = 2.0e-1
rtherm.rtherm5 3 2 = 2.4e-1
rtherm.rtherm6 2 tl = 5.2e-2
}
```



ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative