I2T100

Process Technology

I2T100: 0.7 μm Process Technology

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Overview

The Intelligent Interface Technology (I2T100) process from ON Semiconductor offers 100 V capability in a 0.7 μm CMOS mixed−signal technology. A variety of devices and process options provide a high degree of flexibility in combining mixed analog/digital with low−, medium− and high−voltage circuitry.

Features

- 2−3 Metal Layers
- Floating NMOS and PMOS Transistors
- Low Threshold PMOS Transistor
- Medium− and High−Voltage NDMOS Transistors
- Floating Medium− and High−Voltage NDMOS and PDMOS Transistors
- Low−, Medium− and High−Voltage Bipolar Transistors
- Zener Zap Diode for OTP
- Medium− and High−Resistivity Polysilicon Resistors
- Medium− and High−Voltage Floating Capacitors
- Deep N + Doped Guard Rings
- Optional EEPROM
- High Temperature Capability

PROCESS CHARACTERISTICS

Operating Voltage	5.0 V
Substrate Material	P−sub, Twin−Well
Drawn Transistor Length	0.7 μm
Gate Oxide Thickness	17.0 / 42.0 nm
Contact/Via Size	0.8 μm
Contacted Gate Pitch	2.8 μm
Top Metal Thickness	900 nm
Contacted Metal Pitch	
Metal 1 (Contact/Via)	2.8 / 2.6 μm
Metal 2 (Via 1/Via 2)	3.0 / 3.6 μm
Metal 3 (Via 2)	4.0 μm
Metal Composition	Al/Si/Cu
Isolation	LOCOS
ILD Planarization	BPSG
IMD Planarization	PECVD/SOG

SAMPLE PROCESS OPTIONS

	Mask Layers
2 Metal, NSINKER, HIPO, CAPA, LowVt pMOS	22
3 Metal, NSINKER, HIPO, CAPA, LowVt pMOS	24

DEVICE CHARACTERISTICS
(All Values Typical at 25°C)

LOW−VOLTAGE TRANSISTORS

NMOS Transistor	Typical Value	Units
Vt (20/0.7, linear extrapolated)	0.74	V
Vmax = Vbd	5.5	V
Ids (20/0.7, Vds = Vgs = 5 V)	358	μA/μm
PMOS Transistor	**Typical Value**	**Units**
Vt (20/0.7, linear extrapolated)	−0.95	V
Vmax = Vbd	5.5	V
Ids (20/0.7, Vds = Vgs = 5 V)	−176	μA/μm
Low Vt PMOS Transistor	**Typical Value**	**Units**
Vt (20/1.2, linear extrapolated)	−0.78	V
Vmax = Vbd	5.5	V
Ids (20/1.2, Vds = Vgs = 5 V)	−121	μA/μm

HIGH−VOLTAGE TRANSISTORS

Floating NMOS Transistor @ 100 V	Typical Value	Units
Vt (20/0.7, linear extrapolated)	0.74	V
Vmax = Vfloat to P−substrate	100	V
Vgsmax = Vbdmax	5.5	V
Ids (20/0.7, Vd = Vg = 5 V)	358	μA/μm
Floating PMOS Transistor @ 100 V	**Typical Value**	**Units**
Vt (25/0.7, linear extrapolated)	−1.1	V
Vmax = Vfloat to P−substrate	100	V
Vgsmax = Vbdmax	−5.5	V
Ids (25/0.7, Vd = Vg = 5 V)	−160	μA/μm
100 V NDMOS	**Typical Value**	**Units**
Vt (W = 40)	1	V
Vmax = Vbd	100	V
Vgsmax (full lifetime)	12	V
IDS (40/4, Vds = 40 V, Vgs = 4.0 V)	1210	μA
Ron*W	74	kΩ*μm
Ron*Area	1532	mΩ*mm^2
30 V NDMOS (Thin Ox)	**Typical Value**	**Units**
Vt (W = 40)	0.67	V
Vmax = Vbd	30	V
Vgsmax (full lifetime)	5.5	V
IDS (40/4, Vds = 20 V, Vgs = 5.0 V)	4675	μA
Ron*W	31.8	kΩ*μm
Ron*Area	372	mΩ*mm^2

30 V NDMOS (Thick Ox)	Typical Value	Units
Vt (W = 40)	1.03	V
Vmax = Vbd	30	V
Vgsmax (full lifetime)	12	V
IDS (40/4, Vds = 15 V, Vgs = 4.0 V)	1450	μA/μm
Ron*W	22	kΩ*μm
Ron*Area	257	mΩ*mm^2
100 V Self−Aligned Floating NDMOS	**Typical Value**	**Units**
Vt (W = 40)	2.43	V
Vmax = Vbd	95	V
Vgsmax (full lifetime)	12	V
IDS (40/1.2, Vds = 40 V, Vgs = 5.0 V)	2050	μA/μm
Ron*W	33	kΩ*μm
Ron*Area	488	mΩ*mm^2
60 V Self−Aligned Floating NDMOS	**Typical Value**	**Units**
Vt (W = 40)	2.4	V
Vmax = Vbd	60	V
Vgsmax (full lifetime)	12	V
IDS (40/1.2, Vds = 40 V, Vgs = 5.0 V)	2250	μA/μm
Ron*W	17.6	kΩ*μm
Ron*Area	153	mΩ*mm^2
40 V Self−Aligned Floating NDMOS	**Typical Value**	**Units**
Vt (W = 40)	2.43	V
Vmax = Vbd	40	V
Vgsmax (full lifetime)	12	V
IDS (40/1.2, Vds = 25 V, Vgs = 5.0 V)	2200	μA/μm
Ron*W	11.6	kΩ*μm
Ron*Area	87	mΩ*mm^2
90 V PDMOS	**Typical Value**	**Units**
Vt (W = 40)	−1.13	V
Vmax = Vbd	−100	V
|Vgsmax| (full lifetime)	12	V
IDS (40/4, Vds = 40 V, Vgs = 4.0 V)	980	μA/μm
Ron*W	77	kΩ*μm
Ron*Area	1050	mΩ*mm^2
75 V PDMOS	**Typical Value**	**Units**
Vt (W = 40)	−1.13	V
Vmax = Vbd	−75	V
|Vgsmax| (full lifetime)	12	V

IDS (40/3.4, Vds = 40 V, Vgs = 4.0 V)	1125	μA/μm
Ron*W	59	kΩ*μm
Ron*Area	596	mΩ*mm^2
40 V PDMOS	**Typical Value**	**Units**
Vt (W = 40)	−1.13	V
Vmax = Vbd	−40	V
|Vgsmax| (full lifetime)	12	V
IDS (40/3.2, Vds = 25 V, Vgs = 4.0 V)	1175	μA/μm
Ron*W	45	kΩ*μm
Ron*Area	380	mΩ*mm^2
100 V Depleted PDMOS	**Typical Value**	**Units**
Vmax = Vbd	−100	V
|Vgsmax| (full lifetime)	5.5	V
IDS (40/3, Vds = 40 V, Vgs = 0 V)	180	μA/μm
60 V Power−Kit NDMOS (optimized for switching applications)	**Typical Value**	**Units**
Vt (W = 40)	2.45	V
Vmax = Vbd	60	V
Vgsmax (full lifetime)	12	V
IDS (40/1.2, Vds = 25 V, Vgs = 5.0 V)	2200	μA/μm
Ron*W	18	kΩ*μm
Ron*Area	115	mΩ*mm^2
40 V Power−Kit NDMOS (optimized for switching applications)	**Typical Value**	**Units**
Vt (W = 40)	2.45	V
Vmax = Vbd	40	V
Vgsmax (full lifetime)	12	V
IDS (40/1.2, Vds = 25 V, Vgs = 5.0 V)	2350	μA/μm
Ron*W	11.3	kΩ*μm
Ron*Area	65	mΩ*mm^2

BIPOLAR TRANSISTORS

NPN Floating @ 100 V Ae = 5 μm^2, Area = 3529 μm^2	**Typical Value**	**Units**
Hfe	60	−
Bvceo @ Ie = 1 μA	25	V
Bvces min	60	V
Imax @ 142°C	0.3	mA
NPN Floating @ 100 V Ae = 49 μm^2, Area = 4490 μm^2	**Typical Value**	**Units**
Hfe	40	−
Bvceo @ Ie = 1 μA	25	V
Bvces min	60	V
Imax @ 142°C	2.7	mA
NPN Floating @ 60 V Ae = 5 μm^2, Area = 1352 μm^2	**Typical Value**	**Units**
Hfe	58	−
Bvceo @ Ie = 1 μA	25	V
Bvces min	60	V
Imax @ 142°C	0.96	mA
NPN Floating @ 60 V Ae = 19 μm^2, Area = 3081 μm^2	**Typical Value**	**Units**
Hfe	45	−
Bvceo @ Ie = 1 μA	25	V
Bvces min	25	V
Imax	1.2	mA
Substrate PNP Ae = 460 μm^2, Area = 2289 μm^2, Collector Grounded	**Typical Value**	**Units**
Hfe	22	−
Bvceo @ Ie = 1 μA	30	V
Vbe	0.57	V
PNP Floating @ 100 V Area = 1542 μm^2	**Typical Value**	**Units**
Hfe	700	−
Bvceo @ Ie = 1 μA	5.5	V
Bvces min	5.5	V
Imax @ 142°C	0.3	mA
PNP Area = 5139 μm^2	**Typical Value**	**Units**
Hfe	800	−
Bvceo @ Ie = 1 μA	25	V
Bvces min	40	V
Imax @ 142°C	0.3	mA
PNP Area = 98354 μm^2	**Typical Value**	**Units**
Hfe	880	−
Bvceo @ Ie = 1 μA	25	V
Bvces min	80	V
Imax @ 142°C	0.3	mA

DIODES

Poly Diode Parameter, W = 2.2 μm	**Typical Value**	**Units**
BV	6.76	V
Imax (2.2 μm)	~300	μA
Ileak (2.2 μm) @ −5 V	~90	μA

90 V Floating HV Diode Area = 6432 μm²	Typical Value	Units
BV	90	V
Isub/Ia (Ia = 2.4 mA)	~2	%
Zener Diode Smallest Diode (3784 μm²)	**Typical Value**	**Units**
BV	9.5	V
Ron in Vbd mode	1560	Ω

CAPACITORS (PARAMETER @ 25°C)

Poly/ Thin Gate Ox/ N++ [CAPA]	Typical Value	Units
Cplate	0.75	fF/μm²
Vbd_max (full lifetime)	15	V
Poly/ Poly (Medium Voltage Floating)	**Typical Value**	**Units**
Cplate	0.36	fF/μm²
Vbd_max (full lifetime)	30	V
Metal1/ Poly/ Metal2 (High Voltage Floating)	**Typical Value**	**Units**
Cplate	0.075	fF/μm²
Vbd_max (full lifetime)	100	V

RESISTORS

Resistor Type	Typical Value	Units
High−Resistance Poly [HIPO]	1825	Ω/square
Medium−Resistance Poly [MOPO]	190	Ω/square
Low−Resistance Poly [LOPO]	27	Ω/square
N−Well	1000	Ω/square
Pbody Diffusion in Ntub	1250	Ω/square
N+ Diffusion in P−well	67.5	Ω/square
P+ Diffusion in N−well	96	Ω/square

LIBRARIES

Digital Design	
Standard Cell Core Library	pn sum: 5.7 μm
	Area of 2−input nand (na21): 207 μm²
	Gate density (na21 @ 100% utilization): 4.831 k gates/mm²
	Scan Flop density (scan flops @ 100% utilization): 0.5574 k ff/mm²
	Average power (@ 5.0 V): 2.32 μW/MHz/gate

CAD TOOL COMPATIBILITY

Digital Design	Synopsys Design Compiler
	Cadence Verilog
Analog Design	Cadence DFII (4.4.6)
	Spectre
Place and Route	Synopsys Apollo
	Cadence Silicon Ensemble
Physical Verification	Mentor Calibre

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