I3T25

Process Technology

I3T25: 0.35 μm Process Technology

ON Semiconductor®

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Overview

Providing the density of a 0.35 μm digital process, analog/mixed−signal capability and high voltage, the Intelligent Interface Technology I3T25 process from ON Semiconductor is the answer to the need for increased digital content in a mixed−signal and/or high voltage environment. Featuring high voltage devices up to 18 V as well as digital and analog operation at 3.3 V and 12 V, the I3T25 process family features a wide range of capabilities in a single IC.

Features

- 3 to 5 Metal Layers
- Metal to Metal (MIM) Linear Capacitors
- Poly to Poly Capacitors
- High and Medium Resistivity Polysilicon Resistors
- Floating HV Thick/Thin ox NDMOS and PDMOS Transistors
- Floating Low−voltage Diodes
- Schottky Diode
- Medium−voltage PNP and NPN Bipolar Transistors
- Zener Zap Diode OTP
- Buried Zener Diode for Clamping
- Medium−voltage Floating Metal Capacitors
- Deep N + Doped Guard Rings

PROCESS CHARACTERISTICS

Operating Voltage	3.3, 12 V
Substrate Material	N−epitaxy on P−sub, Retrograde Wells
Drawn Transistor Length	0.35 μm
Gate Oxide Thickness	7/~30 nm
Contact/Via Size	0.4 μm
Contacted Gate Pitch	1.3 μm
Top Metal Thickness	845 nm
Metal Pitch	
Metal 1	1.0 μm
Metal 2	1.1 μm
Top Metal	1.4 μm
Metal Composition	Al/Cu
Isolation	LOCOS
ILD Planarization	PSG/PETEOS/ +CMP
IMD Planarization	PETEOS+CMP

SAMPLE PROCESS OPTIONS

	Mask Layers
3 Metal, 25 V HIPO, OTP	19
4 Metal, 25 V HIPO, OTP	21
5 Metal, 25 V HIPO, OTP	23
Thick Oxide	+3
Poly Poly Cap	+1
MIMC	+1

DEVICE CHARACTERISTICS

All Values Typical at 25°C

LOW−VOLTAGE TRANSISTORS

NMOS Transistor	Typical Value	Units
Vt (10/0.35, linear extrapolated)	0.59	V
Vmax = Vbd	3.6	V
IDS (10/0.35, Vds = Vgs = 3.3 V)	530	μA/μm
PMOS Transistor	**Typical Value**	**Units**
Vt (10/0.35, linear extrapolated)	−0.57	V
Vmax = Vbd	−3.6	V
IDS (10/0.35, Vds = Vgs = 3.3 V)	−250	μA/μm

THICK OXIDE HIGH−VOLTAGE TRANSISTORS (EXTENDED DRAIN)

Floating NDMOS (18 V)	Typical Value	Units
Vt (Vd = 0.1 V)	1.3	V
Vbd (Vgs = 0)	31	V
Vgsmax	12	V
Vdsmax, SOA* (Vgs = Vgsmax, full lifetime)	12	V
Vdsmax, (Vgs full lifetime)	18	V
Ron*Area (Vg = 18 V, Vd = 0.5 V)	27	mΩ*mm^2
Ids	260	μA/μm
Floating PDMOS (18 V)	**Typical Value**	**Units**
Vt (Vd = 0.1 V)	−1.3	V
Vbd (Vgs = 0)	−35	V
Vgsmax	−12	V
Vdsmax, SOA* (Vgs = Vgsmax, full lifetime)	−12	V
Vdsmax, (Vgs full lifetime)	−18	V
Ron*Area (Vg = 18 V, Vd = 0.5 V)	71	mΩ*mm^2
Ids	−110	μA/μm

* Symmetric Device Available

THIN OXIDE HIGH−VOLTAGE TRANSISTORS (EXTENDED DRAIN)

Floating NDMOS	Typical Value	Units
Vt (Vd = 0.1 V)	0.6	V
Vbd (Vgs = 0)	31	V
Vgsmax	3.6	V
Vdsmax, SOA* (Vgs = Vgsmax, full lifetime)	12	V
Vdsmax, (Vgs full lifetime)	18	V
Ron*Area (Vg = 3.3 V, Vd = 0.5 V)	35	mΩ*mm^2
Ids	280	μA/μm
Floating PDMOS	**Typical Value**	**Units**
Vt (Vd = 0.1 V)	−0.6	V
Vbd (Vgs = 0)	−28	V
Vgsmax	−3.6	V
Vdsmax, SOA* (Vgs = Vgsmax, full lifetime)	−12	V
Vdsmax, (Vgs full lifetime)	−18	V
Ron*Area (Vg = 3.3 V, Vd = 0.5 V)	75	mΩ*mm^2
Ids	−121.5	μA/μm

* Symmetric Device Available

THICK OXIDE HIGH−VOLTAGE TRANSISTORS (NESTED DRAIN)

Floating NDMOS (12 V)	Typical Value	Units
Vt (Vd = 0.1 V)	1.3	V
Vbd (Vgs = 0)	21	V
Vgsmax	12	V
Vdsmax, SOA* (Vgs = Vgsmax, full lifetime)	8	V
Vdsmax, (Vgs full lifetime)	12	V
Ron*Area (Vg = 18 V, Vd = 0.5 V)	15	mΩ*mm^2
Ids	260	μA/μm
Floating PDMOS (12 V)	**Typical Value**	**Units**
Vt (Vd = 0.1 V)	−1.4	V
Vbd (Vgs = 0)	−21	V
Vgsmax	−12	V
Vdsmax, SOA* (Vgs = Vgsmax, full lifetime)	−8	V
Vdsmax, (Vgs full lifetime)	−12	V
Ron*Area (Vg = 18 V, Vd = 0.5 V)	75	mΩ*mm^2
Ids	−92	μA/μm

* Symmetric Device Available

BIPOLAR TRANSISTORS

Bipolar Transistors Vertical Low−Voltage NPN (Parameter, E_area = 3.61 μm^2)	Typical Value	Units
Hfe @ Ic = 10 μA	17.3	−
Bvceo @ Ic = 1 μA	20.5	V
Bvces @ Ic = 1 μA	20.9	V
Vertical Low−Voltage PNP Transistor (Parameter, E_area = 0.64 μm^2)	**Typical Value**	**Units**
Hfe @ Ic = 10 μA	20.1	−
Bvceo @ Ic = 1 μA	−14.5	V
Bvces @ Ic = 1 μA	−19.5	V

DIODES

Zener Diode: PBZD (a = 2 μm)	Typical Value	Units
Vz @ 100 μA	4.6	V
Rzener	45	Ω
Ileak @ Vz = 0.5 V	200	nA

Zapping Zener Diode for OTP: UZZD	Typical Value	Units
Vz @ 1 μA	1.5	V
Vbd @ 10 mA	4.5	V
Ileak @ Vz = 1 V	1.4	V
Poly Diode for Gate Clamping: POLYD	**Typical Value**	**Units**
Vreverse @ Ia = 10 μA	6.8	V
Schottky		
Vbd @ 1 μA	15	V
ILeak @ 5.5	< 20	nA

CAPACITORS (PARAMETER @ 25°C)

Type (Maximum Voltage)	Typical Value	Units
Metal2 / Metal2.5 Plate: MIMC (3.6 V)	1.5	$fF/\mu m^2$
Poly Poly Capacitor (13.2 V)	1	$fF/\mu m^2$

RESISTORS (PARAMETER @ 25°C)

Resistor Type	Typical Value	Units
High−Resistance Poly: HIPO	975	Ω/square
Salicided P+ Poly: LOPOR	2.4	Ω/square
Unsalicided P+ Poly: PPOLR	240	Ω/square
Unsalicided P+ in Mwell	64	Ω/square
Unsalicided N+ Poly: NPOLR	292	Ω/square
Unsalicided P+ in Pwell	47.5	Ω/square
Nwell under FOX (field oxide)	958	Ω/square
Nwell in AA (active area)	800	Ω/square
Pwell in AA (active area)	1755	Ω/square

LIBRARIES

All Values Typical at 25°C

Standard Cell	
Ultra High Density Core Shell	pn sum: 2.0
	Area of 2−input nand (na21): 38.88 μm^2
	Gate density (na21 @ 100% utilization): 25.72 k gates/mm^2
	Scan Flop densoty (scan flops @ 100% utilization): 3.215 k ff/mm^2
	Average power (@ 3.3 V): 0.2929 μW/MHz/gate
Core Cell Level Shifters	Unidirectional: 1 cell optimized for speed, pad high to core low
Standard I/O	
Fat Pad I/O Library (for core limited designs)	172.80 μm min in−line pad pitch
	180.00 μm pad height
Tall Pad I/O Library (for pad limited designs)	86 μm min in−line pad pitch
	322.50 μm pad height

MEMORY OPTIONS

RAM	
Synchronous High Speed / High Temp Single Port SRAM	Minimum: 16 words x 2 bits
	Maximum: 128 k bits (i.e: 16 k words x 8 bits, 8 k words x 16 bits, …)
Synchronous High Speed / High Temp Dual Port SRAM	Minimum: 16 words x 2 bits
	Maximum: 128 k bits (i.e: 16 k words x 8 bits, 8 k words x 16 bits, …)
Low Power Synchronous SRAM	Minimum: 64 words x 4 bits
	Maximum: 128 k bits (i.e: 16 k words x 8 bits, 8 k words x 16 bits, …)
ROM	
Synchronous High Speed / High Temp Diffusion ROM	Minimum: 256 words x 4 bits
	Maximum: 512 k bits (i.e: 64 k words x 8 bits, 32 k words x 16 bits, …)
Low Power Synchronous Via Programmable ROM	Minimum: 256 words x 4 bits
	Maximum: 512 k bits (i.e: 64 k words x 8 bits, 32 k words x 16 bits, …)
Non−Volatile Memory	
OTP − One Time Programmable	Fuse: Zener Diode optimized for low power zapping
	Both Serial and Parallel Output Capability
	In field programming available
	Vector: Up to 320 bits
EEPROM − No Additional Masks or Processing Steps	Differential Bit Cell (Redundancy for High Reliability)
	2 ms Write/Erase
	Array: up to 8 k bits (128 x 64), Vector: 8 to 64 bits (1 x 8 to 1 x 64)
	Internal Charge Pump provided
	Memory Failure Rate: < 10 ppm, < 1 ppm with ECC (128 x 56)
	Automotive qualification AEC−Q100

CAD TOOL COMPATIBILITY

Digital Design	Synopsys Design Compiler
	Cadence Verilog
Analog Design	Cadence DFII (4.4.6)
	Cadence Spectre
Place and Route	Synopsys Apollo
	Cadence Silicon Ensemble
Physical Verification	Mentor graphics Calibre

PUBLICATION ORDERING INFORMATION

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