I3T50

Process Technology

I3T50: 0.35 μm Process Technology

ON Semiconductor®

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Overview

Providing the density of a 0.35 μm digital process, analog/mixed−signal capability and high voltage, the ON Semiconductor Intelligent Interface Technology I3T50 process is the answer to the need for increased digital content in a mixed−signal and/or high voltage environment. Featuring high voltage devices up to 40 V as well as digital and analog operation at 3.3 V, the I3T50 process family is the first to use deep trenches for isolating high voltage devices.

Features

- 3 to 5 Metal Layers
- Metal to Metal (MIM) Linear Capacitors
- High−Voltage Metal Capacitors
- High−Resistivity Polysilicon Resistors
- Two Types of Medium−Resistivity Polysilicon Resistors
- Floating High−Voltage NDMOS & PDMOS Transistors
- Floating Medium−Voltage NDMOS Transistors
- Zener Zap Diode for OTP
- Floating High−Voltage and Low−Voltage Diodes
- Polysilicon Gate Protection Diodes
- Medium−voltage NPN Bipolar Transistors
- Deep Trench Isolation
- EEPROM Capability
- High Temperature Capability

PROCESS CHARACTERISTICS

Operating Voltage	3.3 V
Substrate Material	N−epitaxy on P−sub, Retrograde Wells
Drawn Transistor Length	0.35 μm
Gate Oxide Thickness	7.0 nm
Contact/Via Size	0.4 μm
Contacted Gate Pitch	1.3 μm
Top Metal Thickness	1020 nm
Metal Pitch	
Metal 1	1.0 μm
Metal 2	1.1 μm
Top Metal	1.4 μm
Metal Composition	Al/Cu
Isolation	LOCOS for CMOS, DT for HV
ILD Planarization	USG/BPTEOS+CMP
IMD Planarization	HDP/PETEOS+CMP

SAMPLE PROCESS OPTIONS

	Mask Layers
3 Metal, 40 V, MIMC, HIPO, OTP	21
4 Metal, 40 V, MIMC, HIPO, OTP	23
5 Metal, 40 V, MIMC, HIPO, OTP	25

DEVICE CHARACTERISTICS

All Values Typical at 25°C

LOW−VOLTAGE TRANSISTORS

NMOS Transistor	Typical Value	Units
Vt (10/0.35, linear extrapolated)	0.59	V
Vmax = Vbd	3.6	V
IDS (10/0.35, Vds = Vgs = 3.3 V)	530	μA/μm
PMOS Transistor	**Typical Value**	**Units**
Vt (10/0.35, linear extrapolated)	−0.57	V
Vmax = Vbd	−3.6	V
IDS (10/0.35, Vds = Vgs = 3.3 V)	−250	μA/μm

HIGH−VOLTAGE TRANSISTORS

Floating NMOS Transistor: VFNDM50	Typical Value	Units
Vt (W = 40 μm)	0.77	V
Vdsmax (guaranteed by hot carrier measurements)	40	V
Vgsmax (full lifetime)	3.6	V
Ids (Vds = 25 V, Vgs = 3.3 V, 4 channels)	220	μA/μm
Ron*Area (20 channels)	52	mΩ*mm^2
Floating PDMOS Transistor: LFPDM50	**Typical Value**	**Units**
Vt (W = 40 μm)	−0.57	V
Vdsmax (guaranteed by hot carrier measurements)	−40	V
Vgsmax (full lifetime)	−3.6	V
Ids (Vds = 10 V, Vgs = 3.3 V)	−110	μA/μm
Ron*Area	150	mΩ*mm^2
Floating Medium Voltage Transistor: LFNDM14	**Typical Value**	**Units**
Vt (W = 40 μm)	0.59	V
Vdsmax (guaranteed by hot carrier measurements)	14	V
Vgsmax (full lifetime)	3.6	V
Ids (Vds = 10 V, Vgs = 3.3 V)	300	μA/μm
Ron*Area	31	mΩ*mm^2

BIPOLAR TRANSISTORS (PARAMETER E_area = 0.16 μm^2)

Medium Voltage NPN	Typical Value	Units
Hfe @ Ic = 50 nA − 0.5 mA (emitter area 0.16 μm^2)	> 100	−
Hfe @ Ic = 10 nA − 1.0 mA (emitter area 0.49 μm^2)	> 80	−
Vce max @ Ic = 1 μA	11	V
Vce max @ Ic = 0 μA	40	V

DIODES (PARAMETER K_area = 6.76 μm^2)

Floating High Voltage Diode: FID50	Typical Value	Units
Vbd	51	V
Vak_forw, Ik = 1 μA	0.68	V
Poly Diode for Gate Clamping: POLYD	**Typical Value**	**Units**
Vbd	6.8	V
Vbe_forw	0.6	V
Ileak/W @ Vrev = 5 V	40	nA/μm
Vbd_max	7.5	V

DIODES (PARAMETER W = 2 μm)

Zapping Zener Diode for OTP: Z224	Typical Value	Units
Vz @ 50 μA	2.7	V
Vbd @ 10 mA	4.5	V
Ileak_max @ 1 V	1.7	μA

CAPACITORS (PARAMETER @ 25°C)

Metal2 / Metal2.5 Capacitor: MIMC	Typical Value	Units
C	1.5	fF/μm^2
V max	3.6	V
Metal1 / Metal3 Plate Capacitor	**Typical Value**	**Units**
C	0.1	fF/μm^2
V max	50	V
Poly / Metal3 Plate Capacitor	**Typical Value**	**Units**
C	0.14	fF/μm^2
V max	50	V
Metal1 / Metal3 Bar Capacitor	**Typical Value**	**Units**
C	0.26	fF/μm^2
V max	50	V
Poly / Metal3 Bar Capacitor	**Typical Value**	**Units**
C	0.33	fF/μm^2
V max	50	V

RESISTORS (PARAMETER @ 25°C)

Resistor Type	Typical Value	Units
High−Resistance Poly: HIPO	1000	Ω/square
Unsalicided P+ Poly: PPOLR	240	Ω/square
Unsalicided N+ Poly: NPOLR	270	Ω/square

LIBRARIES

Standard Cell	
Ultra High Density Core Shell	pn sum: 2.0
	Area of 2−input nand (na21): 38.88 μm^2
	Gate density (na21 @ 100% utilization): 25.72 k gates/mm^2
	Scan Flop density (scan flops @ 100% utilization): 3.215 k ff/mm^2
	Average power (@ 3.3 V): 0.2929 μW/MHz/gate
Standard I/O	
5 V Capable Fat Pad I/O Library (for core limited designs)	191.40 μm min in−line pad pitch
	214.60 μm pad height
5 V Capable Tall Pad I/O Library (for pad limited designs)	150.80 μm min in−line pad pitch
	417.60 μm pad height
Fat Pad I/O Library (for core limited designs)	174.00 μm min in−line pad pitch
	168.20 μm pad height
Tall Pad I/O Library (for pad limited designs)	92.80 μm min in−line pad pitch
	330.60 μm pad height

MEMORY OPTIONS

RAM	
Synchronous High Speed / High Temp Single Port SRAM	Minimum: 16 words x 2 bits
	Maximum: 128 k bits (i.e: 16 k words x 8 bits, 8 k words x 16 bits, …)
Synchronous High Speed / High Temp Dual Port SRAM	Minimum: 16 words x 2 bits
	Maximum: 128 k bits (i.e: 16 k words x 8 bits, 8 k words x 16 bits, …)
Low Power Synchronous SRAM	Minimum: 64 words x 4 bits
	Maximum: 128 k bits (i.e: 16 k words x 8 bits, 8 k words x 16 bits, …)

ROM	
Synchronous High Speed / High Temp Diffusion ROM	Minimum: 256 words x 4 bits
	Maximum: 512 k bits (i.e: 64 k words x 8 bits, 32 k words x 16 bits, …)
Low Power Synchronous Via Programmable ROM	Minimum: 256 words x 4 bits
	Maximum: 512 k bits (i.e: 64 k words x 8 bits, 32 k words x 16 bits, …)
Non−Volatile Memory	
OTP − One Time Programmable	Fuse: Zener Diode optimized for low power zapping
	Both Serial and Parallel Output Capability
	In field programming available
	Vector: Up to 320 bits
EEPROM − No Additional Masks or Processing Steps	Differential Bit Cell (Redundancy for High Reliability)
	2 ms Write/Erase
	Array: up to 8 k bits (128 x 64), Vector: 8 to 64 bits (1 x 8 to 1 x 64)
	Internal Charge Pump provided
	Memory Failure Rate: < 10 ppm, < 1 ppm with ECC (128 x 56)
	Automotive qualification AEC−Q100

CAD TOOL COMPATIBILITY

Digital Design	Synopsys Design Compiler
	Cadence Verilog
Analog Design	Cadence DFII (4.4.6)
	Spectre
Place and Route	Synopsys Apollo
	Cadence Silicon Ensemble
Physical Verification	Mentor Graphics Calibre

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