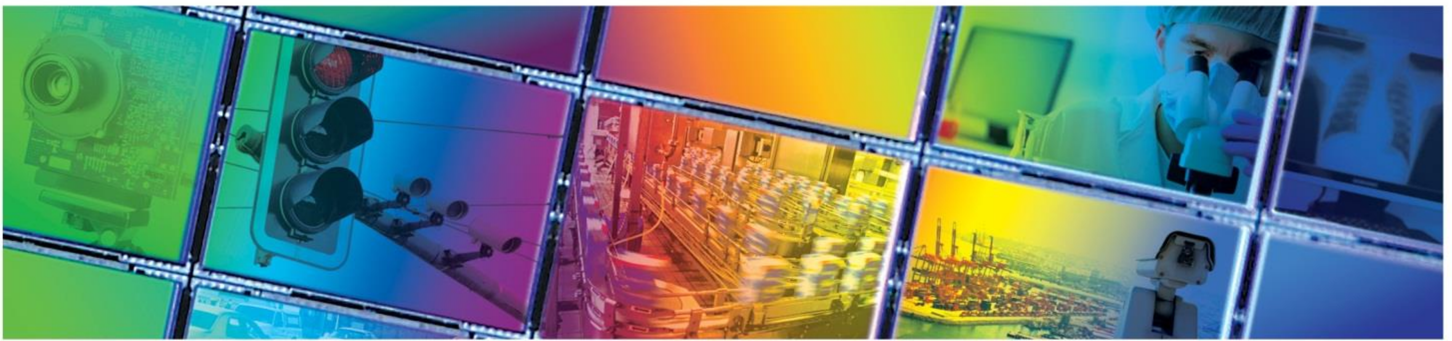
ON Semiconductor®

KAF-31600 IMAGE SENSOR

6496 (H) X 4872 (V) FULL FRAME CCD IMAGE SENSOR



JUNE 24, 2014

DEVICE PERFORMANCE SPECIFICATION

REVISION 1.1 PS-0042

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Summary Specification

KAF-31600 Image Sensor

DESCRIPTION

The KAF-31600 is a dual output, high performance color array CCD (charge coupled device) image sensor with 6496 (H) x 4872 (V) 6.8 µm square pixels, designed for digital still camera applications. Each pixel contains anti-blooming protection to prevent image corruption during high light level conditions. Each of the pixels are selectively covered with red, green or blue pigmented filters for color separation, and microlenses are added for improved sensitivity. The photoactive pixels are surrounded by a border of buffer and light-shielded pixels.

The sensor utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.

KEY FEATURES

- TRUESENSE Transparent Gate Electrode for high sensitivity
- Ultra-high resolution
- Broad dynamic range
- Low noise architecture
- Large active imaging area

APPLICATIONS

- Photography

Parameter	Typical Value
Architecture	Full Frame CCD; with Square Pixels
Total Number of Pixels	6606 (H) x 4954 (V) = 32.8M
Number of Effective Pixels	6536 (H) x 4912 (V) = 32.1M
Number of Active Pixels	6496 (H) x 4872 (V) = 31.6M
Pixel Size	6.8 µm (H) x 6.8 µm (V)
Imager Size	55.2 mm (diagonal)
Chip Size	46.05 mm (H) x 35.0 mm (V)
Aspect Ratio	4:3
Saturation Signal	60 ke$^-$
Charge to Voltage Conversion	24 µV/e$^-$
Quantum Efficiency (RGB)	37%, 43%, 36%
Read Noise (f = 24 MHz)	16 e$^-$
Dark Signal (T = 40 °C)	2 mV
Dark Current Doubling Temperature	6.3 °C
Linear Dynamic Range (f = 24 MHz, T = 40 °C)	70.5 dB
Charge Transfer Efficiency (HCTE/VCTE)	0.999995 0.999999
Blooming Protection (4 ms exposure time)	1000X saturation exposure
Maximum Data Rate	24 MHz
Readout Mode	Dual output only

Parameters above are specified at T = 20 °C unless otherwise noted.

Ordering Information

Catalog Number	Product Name	Description	Marking Code
4H0700	KAF-31600-CXA-DD-AA	Color (Bayer RGB), Special Microlens, CERDIP Package (sidebrazed, CuW), Clear Cover Glass with AR coating (both sides), Standard Grade	KAF-31600-CX S/N
4H0701	KAF-31600-CXA-DD-AE	Color (Bayer RGB), Special Microlens, CERDIP Package (sidebrazed, CuW), Clear Cover Glass with AR coating (both sides), Engineering Sample	
4H0814	KEK-4H0814-KAF-31600-12-24	Evaluation Board (Complete Kit)	N/A

See Application Note *Product Naming Convention* for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

Please address all inquiries and purchase orders to:

Truesense Imaging, Inc.
1964 Lake Avenue
Rochester, New York 14615

Phone: (585) 784-5500
E-mail: info@truesenseimaging.com

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Device Description

ARCHITECTURE

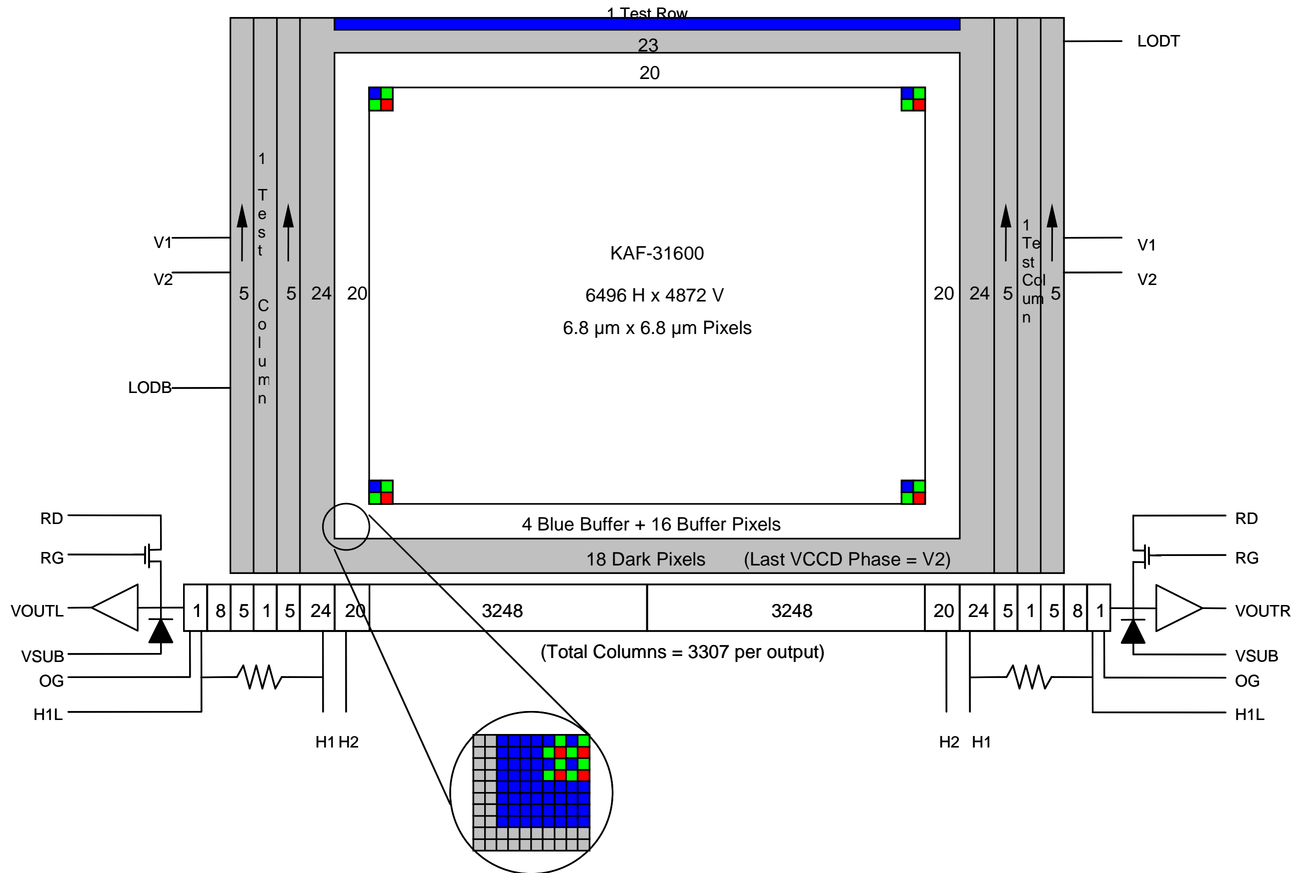


Figure 1: Block Diagram

Dark Reference Pixels

Surrounding the periphery of the device is a border of light shielded pixels creating a dark region. Within this dark region, exist light shielded pixels that include 24 leading dark pixels on every line. There are also 18 full dark lines at the start and 23 full dark lines at the end of every frame. Under normal circumstances, these pixels do not respond to light and may be used as a dark reference.

Dummy Pixels

Within each horizontal shift register there are 20 leading pixels. These are designated as dummy pixels and should not be used to determine a dark reference level.

Active Buffer Pixels

20 unshielded pixels adjacent to any leading or trailing dark reference regions are classified as active buffer pixels. These pixels are light sensitive but they are not tested for defects and non-uniformities. Of these 20 pixels, the outermost 4 pixels are covered with blue pigment while the remaining are arranged in a Bayer pattern (R, GR, GB, B)

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the device. These photon-induced electrons are collected locally by the formation of potential wells at each pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain to prevent crosstalk or 'blooming'. During the integration period, the V1 and V2 register clocks are held at a constant (low) level.

Charge Transport

The integrated charge from each pixel is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCDs to a horizontal CCD register using the V1 and V2 register clocks. The horizontal CCD is presented a new line on the falling edge of V2 while H1 is held high. The horizontal CCDs then transport each line, pixel by pixel, to the output structure by alternately clocking the H1 and H2 pins in a complementary fashion. A separate connection to the last H1 phase (H1L) is provided to improve the transfer speed of charge to the output amplifier. On each falling edge of H1L a new charge packet sensed by the output amplifier.

Horizontal Register

Output Structure

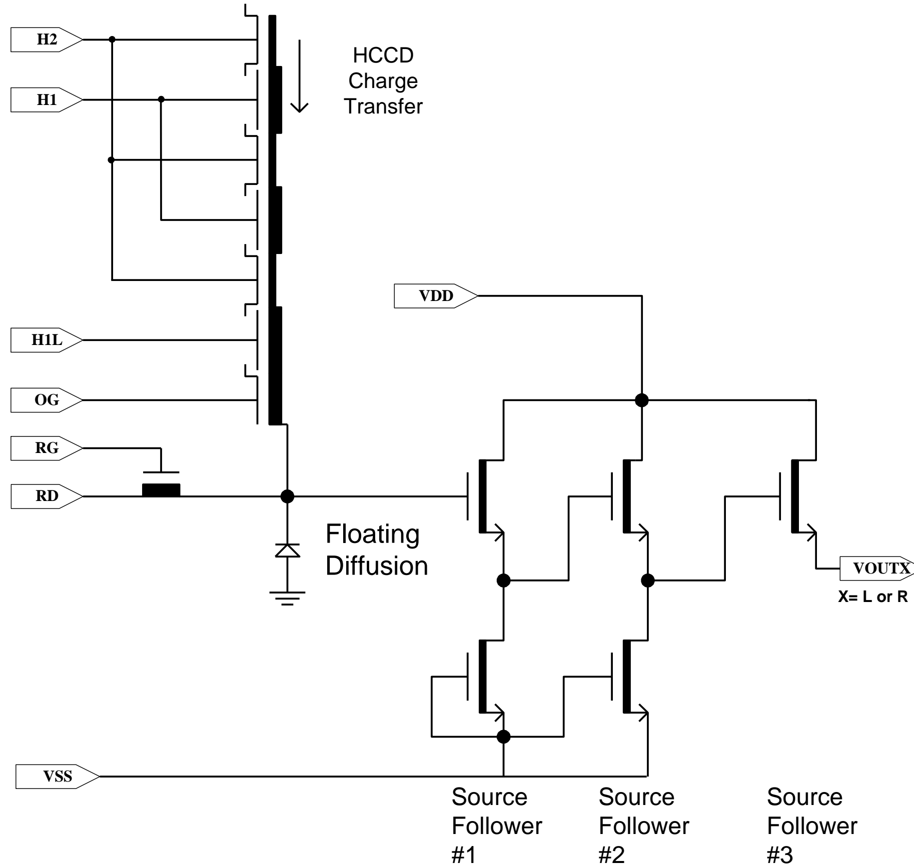


Figure 2: Output Architecture (Left or Right)

The output consists of a floating diffusion capacitance connected to a three-stage source follower. Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (RG) is clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structure, an off-chip current source must be added to the VOUT pin of the device.

Output Load

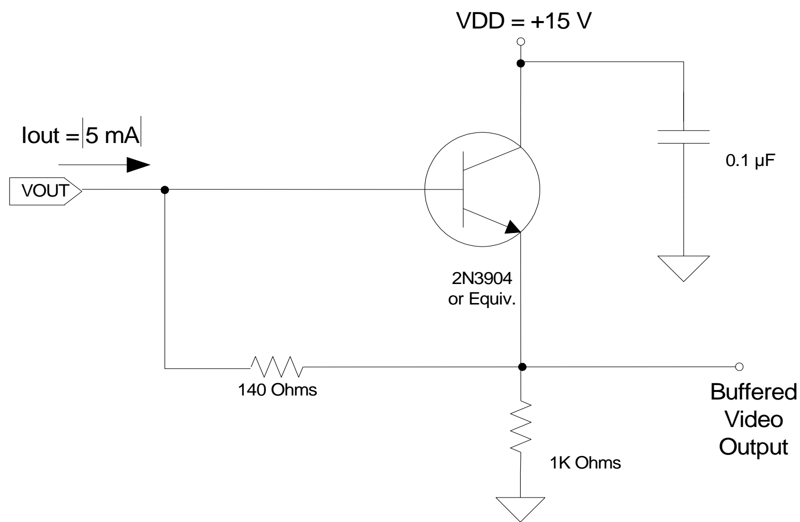


Figure 3: Recommended Output Structure Load Diagram

Notes:

1. Component values may be revised based on operating conditions and other design considerations.

Physical Description

Pin Description and Device Orientation

60 V1
59 V1
58 V2
57 V2
56 VSUB
55 VLOD
54 N/C
53 N/C
52 N/C
51 N/C
50 N/C
49 N/C
48 N/C
47 N/C
46 N/C
45 N/C
44 N/C
43 N/C
42 N/C
41 N/C
40 N/C
39 N/C
38 N/C
37 N/C
36 VLOD
35 VSUB
34 V2
33 V2
32 V1
31 V1

1 VSUB
2 VLOD
3 VDD
4 VOUTL
5 VSS
6 VRD
7 VRD
8 RG
9 VOG
10 H1L
11 H2
12 H2
13 H1
14 H1
15 VSUB
16 VSUB
17 H1
18 H1
19 H2
20 H2
21 H1L
22 VOG
23 RG
24 VRD
25 VRD
26 VSS
27 VOUTR
28 VDD
29 VLOD
30 VSUB

Notes:
1. Pins with the same name are to be tied together on the circuit board and have the same timing.

Pin	Name	Description
1	SUB	Substrate
2	LOD	Lateral Overflow Drain Bottom
3	VDD	Output Amplifier Supply
4	VOUTL	Video Output: Left
5	VSS	Output Amplifier Return
6	RD	Reset Drain
7	RD	Reset Drain
8	RG	Reset Gate
9	OG	Output Gate
10	H1L	Horizontal Phase 1, Last Gate
11	H2	Horizontal Phase 2
12	H2	Horizontal Phase 2
13	H1	Horizontal Phase 1
14	H1	Horizontal Phase 1
15	SUB	Substrate
16	SUB	Substrate
17	H1	Horizontal Phase 1
18	H1	Horizontal Phase 1
19	H2	Horizontal Phase 2
20	H2	Horizontal Phase 2
21	H1L	Horizontal Phase 1, Last Gate
22	OG	Output Gate
23	RG	Reset Gate
24	RD	Reset Drain
25	RD	Reset Drain
26	VSS	Output Amplifier Return
27	VOUTR	Video Output Right
28	VDD	Output Amplifier Supply
29	LOD	Lateral Overflow Drain Bottom
30	SUB	Substrate

Pin	Name	Description
60	V1	Vertical Phase 1
59	V1	Vertical Phase 1
58	V2	Vertical Phase 2
57	V2	Vertical Phase 2
56	SUB	Substrate
55	LOD	Lateral Overflow Drain Top
54	N/C	No Connection
53	N/C	No Connection
52	N/C	No Connection
51	N/C	No Connection
50	N/C	No Connection
49	N/C	No Connection
48	N/C	No Connection
47	N/C	No Connection
46	N/C	No Connection
45	N/C	No Connection
44	N/C	No Connection
43	N/C	No Connection
42	N/C	No Connection
41	N/C	No Connection
40	N/C	No Connection
39	N/C	No Connection
38	N/C	No Connection
37	N/C	No Connection
36	LOD	Lateral Overflow Drain Top
35	SUB	Substrate
34	V2	Vertical Phase 2
33	V2	Vertical Phase 2
32	V1	Vertical Phase 1
31	V1	Vertical Phase 1

Notes:

1. The leads are on a 0.070" spacing

Performance

Image Performance Operational Conditions

Description	Condition - Unless otherwise noted	Notes
Frame time ($t_{readout}$ + t_{int})	1100 ms	Includes overclock pixels
Integration time (t_{int})	250 ms	
Horizontal clock frequency	24 MHz	
Temperature	20 °C	Room temperature
Mode	integrate – readout cycle	
Operation	Nominal operating voltages and timing with min. vertical pulse width t_{VW} = 17 μs	

Image Performance Specifications

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Sample Plan[15]
Saturation Signal	Vsat Ne^{-}_{sat} Q/V	1300 54K	1440 60K 24		mV e^{-} μV/e^{-}	1	die design design
Quantum Efficiency red green blue	Rr Rg Rb		37 43 36		%QE %QE %QE	3	design design design
High Level Photoresponse Non-Linearity	PRNL		5	10	%	2	die
Photo Response Non-Uniformity	PRNU red PRNU g, b		10	20	%p-p	3	die
Readout Dark Current	Vdark, read		8		mV	5	die
Integration Dark Signal	Vdark, int		6.5	20	mV/s	4	die
Dark Signal Non-Uniformity	DSNU		2	8	mV p-p	6	die
Dark Signal Doubling Temperature	ΔT		6.3		°C		design
Read Noise	NR		16		e^{-} rms		design
Total Noise	N		18		e^{-} rms	7	design
Linear Dynamic Range	DR		70.5		dB	8	design
Red-Green Hue Shift Blue-Green Hue Shift	RG Hue Unif BG Hue Unif		4	12	%	9	die
Horizontal Charge Transfer Efficiency	HCTE		0.999995			10	die
Vertical Charge Transfer Efficiency	VCTE		0.999999				die
Blooming Protection	X_ab	800	1000		x Esat	11	design
DC Offset, output amplifier	Vodc	7.5	8.5	9.5	V	12	die
Output Amplifier Bandwidth	f_{-3dB}	80	100	122	MHz	13	design
Output Impedance, Amplifier	ROUT	130	150	200	Ohms		die
Reset Feedthru	V_{rft}		1		V	14	design

Notes:

1. Increasing output load currents to improve bandwidth will decrease these values.
2. Worst-case deviation (from 10 mV to Vsat min), relative to a linear fit applied between 0 and 65% of $Vsat_{min}$.
3. Difference between the maximum and minimum average signal levels of 146 x 146 blocks within the sensor on a per color basis as a % of average signal level.
4. T = 60 °C. Average non-illuminated signal with respect to over-clocked vertical register signal.
5. T = 60 °C, 24 MHz pixel rate, readout time = 900 ms.
6. T = 60 °C. Absolute difference between the maximum and minimum average signal levels of 146 x 146 blocks within the sensor.
7. rms deviation of a multi-sampled pixel measured in the dark including amplifier and dark current shot noise.
8. 20log (Vsat/VN) - See Note 6 and Note 1. V_N = Nread * nominal charge to voltage.
9. Gradual variations in hue (red with respect to green pixels and blue with respect to green pixels) in regions of interest (146 x 146 blocks) within the sensor when illuminated with Daylight 5500 K.
10. Measured per transfer at Vsat min. Typically, no degradation in CTE is observed up to 24 MHz.
11. X_ab is the number of times above the Vsat illumination level that the sensor will bloom by spot size doubling. The spot size is 10% of the imager height. X_ab is measured at 4 ms.
12. Video level offset with respect to ground.
13. Last stage only. Assumes 10 pF off-chip load.
14. Amplitude of feed-through pulse in VOUT due to RG coupling.
15. “Die” indicates a parameter that is measured on every sensor during the production testing. “Design” designates a parameter that is quantified during the design verification activity.

TYPICAL PERFORMANCE CURVES

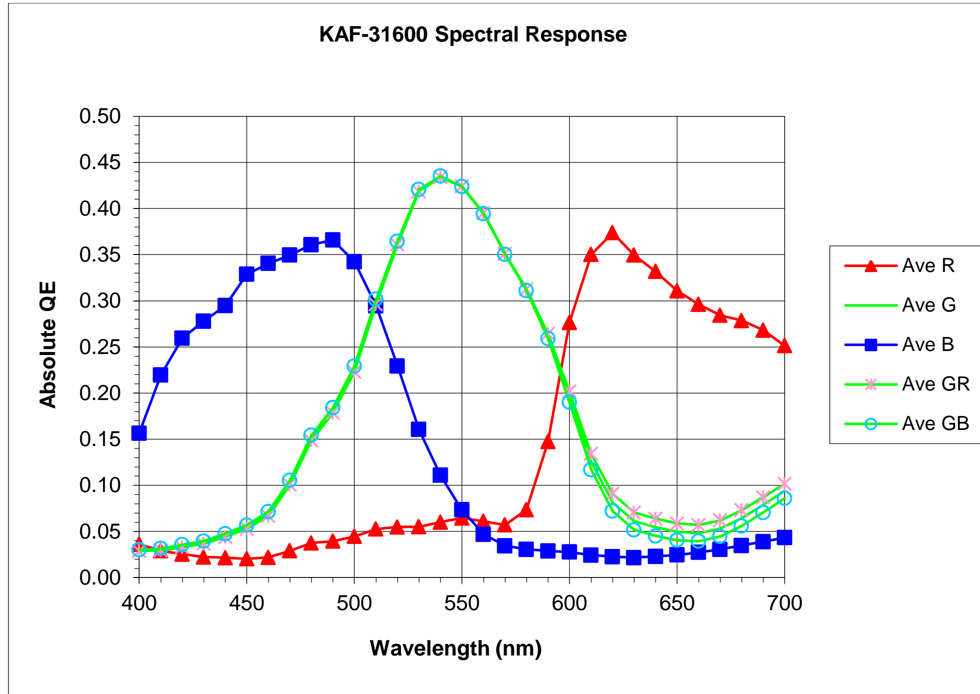


Figure 4: Typical Quantum Efficiency

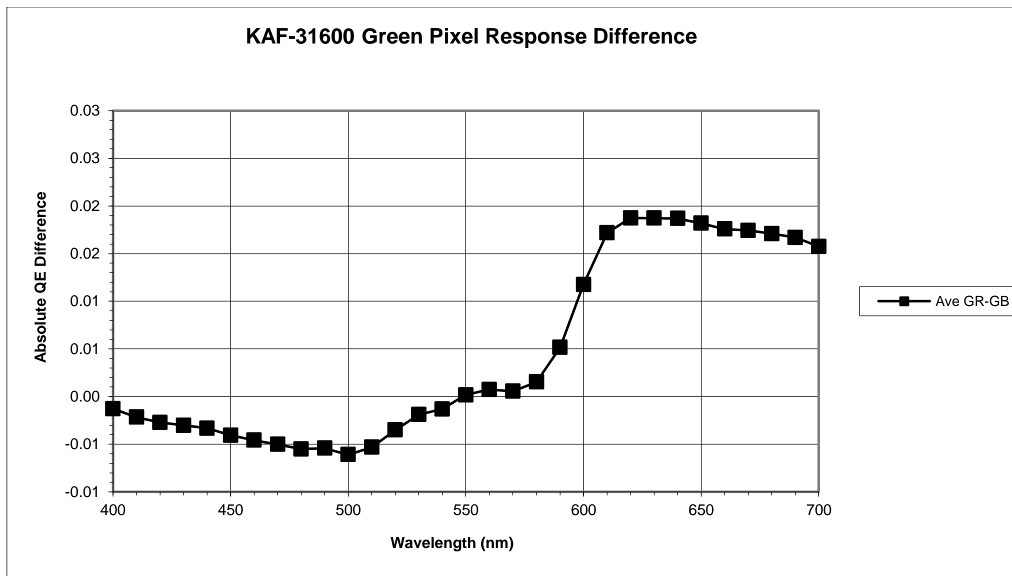


Figure 5: Typical GR - GB QE Difference

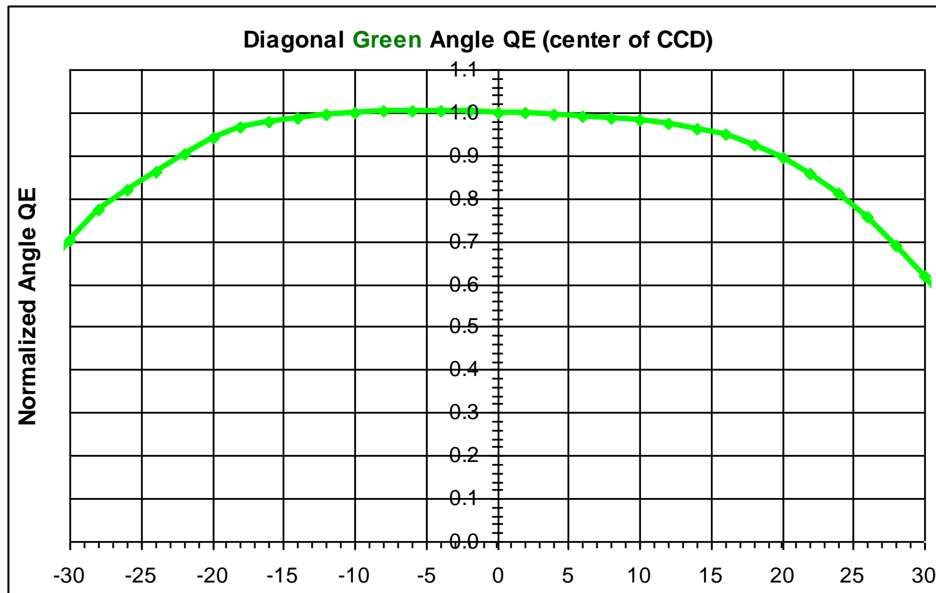


Figure 6: Typical Normalized Angle QE. (Angle in degrees)

Notes:

1. Normalized Angle QE at the center of the sensor under green LED illumination. Microlenses are proportionally offset from center to edge to compensate incident light angles. Angle QE midpoint at the corners of the sensor, therefore, results in an offset of 8° relative to this figure.

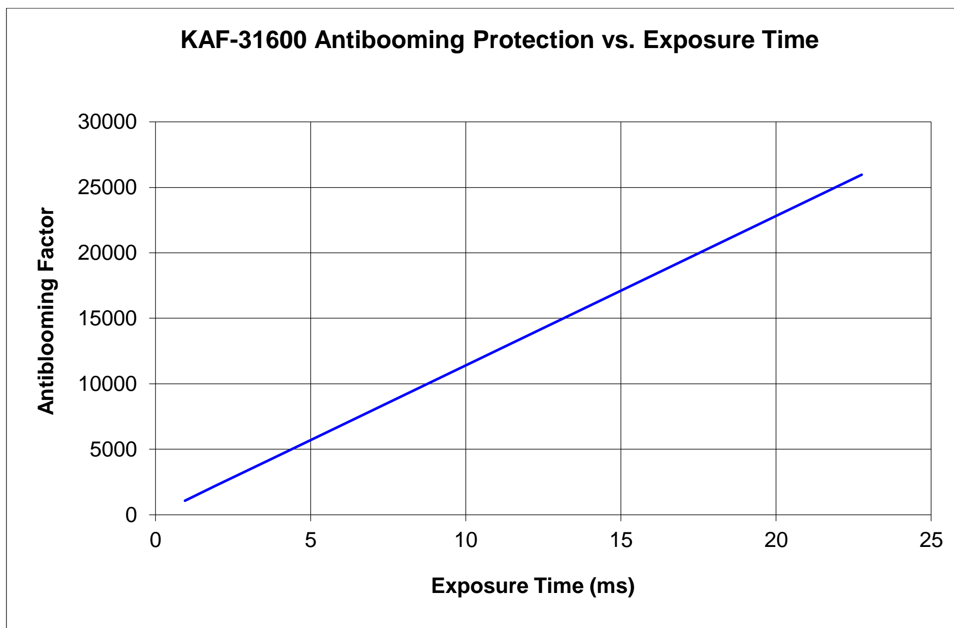


Figure 7: Typical Anti-blooming Performance

Defect Definitions

Operating Conditions

All defect tests performed at T = 20 °C, t_{int} = 250 ms and $t_{readout}$ = 850 ms

Specifications

Classification	Points	Clusters	Columns	Includes dead columns
Standard Quality (SQ)	<4,000	<50	<20	yes

Point Defects A pixel that deviates by more than 9 mV above neighboring pixels under non-illuminated conditions

-- OR --

A pixel that deviates by more than 7% above or 11% below neighboring pixels under illuminated conditions

Cluster Defect A grouping of not more than 10 adjacent point defects

Cluster defects are separated by no less than 4 good pixels in any direction

Column Defect A grouping of more than 10 point defects along a single column

-- OR --

A column that deviates by more than 0.9 mV above or below neighboring columns under non-illuminated conditions

-- OR --

A column that deviates by more than 1.5% above or below neighboring columns under illuminated conditions

Column defects are separated by no less than 4 good columns. No multiple column defects (double or more) will be permitted.

Column and cluster defects are separated by at least 4 good columns in the x direction.

Dead Columns A column that deviates by more than 50% below neighboring columns under illuminated conditions.

Saturated Columns A column that deviates by more than 100 mV above neighboring columns under non-illuminated conditions. No saturated columns are allowed.

Operation

Absolute Maximum Ratings

Description	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	V_{diode}	-0.5	+17.5	V	1,2
Gate Pin Voltages	V_{gate1}	-13.5	+13.5	V	1,3
Overlapping Gate Voltages	V_{1-2}	-13.5	+13.5	V	4
Non-overlapping Gate Voltages	V_{g-g}	-13.5	+13.5	V	5
Output Bias Current	I_{out}		-30	mA	6
LODT Diode Voltage	V_{LODT}	-0.5	+13.0	V	7
Operating Temperature	T_{OP}	0	60	°C	9

Notes:

1. Referenced to pin VSUB.
2. Includes pins: VRD, VDD, VSS, VOUT.
3. Includes pins: V1, V2, H1, H1L, H2, RG, VOG.
4. Voltage difference between overlapping gates. Includes: V1 to V2; H1, H1L to H2; H1L to VOG; V1 to H2.
5. Voltage difference between non-overlapping gates. Includes: V1 to H1, H1L; V2, VOG to H2.
6. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity). Operation at these values will reduce MTTF.
7. V1, H1, V2, H2, H1L, VOG, and VRD are tied to 0 V.
8. Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or condition is exceeded, the device will be degraded and may be damaged.
9. Noise performance will degrade at higher temperatures.

Power-up Sequence

The sequence chosen to perform an initial power-up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

1. Connect the ground pins (VSUB).
2. Supply the appropriate biases and clocks to the remaining pins.

DC Bias Operating Conditions

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	VRD	11.3	11.5	11.7	V	IRD = 0.01	
Output Amplifier Return	VVSS	0.5	0.7	1.0	V	ISS = 3.0	
Output Amplifier Supply	VVDD	14.5	15.0	15.5	V	IOUT + ISS	
Substrate	VSUB		0		V	0.01	
Output Gate	VOG	-3.2	-3.0	-2.8	V	0.01	
Lateral Drain	VLOD	9.8	10.0	10.2	V	0.01	
Video Output Current	IOUT		-5	-10	mA		1

Notes:

1. An output load sink must be applied to VOUT to activate output amplifier.

AC Operating Conditions

Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Effective Capacitance	Notes
V1 Low Level	V1L	Low	-9.2	-9.0	-8.8	V	360 nF	1
V1 High Level	V1H	High	2.3	2.5	2.7			1
V2 Low Level	V2L	Low	-9.2	-9.0	-8.8	V	440 nF	1
V2 High Level	V2H	High	2.3	2.5	2.7			1
H1 Low Level	H1L	Low	-4.7	-4.5	-4.3	V	550 pF	1
H1 High Level	H1H	High	2.5	2.7	2.9			1
H1L Low Level	$H1L_{low}$	Low	-6.7	-6.5	-6.3	V	13 pF	1
H1L High Level	$H1Lh_{igh}$	High	2.5	2.7	2.9			1
H2 Low Level	H2L	Low	-5.2	-5.0	-4.8	V	370 pF	1
H2 High Level	H2H	High	2.0	2.2	2.4			1
RG Low Level	V_{RGL}	Low	0.3	0.5	0.7	V	13 pF	1
RG High Level	V_{RGH}	High	7.8	8.0	8.2			1

Notes:

1. All pins draw less than 10 μA DC current. Capacitance values relative to SUB (substrate).

Timing

Requirements and Characteristics

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
H1, H2 Clock Frequency	f_H			24	MHz	1, 2
V1, V2 Clock Frequency	f_V			30	kHz	1, 2
H1, H2 Rise, Fall Times	t_{H1r} , t_{H1f}	5		10	%	3, 7
V1, V2 Rise, Fall Times	t_{V1r} , t_{V1f}	5		10	%	3
V1 - V2 Cross-over	V_{VCR}	-1	0	1	V	
H1 - H2 Cross-over	V_{HCR}	-2.8	-1.4	0	V	
Off Time	t_{off}	0			μs	
H1, H2 Setup Time	t_{HS}	1	5		μs	
RG Clock Pulse Width	t_{RGw}	5			ns	4
RG Rise, Fall Times	t_{RGr} , t_{RGf}	5		10	%	3
V1, V2 Clock Pulse Width	t_{Vw}	17	19		μs	2, 6,9
Pixel Period (1 Count)	t_e	42	42		ns	2
H1L – VOUT Delay	t_{HV}		5		ns	
RG - VOUT Delay	t_{RV}		5		ns	
Readout Time	$t_{readout}$	877	897		ms	6, 8
Integration Time	t_{int}		-			5, 6
Line Time	t_{line}	177	181		μs	6
Fast Flush Time	t_{flush}	149			ms	

Notes:

1. 50% duty cycle values.
2. CTE will degrade above the nominal frequency.
3. Relative to the pulse width (based on 50% of high/low levels).
4. RG should be clocked continuously.
5. Integration time is user specified.
6. Longer times will degrade noise performance.
7. The maximum specification or 10 ns whichever is greater based on the frequency of the horizontal clocks.
8. $t_{readout} = t_{line} * 4954$ lines.
9. Measured where Vclock is at 0 Volts

Edge Alignment

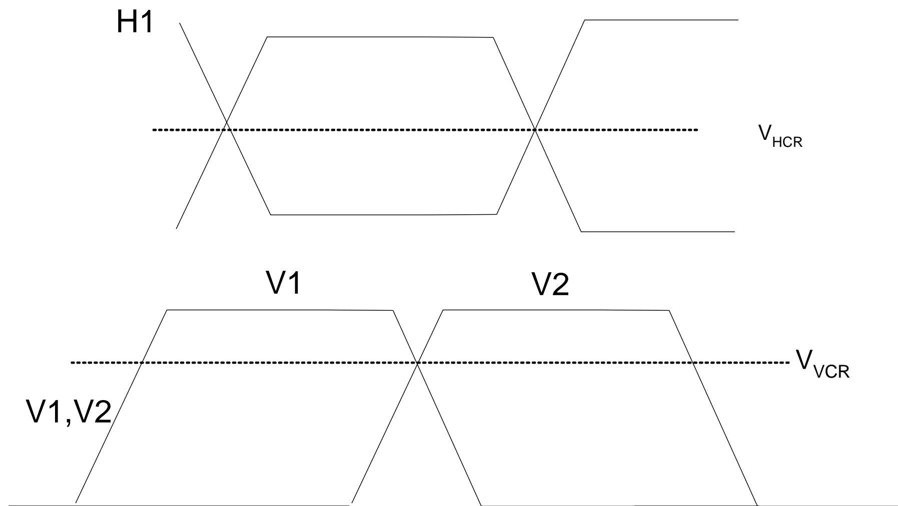


Figure 8: Timing Edge Alignment

FRAME TIMING

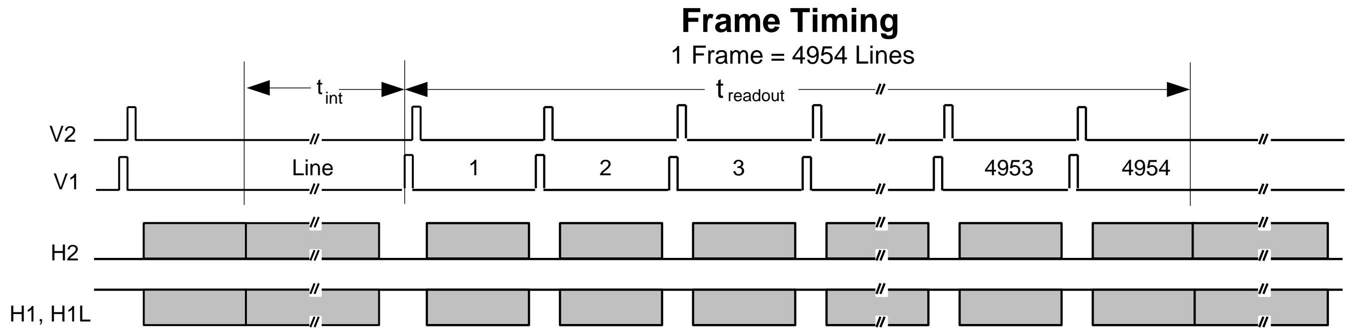


Figure 9: Frame Timing Overview

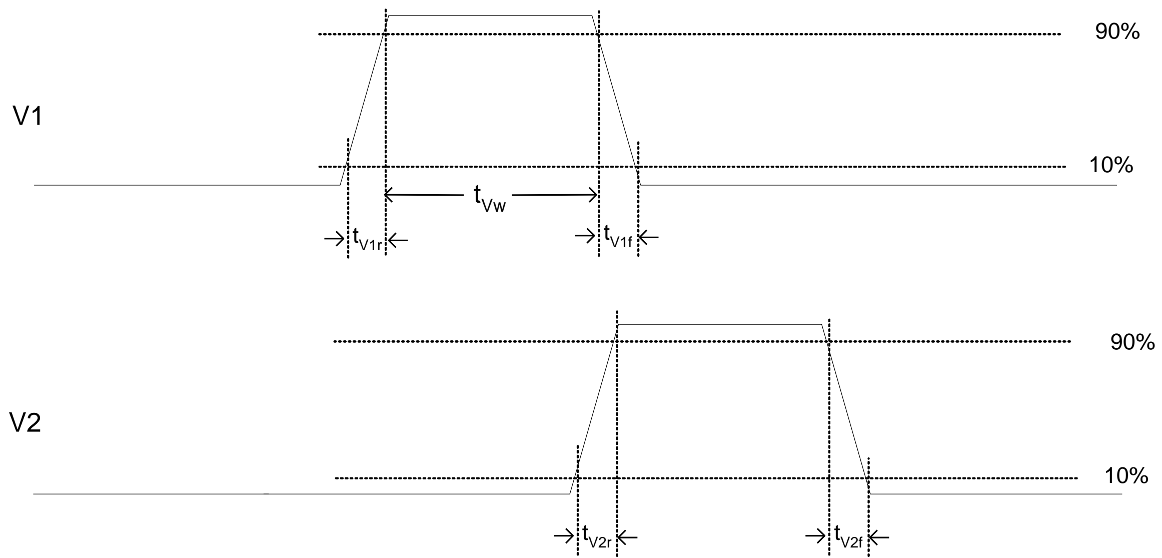


Figure 10: Frame Timing Detail

LINE TIMING

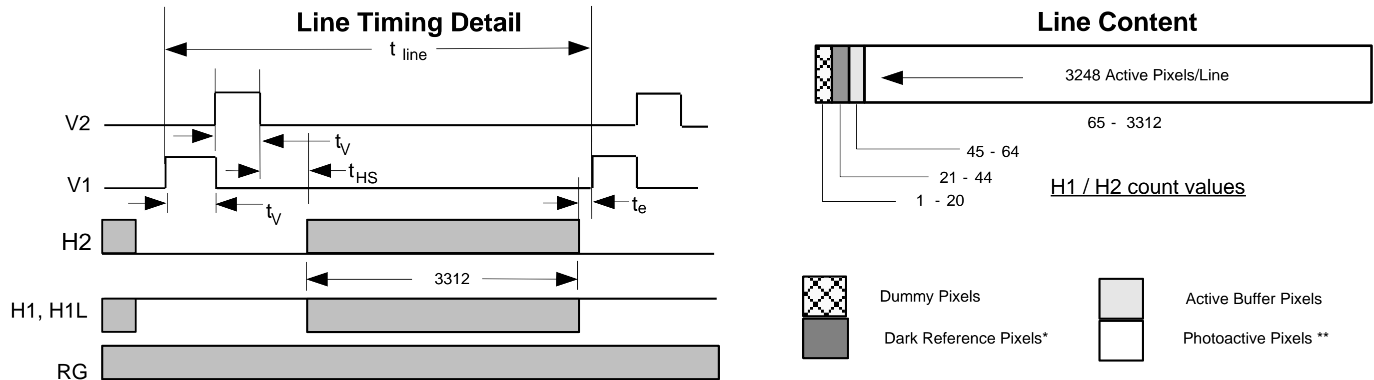


Figure 11: Line Timing

PIXEL TIMING

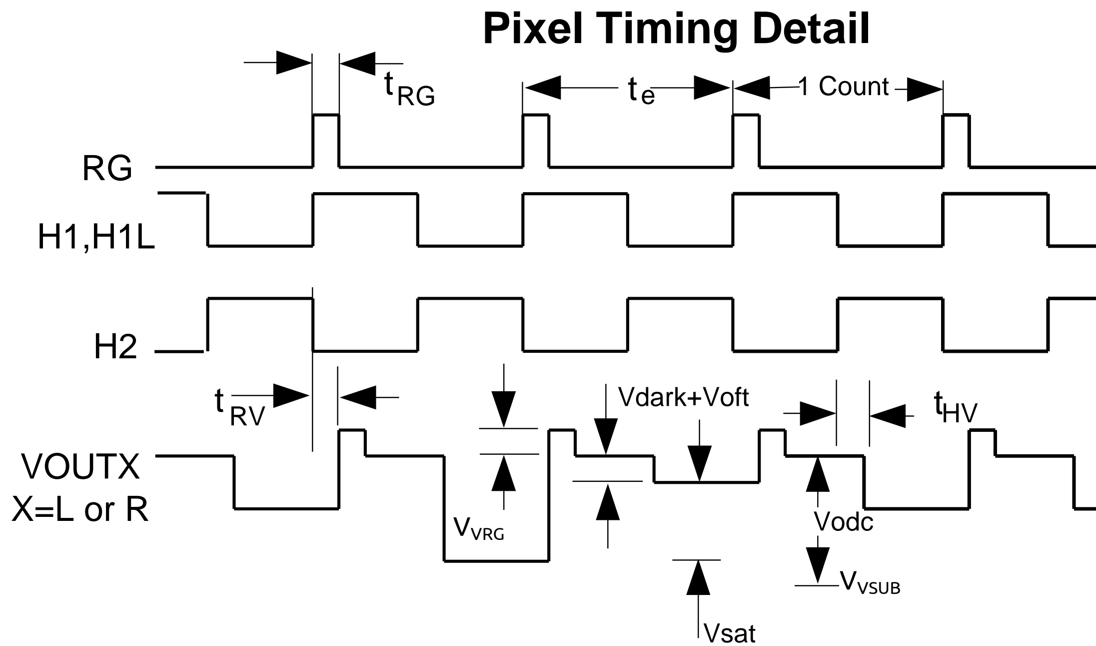


Figure 12: Pixel Timing Overview

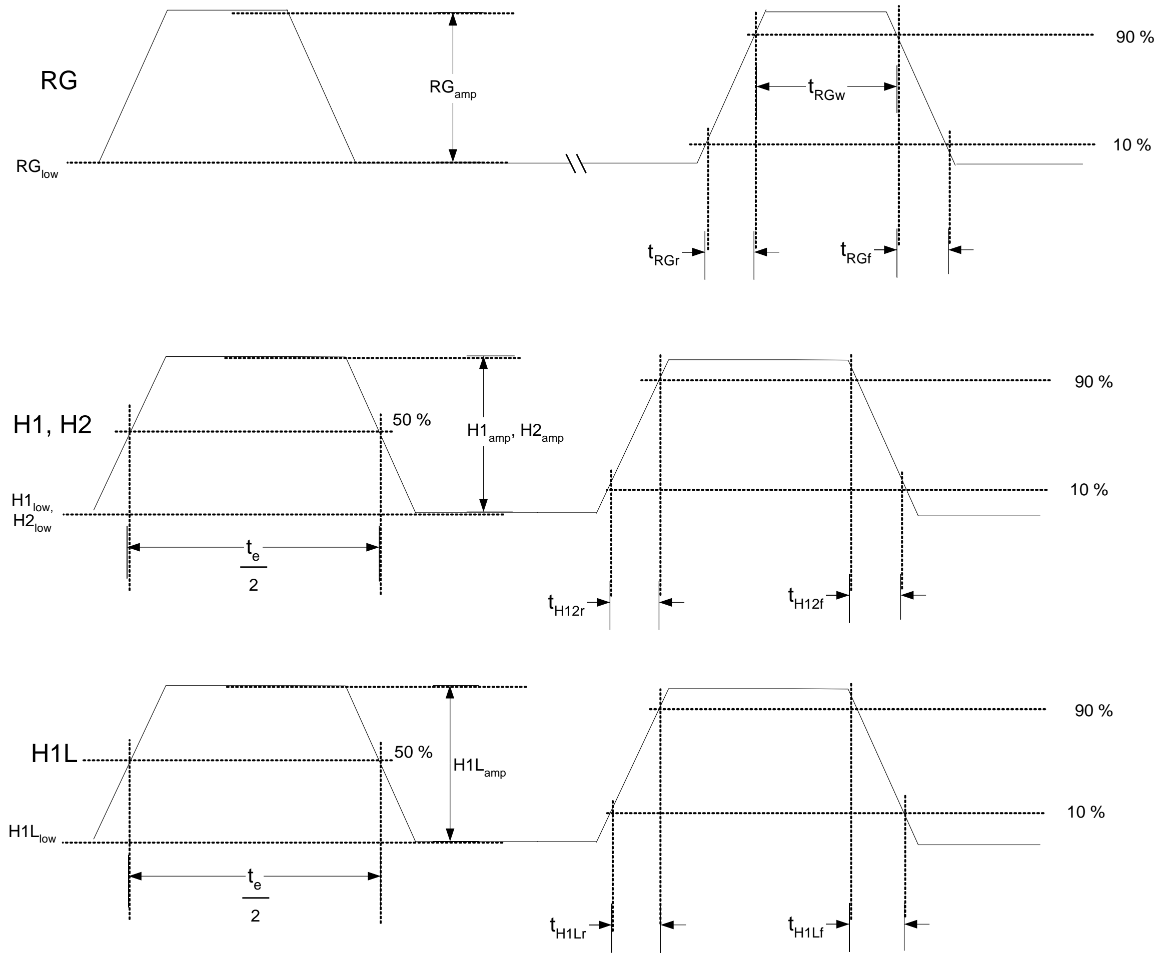


Figure 13: Pixel Timing Detail

Mode of Operation

Power-up Flush Cycle

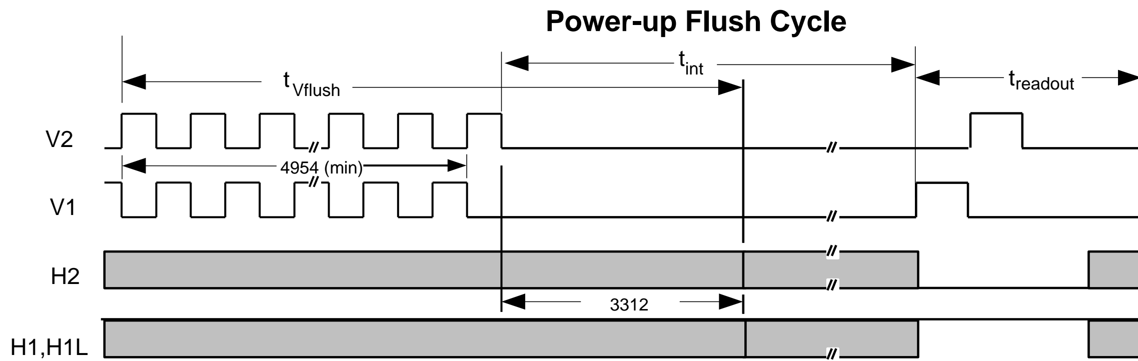


Figure 14: Power-up Flush Cycle

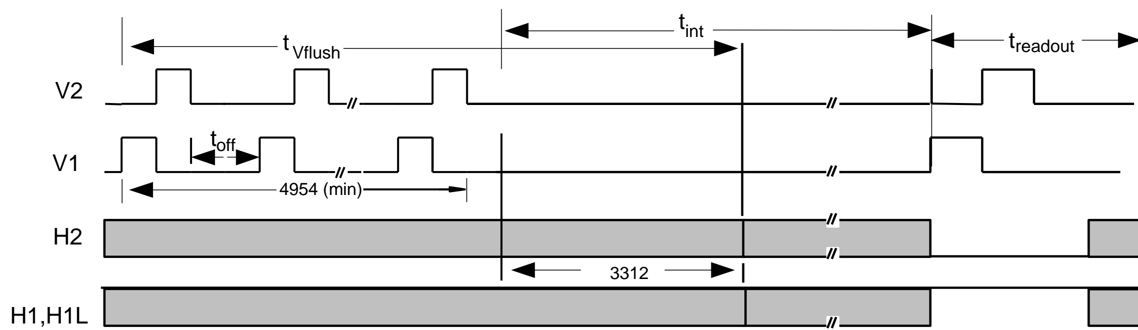


Figure 15: Modified (Slow) Flush Cycle

Storage and Handling

Storage Conditions

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-20	70	°C	1

Notes:

1. Long-term storage toward the maximum temperature will accelerate color filter degradation.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250 V per JESD22 Human Body Model test), or Class A (<200 V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

Cover Glass Care and Cleanliness

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices.*

Environmental Exposure

1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions.*
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

Soldering Recommendations

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30 W soldering iron. Heat each pin for less than 2 seconds duration.

Mechanical Drawings

Completed Assembly

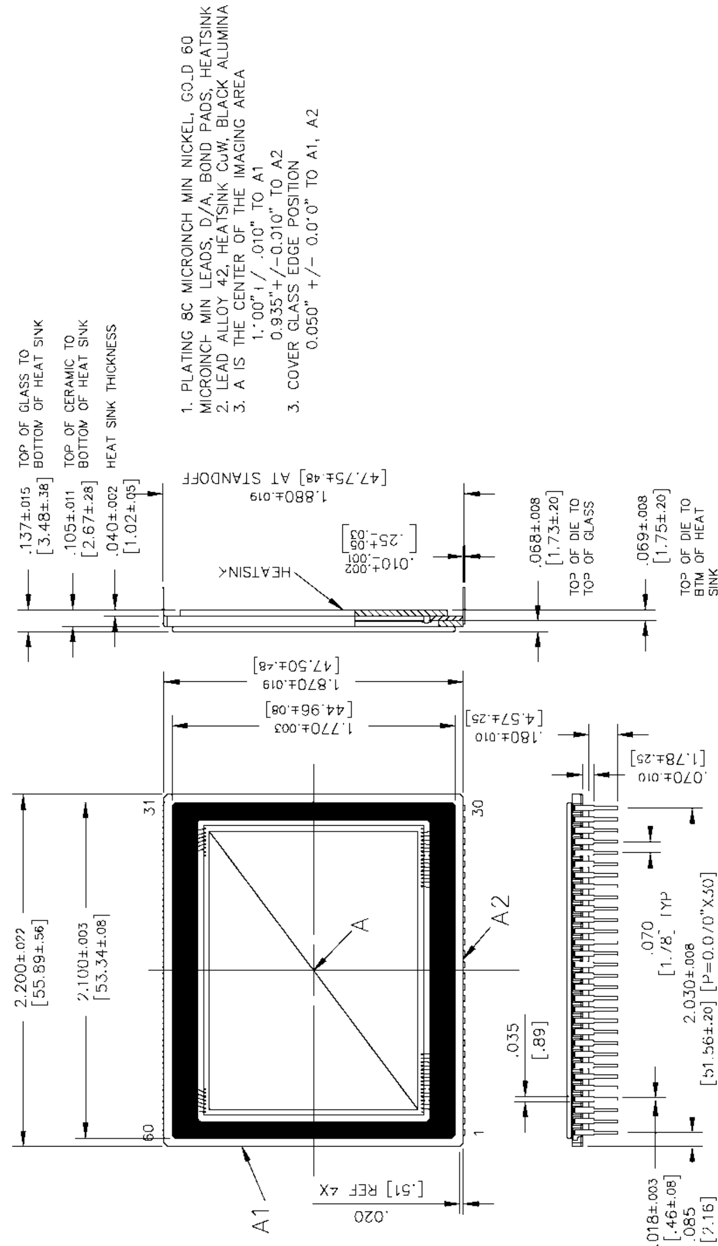


Figure 16: Completed Assembly (1 of 2)

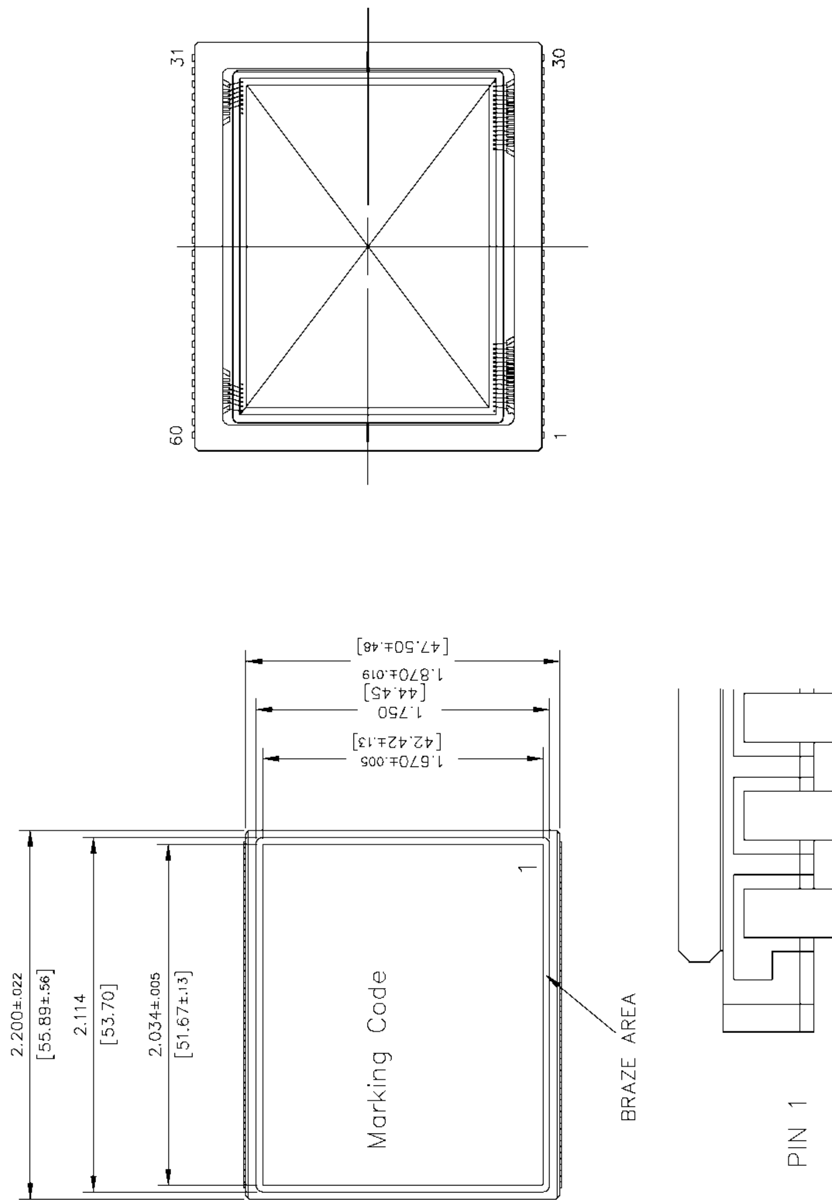


Figure 17: Completed Assembly (2 of 2)

Cover Glass Specification

1. Scratch and dig: 10 micron max.
2. Substrate material Schott D263T eco or equivalent.
3. Multilayer anti-reflective coating.

Wavelength	Total Reflectance
420-450	≤ 2%
450-630	≤ 1%
630-680	≤ 2%

Quality Assurance and Reliability

Quality and Reliability

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

Replacement

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

Liability of the Supplier

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

Liability of the Customer

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Test Data Retention

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.

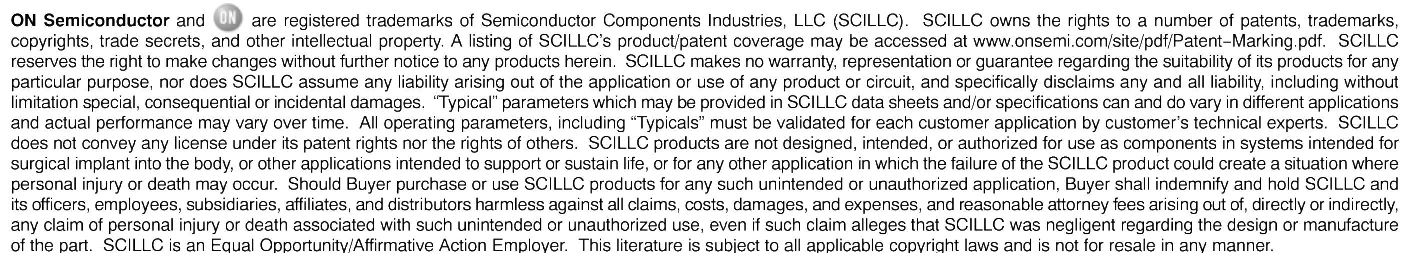
Revision Changes

MTD/PS-0860

Revision Number	Description of Changes
1.0	• Initial Release.
2.0	• Formatting Changes and: • p4 added mm dimensions for package size • p11 Changed D to d in some cases i.e. from Die to die for consistency. • p14 Added axis units (degrees) • p14 Changed 8o to 8° • p16 Removed Superscripted "9" from title description in table heading. • p20 "PIXEL TIMING" appeared twice • p26 Replace cover glass drawing with text, also added text " or equivalent" • P12 added "when illuminated with Daylight 5500 K." to note 9 • Changed package drawings. • Changed name from KAF-31600CE to KAF-31600.
3.0	• Updated format
3.1	• Changed cover glass material to D263T eco or equivalent.

PS-0042

Revision Number	Description of Changes
1.0	• Initial release with new document number, updated branding and document template • Updated *Storage and Handling* and *Quality Assurance and Reliability* sections
1.1	• Updated branding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