KAF-37500

7500 (H) x 5000 (V) Full Frame CCD Image Sensor

ON Semiconductor®

www.onsemi.com

Description

The KAF−37500 is a quad output, high performance color CCD (charge coupled device) image sensor with 7500 (H) × 5000 (V) photoactive pixels designed for a wide range of color image sensing applications including digital imaging. Each pixel contains anti-blooming protection by means of a lateral overflow drain thereby preventing image corruption during high light level conditions. Each of the 6.0 μm square pixels is selectively covered with red, green or blue pigmented filters for color separation. Microlenses are added for improved sensitivity.

The sensor utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Full Frame CCD (Square Pixels)
Total Number of Pixels	7652 (H) × 5094 (V) = 38.7 Mp
Number of Effective Pixels	7540 (H) × 5040 (V) = 38.0 Mp
Number of Active Pixels	7500 (H) × 5000 (V) = 37.5 Mp
Pixel Size	6.0 μm (H) × 6.0 μm (V)
Active Image Size	47.1 mm (H) × 32.8 mm (V) 54.1 mm (Diagonal), 645 1.5x Optical Format
Aspect Ratio	3:2
Saturation Signal	41 ke^-
Charge to Voltage Conversion	31 $\mu V/e^-$
Quantum Efficiency (RGB at Peak, Using IR Coverglass)	23%, 39%, 35%
Read Noise (f = 24 MHz)	14.0 e^-
Dark Signal (T = 60°C)	42 pA/cm^2
Dark Current Doubling Temperature	5.7°C
Linear Dynamic Range (f = 24 MHz)	68.9 dB
Charge Transfer Efficiency HCTE VCTE	 0.999995 0.999999
Blooming Protection (4 ms Exposure Time)	> 1500X Saturation Exposure
Maximum Date Rate	24 MHz

NOTE: All Parameters are specified at T = 25°C unless otherwise noted.

Figure 1. KAF−37500 Full Frame CCD Image Sensor

Features

- TRUESENSE Transparent Gate Electrode for High Sensitivity
- High Resolution
- Board Dynamic Range
- Low Noise Architecture
- Large Active Imaging Area

Application

- Professional Digital Cameras and Camera Backs

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION

Part Number	Description	Marking Code
KAF−37500−NXA−JH−AA	Special Color, Aperture, Enhanced, ESD, LOD, Microlens, Sealed IR Cover Glass, Ceramic PGA, Standard Grade	KAF−37500−NXA Serial Number
KAF−37500−NXA−JH−AE	Special Color, Aperture, Enhanced, ESD, LOD, Microlens, Sealed IR Cover Glass, Ceramic PGA, Engineering Grade	

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

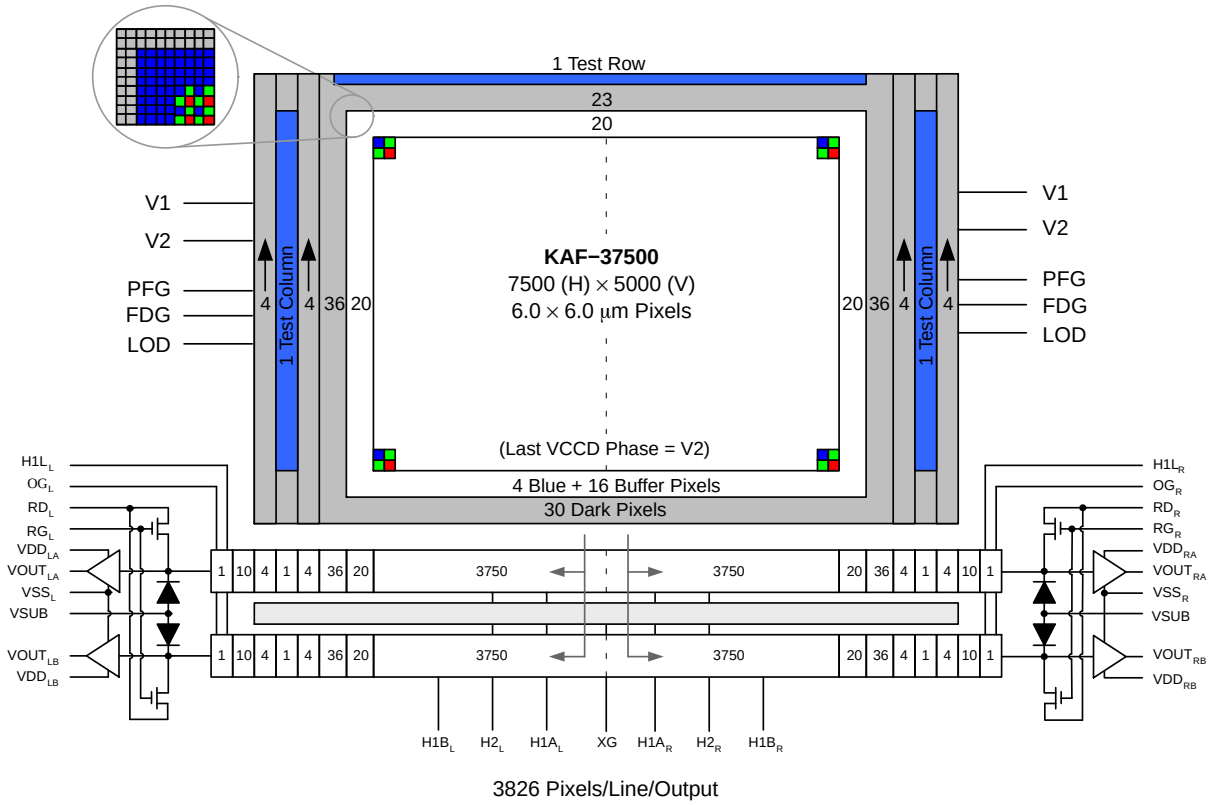


Figure 2. Block Diagram

Dark Reference Pixels

Surrounding the periphery of the device is a border of light shielded pixels creating a dark region. Within this dark region are light shielded pixels that include 36 leading dark pixels on every line. There are also 30 full dark lines at the start and 23 full dark lines at the end of every frame. Under normal circumstances, these pixels do not respond to light and may be used as a dark reference.

Dummy Pixels

Within each horizontal shift register there are 20 leading additional shift phases 1 + 10 + 4 + 1 + 4 (see Figure 2). These pixels are designated as dummy pixels and should not be used to determine a dark reference level.

Active Buffer Pixels

Forming the outer boundary of the effective active pixel region, there are 20 unshielded active buffer pixels between the photoactive area and the dark reference. These pixels are light sensitive but they are not tested for defects and non-uniformities. For the leading 20 active column pixels, the first 4 pixels are covered with blue pigment while the remaining are arranged in a Bayer pattern (R, GR, GB, B).

CTE Monitor Pixels

Two CTE test columns, one on each of the leading and trailing ends and one CTE test row are included for manufacturing test purposes.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the device. These photon-induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain to prevent crosstalk or 'blooming'. During the integration period, the V1 and V2 register clocks are held at a constant (low) level.

Charge Transport

The integrated charge from each pixel in the Vertical CCD (VCCD) is transported to the output using a two-step process. Each remaining line (row) of charge is first transported from the VCCD to a dual parallel split horizontal register (HCCD) using the V1 and V2 register clocks. The transfer to the HCCD occurs on the falling edge of V2 while H1A is held high. This line of charge may be readout immediately (dual split) or may be passed through a transfer gate (XG) into a second (B) HCCD register while the next line loads into the first (A) HCCD register (dual parallel split). Readout of each line in the HCCD is always split at the middle and, thus, either two or four outputs are used. Left (or right) outputs carry image content from pixels in the left (or right) columns of the VCCD. A separate connection to the last H1 phase ($H1L_R$ and $H1L_L$) is provided to improve the transfer speed of charge to the output amplifier. On each falling edge of H1L the output amplifier senses a new charge packet. Left and right HCCDs are electrically isolated from each other except for the common transfer gate (XG).

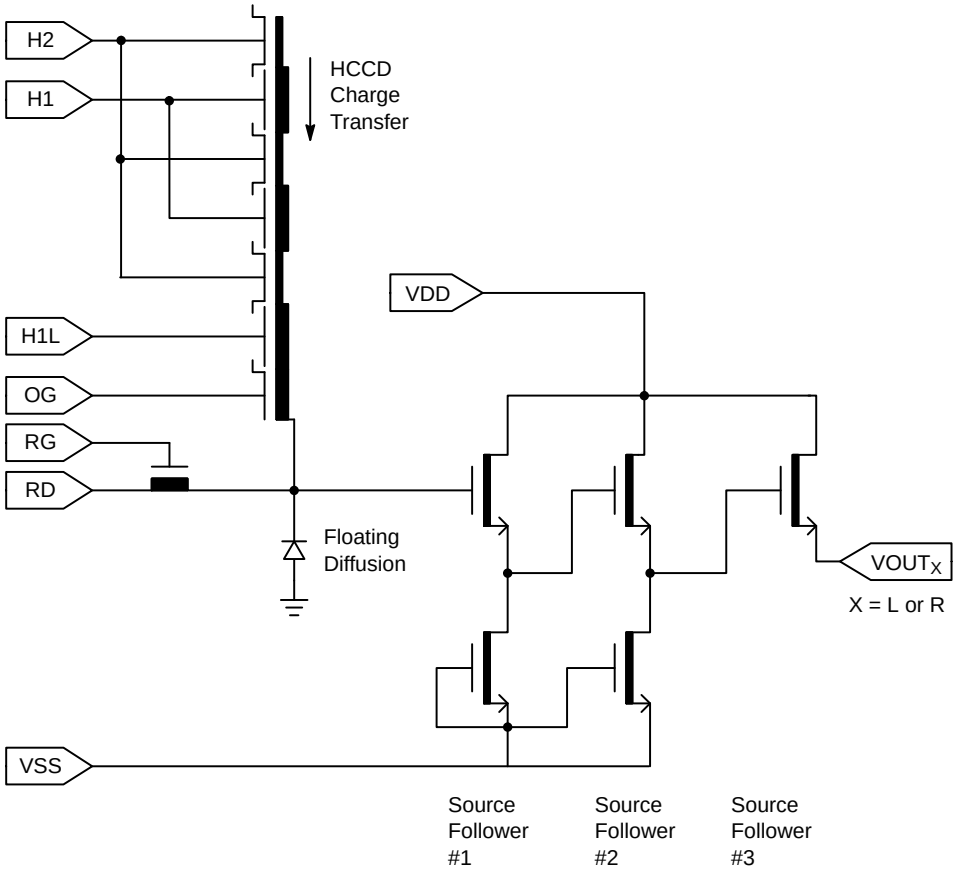
Pulsed Flush Gate/Fast Dump Gate

The Pulsed Flush Gate (PFG) feature is used to drain the charge of all pixels prior to exposure. The exception is pixels in the Fast Dump Gate (FDG) row that are drained using the separate FDG pin. Draining is accomplished by clocking V2 high while V1 is held low. This forces all charge into the V2 phase of the pixel. While V2 is high, PFG (or FDG) may be clocked high to begin draining the signal from the pixel to the LOD. Charge transfer out of the pixel is fully completed only after V2 has been clocked low plus some characteristic time period (t_{PFG}).

Horizontal Register

Output Structure

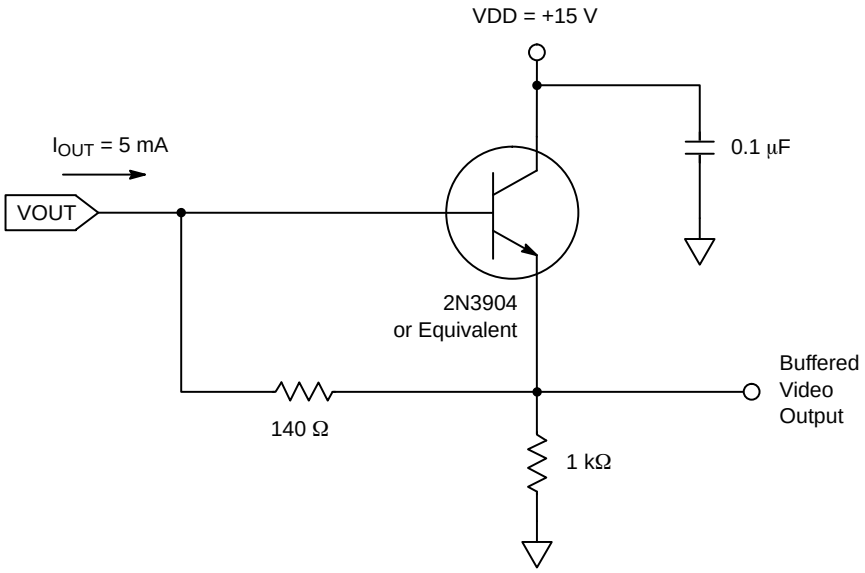
The output consists of a floating diffusion capacitance connected to a three-stage source follower. Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (RG) is clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structures, an off-chip current source must be added to the VOUT pins of the device. See Figure 4.



NOTE: Represents either the left of the right output. The designation is omitted in the figure.

Figure 3. Output Architecture (Left or Right)

Output Load



NOTE: Component values may be revised based on operating conditions and other design considerations.

Figure 4. Recommended Output Structure Load Diagram

Physical Description

Pin Description and Device Orientation

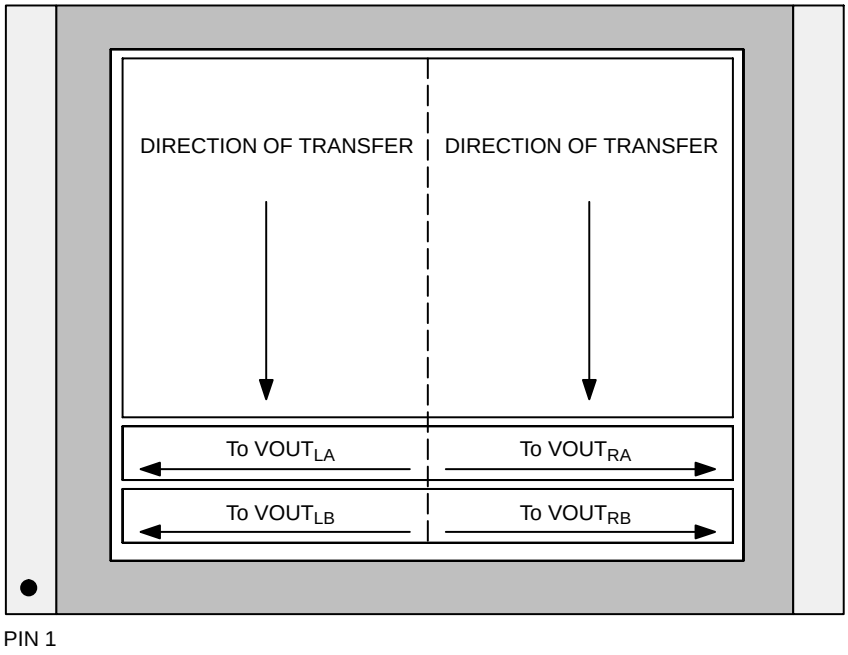


Figure 5. KAF−37500 Image Transfer Diagram (Top View − Coverglass Side)

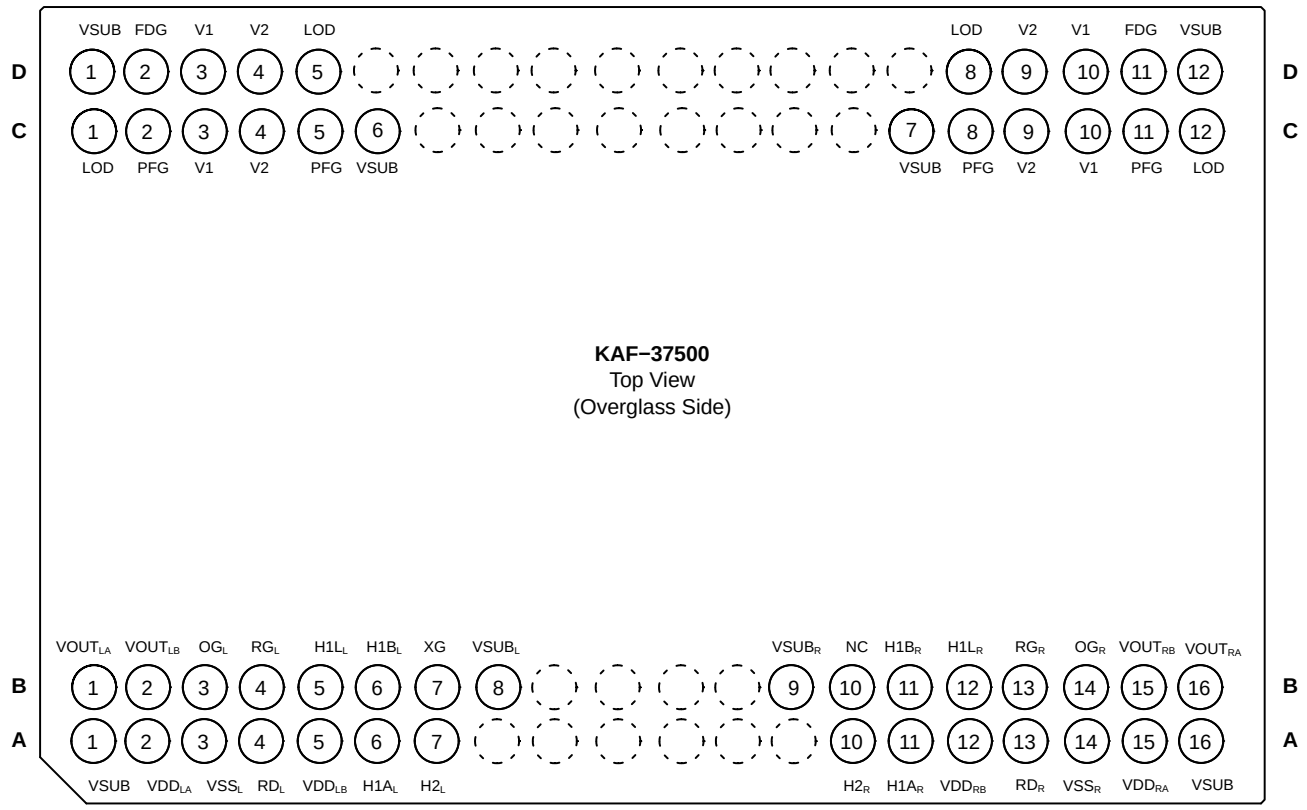


Figure 6. Pinout Diagram

Table 3. PIN DESCRIPTION

Pin	Name	Description
A1	VSUB	Substrate
A2	VDD_{LA}	Output Amplifier Supply, Left Side, A Output Stage
A3	VSS_L	Output Amplifier Return, Left Side
A4	RD_L	Reset Drain, Left Side
A5	VDD_{LB}	Output Amplifier Supply, Left Side, B Output Stage
A6	$H1A_L$	Horizontal Phase 1, Left Side
A7	$H2_L$	Horizontal Phase 2, Left Side
A8	No Pin	No Physical Pin
A9	No Pin	No Physical Pin
A10	$H2_R$	Horizontal Phase 2, Right Side
A11	$H1A_R$	Horizontal Phase 1, Right Side
A12	VDD_{RB}	Output Amplifier Supply, Right Side, B Output Stage
A13	RD_R	Reset Drain, Right Side
A14	VSS_R	Output Amplifier Return, Right Side
A15	VDD_{RA}	Output Amplifier Supply, Right Side, B Output Stage
A16	VSUB	Substrate
B1	$VOUT_{LA}$	Video Output, Left Side, A Output
B2	$VOUT_{LB}$	Video Output, Left Side, B Output
B3	OG_L	Output Gate, Left Side
B4	RG_L	Reset Gate, Left Side
B5	$H1L_L$	Horizontal Phase 1, Last Phase, Left Side
B6	$H1B_L$	Horizontal Phase 1, Left Side
B7	XG	Horizontal Transfer Gate
B8	VSUB	Substrate
B9	VSUB	Substrate
B10	NC	Physical Pin with No Connection on Die
B11	$H1B_R$	Horizontal Phase 1, Right Side
B12	$H1L_R$	Horizontal Phase 1, Last Phase, Right Side
B13	RG_R	Reset Gate, Right Side
B14	OG_R	Output Gate, Right Side
B15	$VOUT_{RB}$	Video Output, Right Side, B Output
B16	$VOUT_{RA}$	Video Output, Right Side, A Output
C1	LOD	Lateral Overflow Drain
C2	PFG	Pulse Flush Gate
C3	V1	Vertical Phase 1
C4	V2	Vertical Phase 2
C5	PFG	Pulse Flush Gate
C6	VSUB	Substrate
C7	VSUB	Substrate
C8	PFG	Pulse Flush Gate
C9	V2	Vertical Phase 2
C10	V1	Vertical Phase 1
C11	PFG	Pulse Flush Gate
C12	LOD	Lateral Overflow Drain
D1	VSUB	Substrate
D2	FDG	Fast Dump Gate
D3	V1	Vertical Phase 1
D4	V2	Vertical Phase 2
D5	LOD	Lateral Overflow Drain
D6	No Pin	No Physical Pin
D7	No Pin	No Physical Pin
D8	LOD	Lateral Overflow Drain
D9	V2	Vertical Phase 2
D10	V1	Vertical Phase 1
D11	FDG	Fast Dump Gate
D12	VSUB	Substrate

1. Pins with the same name are to be tied together on the circuit board and have the same timing. In addition, pins labeled with left (‘L’) and right (‘R’) designations may also be tied together except for VOUT pins.
2. To achieve optimal output signal matching, electrical layout of the PCB should be made as symmetrical as possible relative to the left and right sides of the sensor.

IMAGING PERFORMANCE

Table 4. TYPICAL OPERATIONAL CONDITIONS

(Unless otherwise noted, the Specifications are measured using the following conditions.)

Description	Condition	Units	Notes
Readout Time ($t_{READOUT}$)	1,060	ms	Includes Overclock Pixels
Integration Time (t_{INT}) Varies per Test: Bright Field Dark Filed Saturation Low Light	 250 1 250 33	 ms s ms ms	
Horizontal Clock Frequency	24	MHz	
Temperature	25	°C	Room Temperature
Mode	Integrate − Readout Cycle		
Operation	Worst Case Operating Conditions		

Table 5. SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Verification Plan
Saturation Signal	N_{SAT} N_{e^-SAT} Q/V	1,200 − −	1,280 41 31	− − −	mV ke$^-$ μV/e$^-$	1, 17	Die[15] Design[16] Design[16]
Quantum Efficiency at Peak Red Green Blue	QE_{MAX}	 − − −	 23 39 35	 − − −	%		Design[16]
Photoresponse Non-Linearity	PRNL	−	3	10	%	2	Die[15]
Photoresponse Non-Uniformity	PRNU	−	10	25	% p−p	3	Die[15]
Readout Dark Signal	$V_{DARK,READ}$	−	17	20	mV/s	4, 14	Die[15]
Integration Dark Signal	$V_{DARK,INT}$	−	3	10	mV/s	5, 14	Die[15]
Dark Signal Non-Uniformity	DSNU	−	1	4	mV p−p	6, 18	Die[15]
Dark Signal Doubling Temperature	ΔT	−	5.7	−	°C		Design[16]
Read Noise	N_R	−	14	−	e$^-$ rms		Design[16]
Dynamic Range	DR	−	69.3	−	dB	7	Design[16]
Estimated Linear Dynamic Range	DR_{LIN} (Est.)	−	68.4	−	dB		Design[16]
Red-Green Hue Shift Blue-Green Hue Shift	$RG_{HueUnif}$ $BG_{HueUnif}$	− −	1.4 2.6	12 12	%	8	Die[15]
Horizontal Charge Transfer Efficiency	HCTE	0.999995	−	−		9	Die[15]
Vertical Charge Transfer Efficiency	VCTE	0.999998	0.999999	−			Die[15]
Blooming Protection	X_{AB}	−	800		x V_{SAT}	10	Design[16]
DC Offset, Output Amplifier	V_{ODC}	6.0	7.7	9.5	V	11	Die[15]
Output Amplifier Bandwidth	f_{-3dB}	−	220	−	MHz	12	Design[16]

Table 5. SPECIFICATIONS (continued)

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Verification Plan
Output Impedance, Amplifier	R_{OUT}	100	135	300	Ω		Die[15]
Reset Feedthrough	V_{RFT}	−	0.5	−	V	13	Design[16]

1. Increasing output load currents to improve bandwidth will decrease the conversion factor (Q/V).
2. Worst-case deviation (at 15 mV & 90% N_{SATmin}), relative to a linear fit applied between 0 and 65% of N_{SATmin}.
3. Difference between the maximum and minimum average signal levels of 168 × 168 blocks within the sensor on a per color basis as a % of average signal level.
4. T = 60°C and t_{INT} = 0, average non-illuminated signal with respect to over-clocked horizontal register signal.
5. T = 60°C, average non-illuminated signal with respect to over-clocked vertical register signal.
6. T = 60°C. Absolute difference between the maximum and minimum average signal levels of 168 × 168 blocks within the sensor.
7. 20Log ($N_e^-{}_{SAT}$ / N_R). Specified at T = 60°C.
8. Gradual variations in hue (red with respect to green pixels and blue with respect to green pixels) in regions of interest (168 × 168 blocks) within the sensor.
9. Measured per transfer above and below (~70% V_{SAT} min) saturation exposure levels. Typically, no degradation in HCCD CTE is observed up to 24 MHz.
10. X_{AB} is the number of times above the V_{SAT} illumination level that the sensor will bloom by spot size doubling. The spot size is 10% of the imager height. X_{AB} is measured at 4 ms.
11. Video level offset with respect to ground.
12. Last stage only. Assumes 5 pF off-chip load.
13. Amplitude of feedthrough in VOUT during RG clocking.
14. Total dark signal = ($V_{DARK,INT} \cdot t_{INT}$) + $V_{DARK,READ} \cdot t_{READOUT}$
15. A parameter that is measured on every sensor during production testing.
16. A parameter that is quantified during the design verification activity.
17. t_{INT} = 1,000 ms.
18. Specified at T = 60°C.

TYPICAL PERFORMANCE CURVES

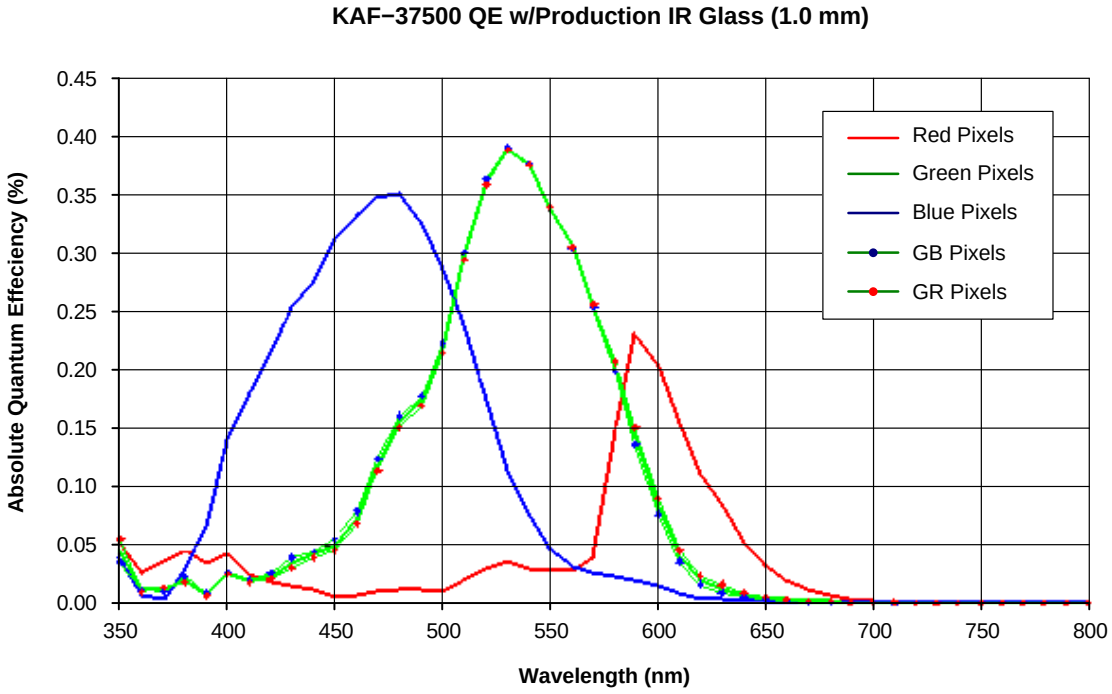


Figure 7. Typical Quantum Efficiency

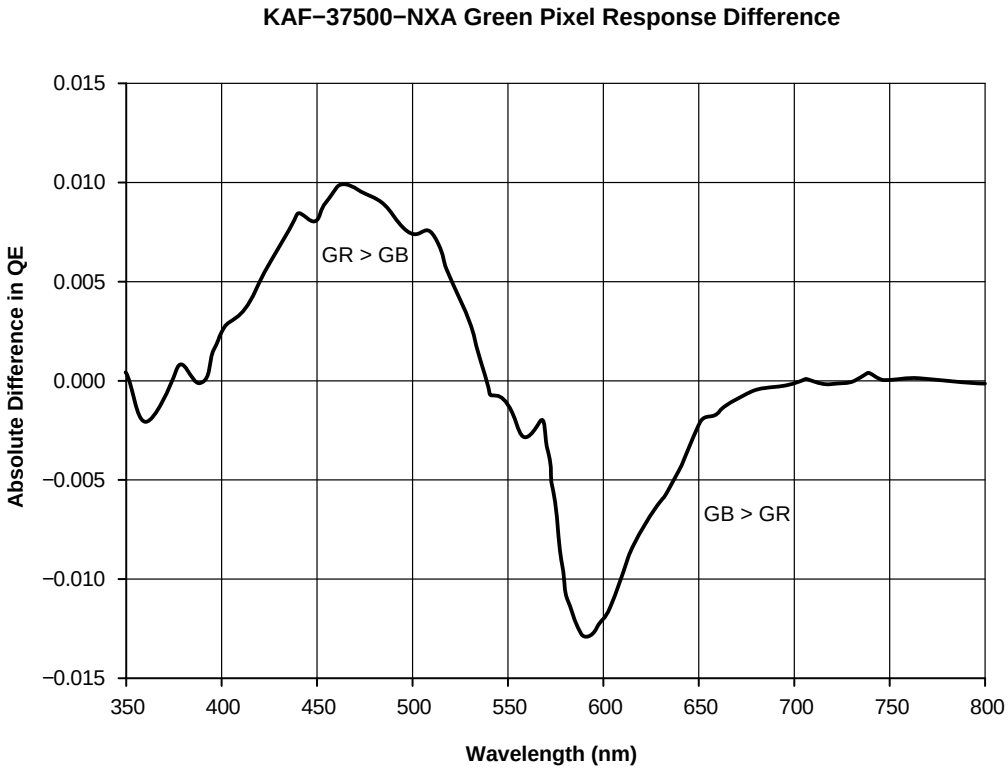


Figure 8. Typical GR−GB QE Difference

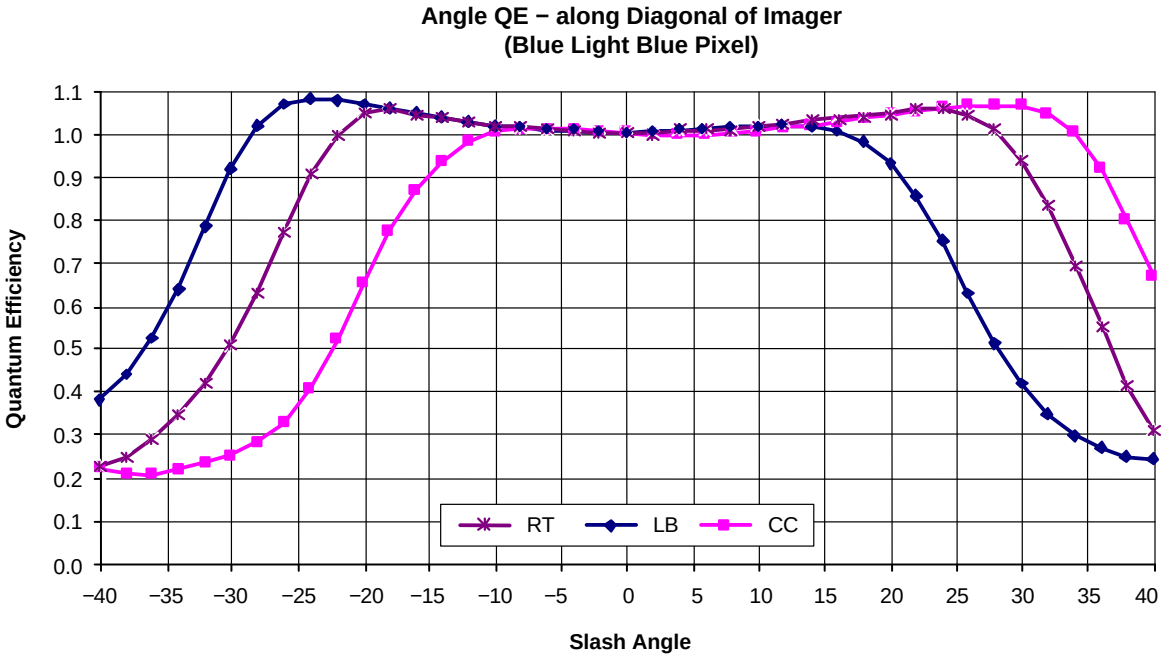


Figure 9. Typical Normalized Angle QE

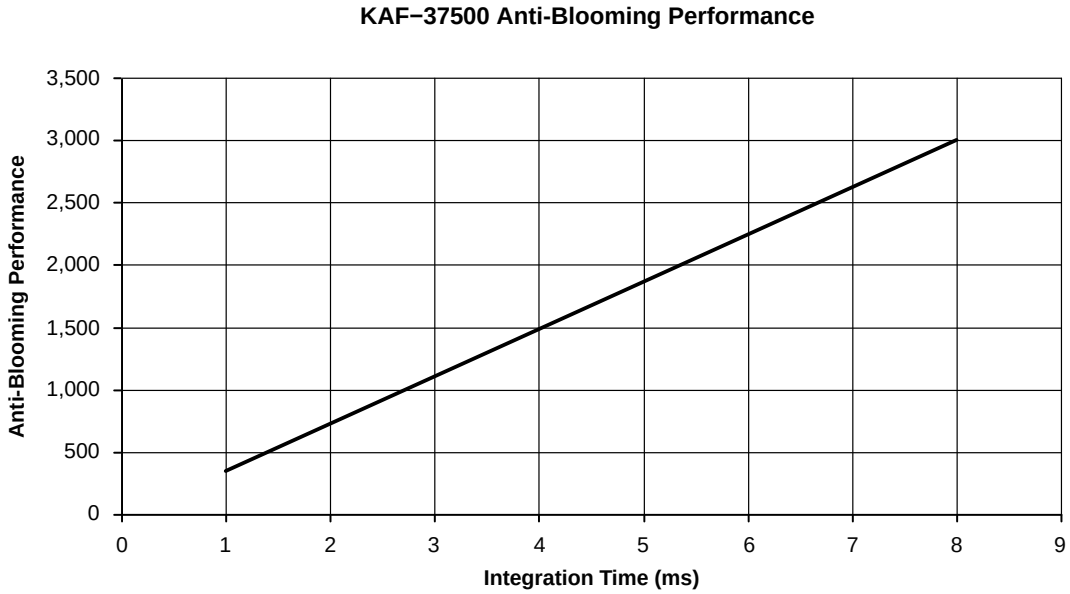


Figure 10. Typical Anti-Blooming Performance

DEFECT DEFINITIONS

Operating Conditions

Bright defect tests performed at T = 25°C, t_{INT} = 250 ms and $t_{READOUT}$ = 1,060 ms.
Dark defect tests performed at T = 25°C, t_{INT} = 1,000 ms and $t_{READOUT}$ = 1,060 ms.

Table 6. SPECIFICATIONS

Classification	Points	Clusters	Columns	Includes Dead Columns
Standard Grade	≤ 4,000	≤ 83 (Small and Large Clusters) ≤ 5 (Large Clusters)	≤ 20	Yes

Point Defects

A pixel that deviates by more than 9 mV above neighboring pixels under non-illuminated conditions.

A pixel that deviates by more than 7% above or 11% below neighboring pixels under illuminated conditions.

Small Cluster Defect

A grouping of not more than 10 adjacent point defects. Cluster defects are separated by no less than 4 good pixels in any direction.

Large Cluster Defect

A grouping of more than 10 but not greater than 20 adjacent point defects. A single large cluster is not to exceed 5 adjacent pixels within the same color plane.

Column Defect

A grouping of more than 10 point defects along a single column.

A column that deviates by more that 1.2 mV above or below neighboring columns under non-illuminated conditions.

A column that deviates by more that 1.5% above or below neighboring columns under illuminated conditions.

Column and cluster defects are separated by at least 4 good columns in the x direction. No multiple column defects (double or more) will be permitted.

Dead Column

A column that deviates by more than 50% below neighboring columns under illuminated conditions.

Saturated Column

A column that deviates by more than 100 mV above neighboring columns under non-illuminated conditions. No saturated columns are allowed.

OPERATION

Table 7. ABSOLUTE MAXIMUM RATINGS

(Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or condition is exceeded, the device will be degraded and may be damaged.)

Description	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	V_{DIODE}	−0.5	20	V	1, 2
Gate Pin Voltages	V_{GATE1}	−14.3	14.5	V	1, 3
Reset Gate Pin Voltage	V_{RG}	−0.5	14.5	V	1
Overlapping Gate Voltages	$V_{1−2}$	−14.3	14.5	V	4
Non-Overlapping Gate Voltages	$V_{g−g}$	−14.3	14.5	V	5
Output Bias Current	I_{OUT}	−	−30	mA	6
LOD Diode Voltage	V_{LOD}	−0.5	13.5	V	1
Operating Temperature	T_{OP}	0	60	°C	7

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Referenced to pin VSUB.
2. Includes pins: RD, VDD_{LA}, VDD_{LB}, VDD_{RA}, VDD_{RB}, VSS_L, VSS_R, $VOUT_{LA}$, $VOUT_{LB}$, $VOUT_{RA}$, & $VOUT_{RB}$.
3. Includes pins: V1, V2, $H1A_L$, $H1A_R$, $H1B_L$, $H1B_R$, $H1L_L$, $H1L_R$, $H2_L$, $H2_R$, OG_L, OG_R, PFG, FDG, & XG.
4. Voltage difference between overlapping gates. Includes: V1 to $V2_X$, $H1_X$/$H1L_X$ to $H2_X$, $H1L_X$ to OG_X, V1 to $H2_X$, PFG to V1/V2, FDG to V1/V2, XG to $H1A_X$/$H1B_X$/$H2_X$. [where “X” can be “L” or “R”]
5. Voltage difference between non-overlapping gates. Includes: V1 to $H1A_X$/$H1B_X$/$H1L_X$, V2 to XG, $H2_X$ to PFG /FDG, PFG to FDG. [where “X” can be “L” or “R”]
6. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity). Operation at these values will reduce MTTF (Mean Time to Failure).
7. Noise performance will degrade at higher temperatures.

Power-Up Sequence

The sequence chosen to perform an initial power-up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

1. Connect the Ground Pins (VSUB)
2. Supply the Appropriate Biases and Clocks to the Remaining Pins

Table 8. DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	RD	11.3	11.5	11.7	V	I_{RD} = 0.01	
Output Amplifier Return	V_{SS}	0.5	0.7	1.0	V	I_{SS} = 3.0	
Output Amplifier Supply	V_{DD}	14.5	15.0	15.5	V	I_{OUT} + I_{SS}	
Substrate	SUB	−	0	−	V	0.01	
Output Gate	OG	−2.2	−2.0	−1.8	V	0.01	
Lateral Drain/Guard	LOD	9.8	10.0	10.2	V	0.01	
Video Output Load Current	I_{OUT}	−	−5	−10	mA		1

1. An output load sink must be applied to each of the four VOUT pins to activate output amplifier – see Figure 4.

AC Operating Conditions

Table 9. CLOCK LEVELS

Description	Symbol	Level	Min.	Nom.	Max.	Units	Effective Capacitance	Notes
Vertical CCD Clock − Phase 1	V1	Low	−9.2	−9.0	−8.8	V	463 nF	1, 2, 3
		High	2.3	2.5	2.7	V		
Vertical CCD Clock − Phase 2	V2	Low	−9.2	−9.0	−8.8	V	495 nF	1, 2, 3
		High	3.3	3.5	3.7	V		
Horizontal CCD Clock − Phase 1A	H1A	Low	−4.2	−4.0	−3.8	V	384 pF	1, 2, 3
		High	1.8	2.0	2.2	V		
Horizontal CCD Clock − Phase 1B	H1B	Low	−4.2	−4.0	−3.8	V	488 pF	1, 2, 3
		High	1.8	2.0	2.2	V		
Horizontal CCD Clock − Phase 2	H2	Low	−4.2	−4.0	−3.8	V	958 pF	1, 2, 3
		High	1.8	2.0	2.2	V		
Horizontal CCD Clock − Phase 1 (Last)	H1L	Low	−6.2	−6.0	−5.8	V	23 pF	1, 2, 3
		High	1.8	2.0	2.2	V		
Reset Gate	RG	Low	0.8	1.0	1.2	V	26 pF	1, 2, 3
		High	7.8	8.0	8.2	V		
Pulsed Flush Gate	PFG	Low	−9.2	−9.0	−8.8	V	294 nF	1, 2, 3
		High	4.8	5.0	5.2	V		
Fast Dump Gate	FDG	Low	−9.2	−9.0	−8.8	V	132 pF	1, 2, 3
		High	4.8	5.0	5.2	V		
Horizontal CCD Transfer Gate	XG	Low	−4.7	−4.5	−4.3	V	282 nF	1, 2
		High	2.8	3.0	3.2	V		

1. All pins draw less than 10 A DC current.
2. Capacitance values relative to SUB (substrate).
3. Capacitance values of left and right pins combined where appropriate.

TIMING

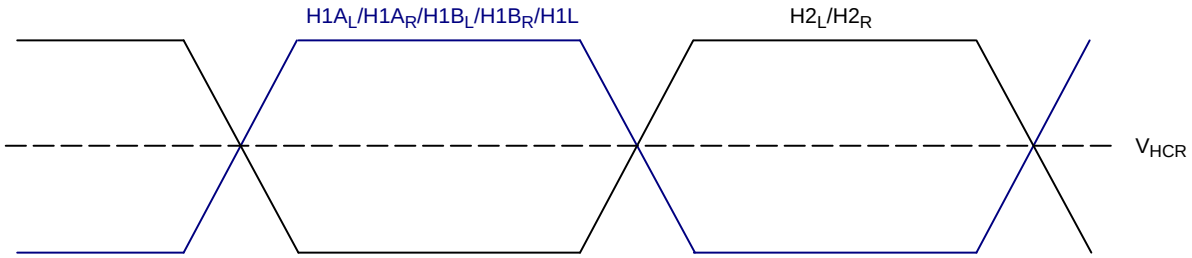
Table 10. REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Min.	Nom.	Max.	Units	Notes
H1, H2 Clock Frequency	f_H	−	−	24	MHz	1, 2
V1, V2 Clock Frequency	f_V	−	−	25	kHz	1, 2
H1, H2 Rise, Fall Times	t_{H1r}, t_{H1f}	5	−	10	%	3, 7
V1, V2 Rise, Fall Times	t_{V1r}, t_{V1f}	5	−	10	%	3
V1−V2 Cross-over	V_{VCR}	0	1.0	2.7	V	
H1−H2 Cross-over	V_{HCR}	−2.0	−1.0	0	V	
H1L Rise − H2 Fall Cross-over	V_{H1LCR}	−2.0	−1.0	1.0	V	9
H1, H2 Setup Time	t_{HS}	3	−	−	μs	
V2, H1A Delay	t_{D1}	3	−	−	μs	
H1A, XG Delay	t_{D2}	30	−	34	μs	
XG, V2 Delay	t_{D3}	3	−	−	μs	
PFG Holdoff Time	t_{PFG}	180	−	−	μs	
FDG Holdoff Time	t_{FDG}	20	−	−	μs	
RG Clock Pulse Width	t_{RGw}	5	−	−	ns	4
RG Rise, Fall Times	t_{RGr}, t_{RGf}	5	−	10	%	3
V1, V2 Clock Pulse Width	t_V	20	−	−	μs	2, 6
Pixel Period (1 Count)	t_e	41.67	−	−	ns	2
H1L−VOUT Delay	t_{HV}	−	5	−	ns	
RG−VOUT Delay	t_{RV}	−	5	−	ns	
Line Time	t_{LINE} − DS t_{LINE} − DPS	202.42 242.42	− −	− −	μs	6, 10, 11
Readout Time	$t_{READOUT}$ − DS $t_{READOUT}$ − DPS	1.03 0.62	− −	− −	s	6, 8,10, 11
Frame Rate	t_{FRAME} − DS t_{FRAME} − DPS	0.95 1.58	− −	− −	fps	12
Integration Time	t_{INT}	−	−	−		5, 6
Fast Flush Time	t_{FLUSH}	40	−	−	ms	

1. 50% duty cycle values.
2. CTE will degrade above the maximum frequency.
3. Relative to the pulse width (based on 50% of high/low levels).
4. RG should be clocked continuously.
5. Integration Time is user specified.
6. Longer times will degrade noise performance.
7. The maximum specification or 10 ns whichever is greater based on the frequency of the horizontal clocks.
8. $t_{READOUT} = t_{LINE} \cdot 5094$ lines.
9. The charge capacity near the output could be degraded if the voltage at the clock crossover point is outside this range.
10. Dual Split operation of the video output.
11. Dual-Parallel Split operation of the video output.
12. At $1/60^{th}$ second integration time.
13. DS = Dual Split; DPS = Dual Parallel Split.

Edge Alignment

Horizontal Clock



Vertical Clock

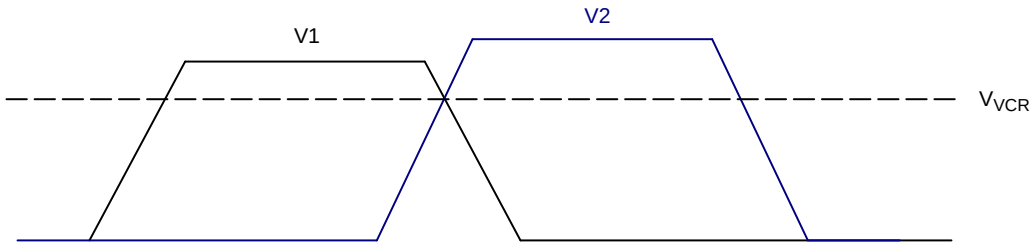


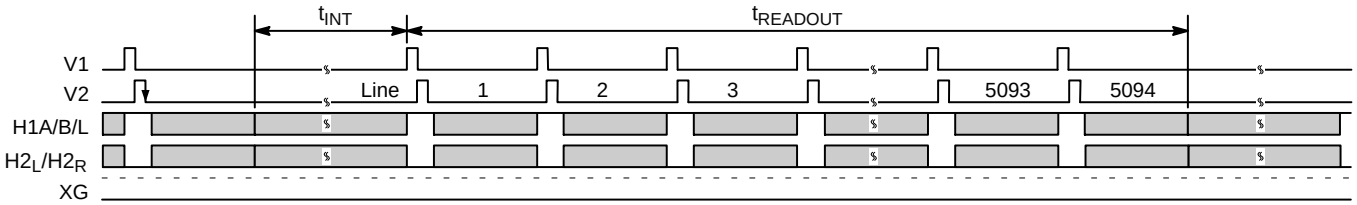
Figure 11. Timing Edge Alignment

Frame Timing

Dual split timing reads the pixels out of $VOUT_{LA}$ and $VOUT_{RA}$. $H1B_L$ and $H1B_R$ may be grounded in this operating mode.

Dual-Parallel Split timing reads pixels out of all four outputs with even lines reading out of $VOUT_{LA}$ and $VOUT_{RA}$ and odd lines reading out of $VOUT_{LB}$ and $VOUT_{RB}$.

Frame Timing − Dual Split



Frame Timing − Dual-Parallel Split

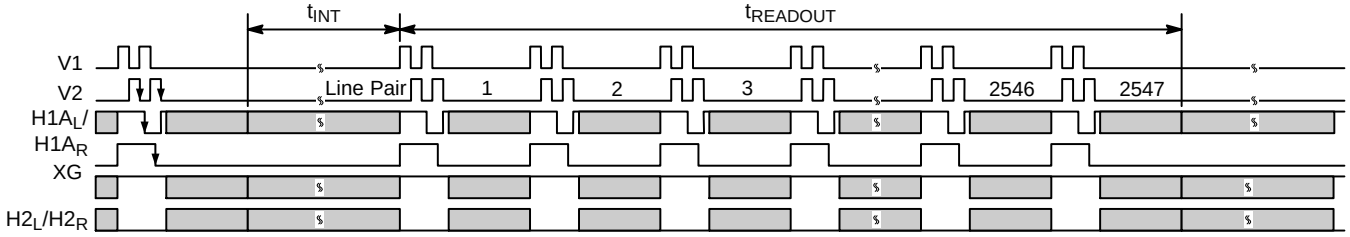


Figure 12. Frame Timing

Frame Timing Detail

Vertical Clocks

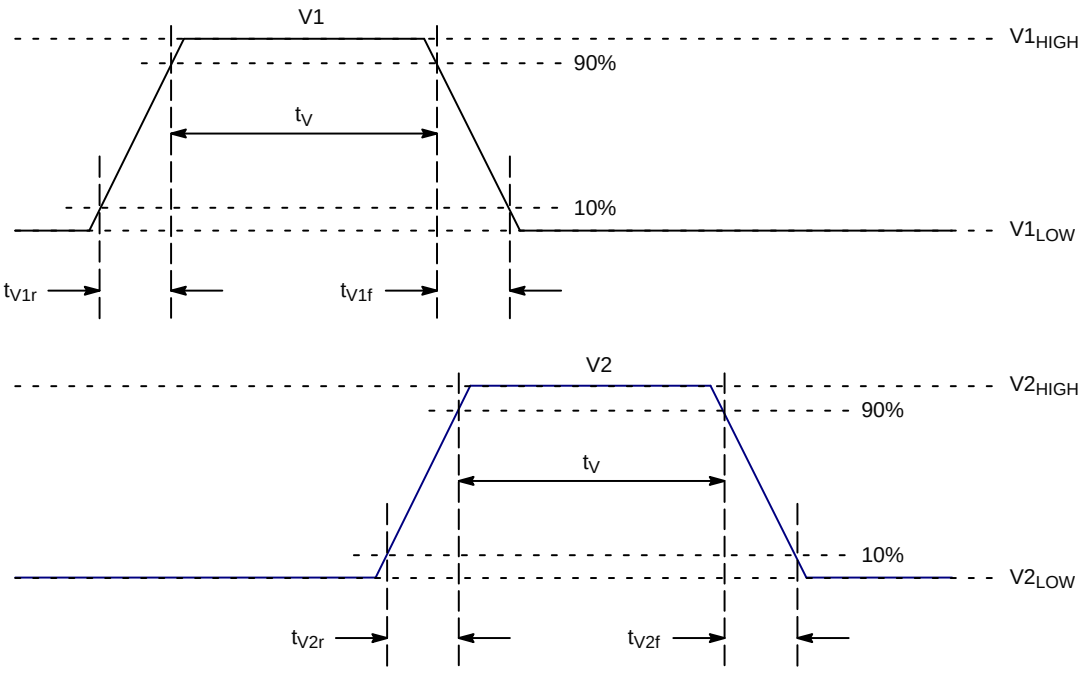
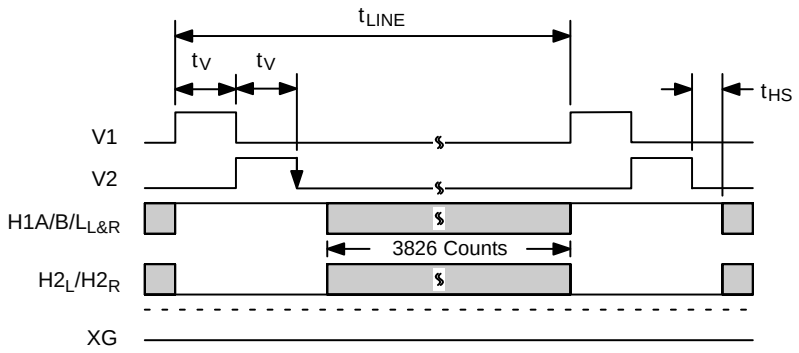


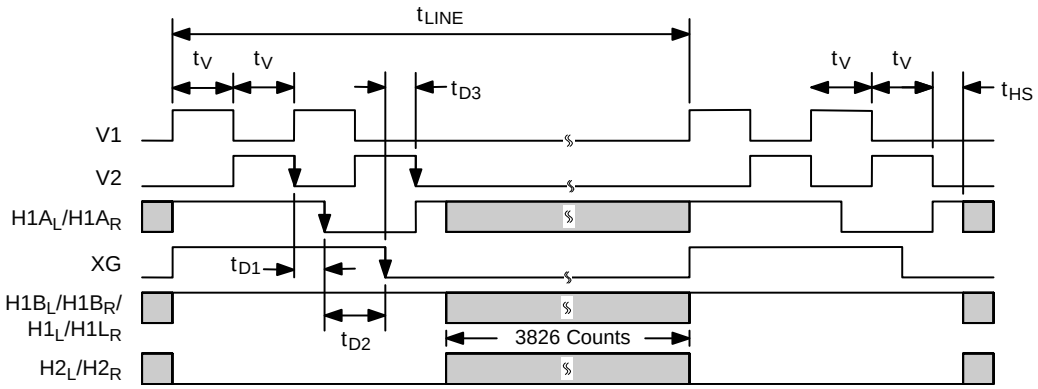
Figure 13. Frame Timing Detail

Line Timing (Each Output)

Line Timing − Dual Split



Line Timing − Dual-Parallel Split



Line Timing − Block Diagram

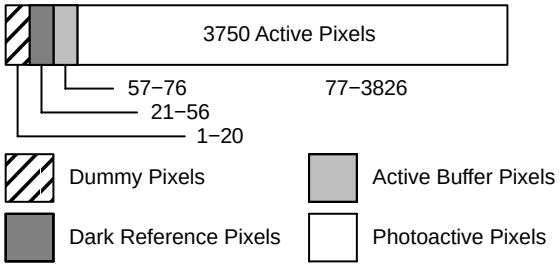


Figure 14. Line Timing

Pixel Timing

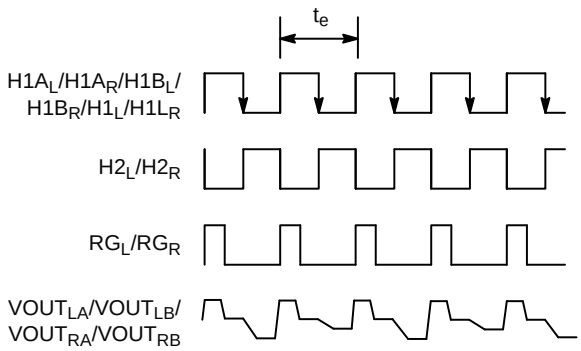
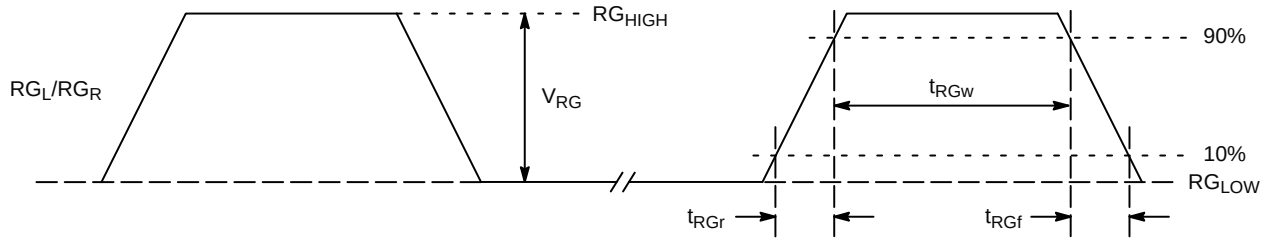


Figure 15. Pixel Timing

Pixel Timing Detail

Reset Clock



Horizontal Clocks

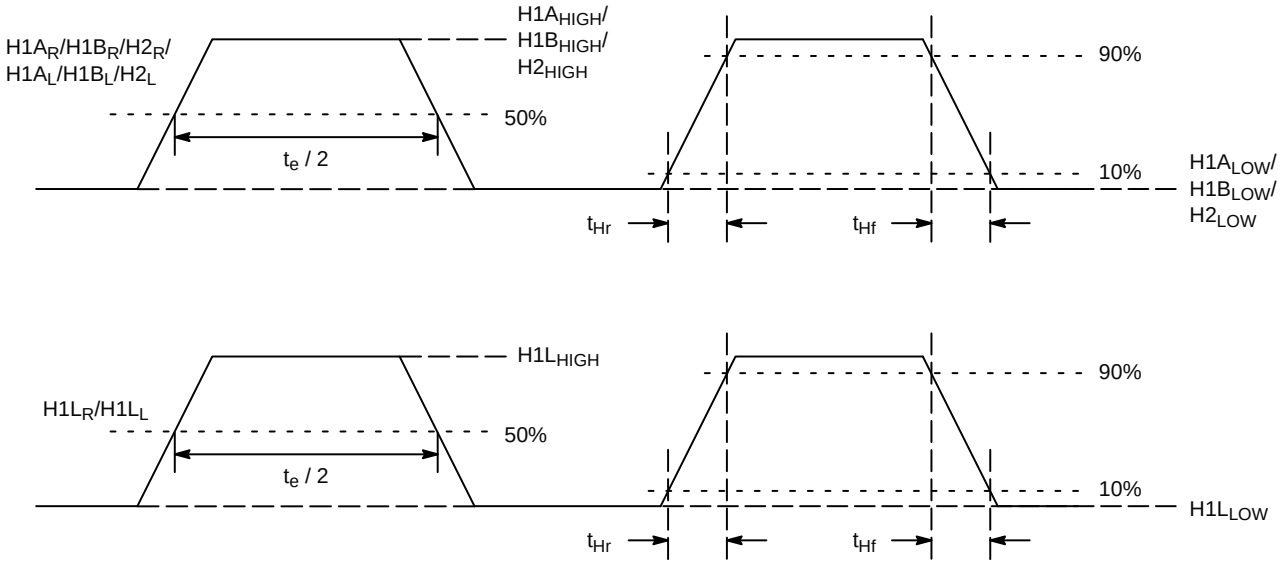


Figure 16. Pixel Timing Detail

MODE OF OPERATION

Power-Up Flush Cycle

Pulse Flush Gate Timing

The pulse flush gate, (PFG), resets all pixels in the array (except the fast dump gate row). Charge transfer out of the pixel is fully completed only after V2 has been clocked low as shown.

Frame Timing − Pulse Flush Operation

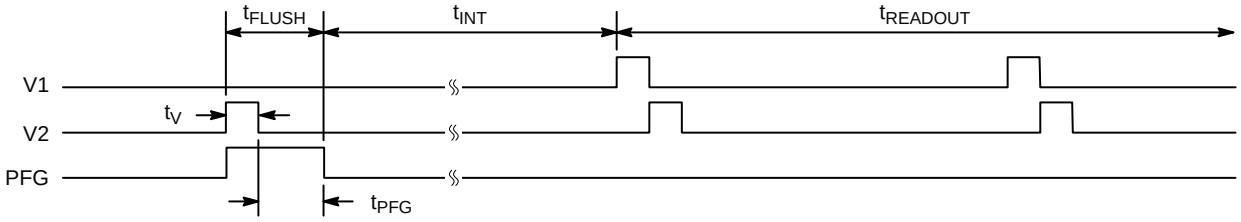


Figure 17. Frame Timing − Pulse Flush

Fast Dump Gate (FDG) Timin

The fast dump gate clock, (FDG), only resets pixels that happen to be in the fast dump gate row. Charge transfer out of the pixel is fully completed only after the vertical clock (V2), has been clocked low plus the characteristic time period (t_{FDG}). The position of the fast dump gate row is illustrated in Figure 18 through Figure 21, including the timing required for a simple 1 line dump operation. Pixels colored in yellow represent dumped pixels.

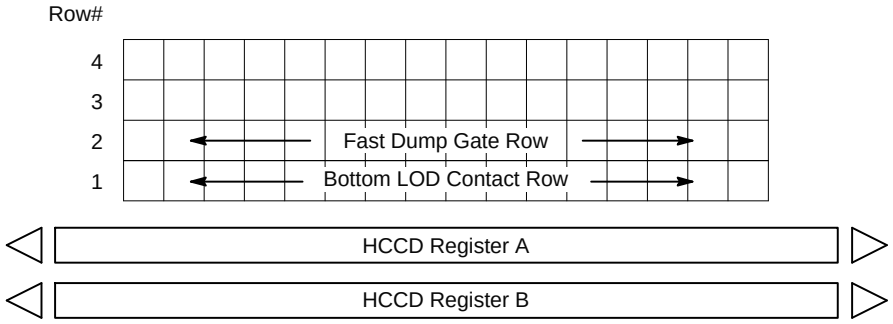


Figure 18. Fast Line Dump Layout

Line Timing − Fast Dump Gate (1 Line Dump)

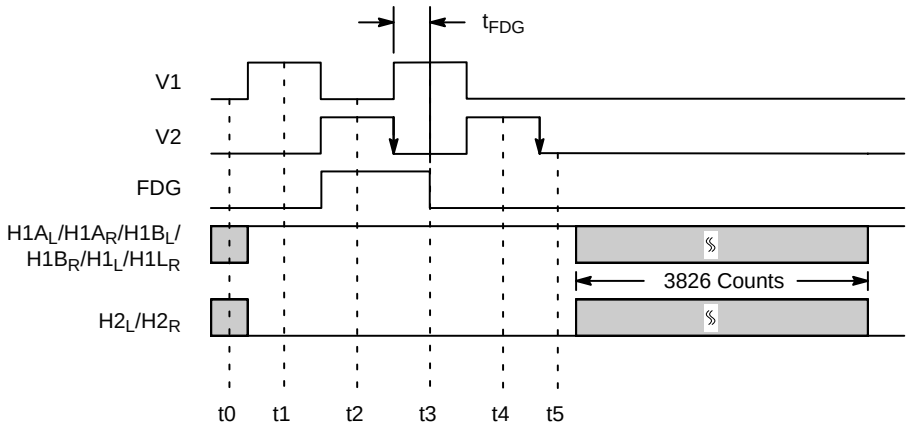


Figure 19. One Line Dump Timing Example

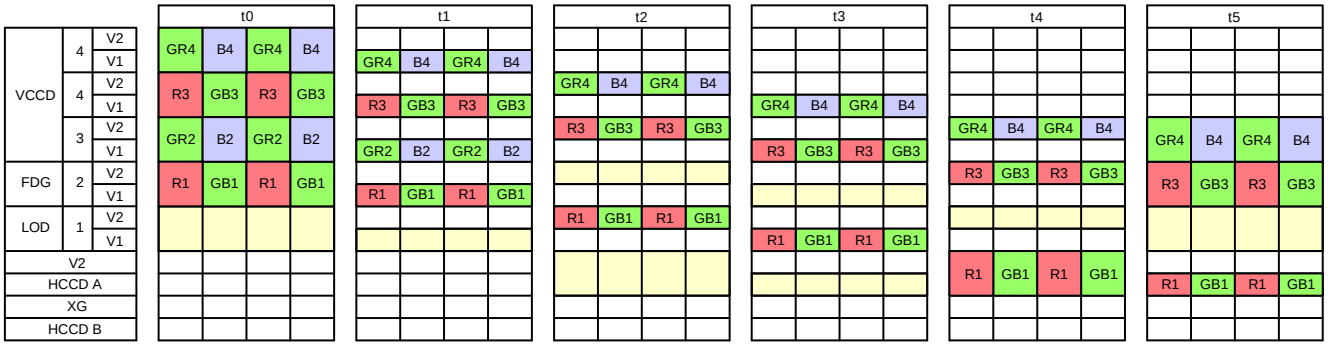


Figure 20. One Line Dump Pixel Illustration

Line Timing − Fast Dump Gate (3-Line Dump)

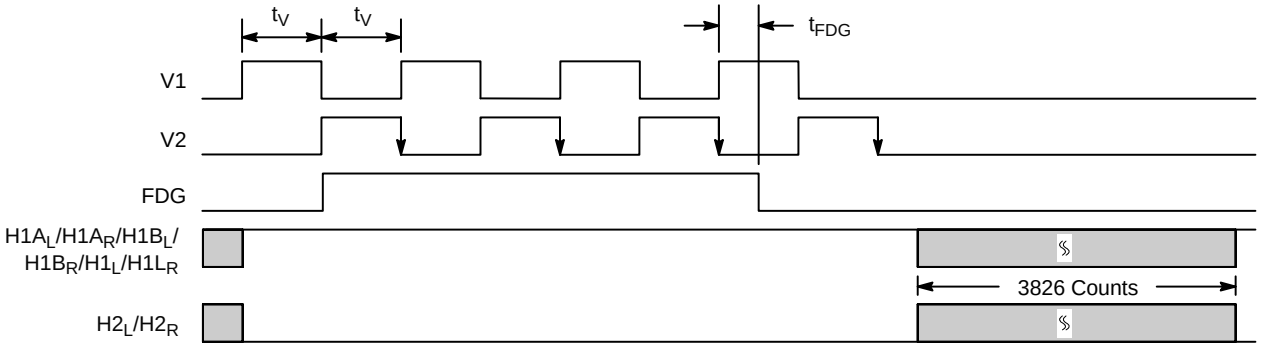


Figure 21. 3-Line Dump Timing Example

MECHANICAL INFORMATION

Completed Assembly

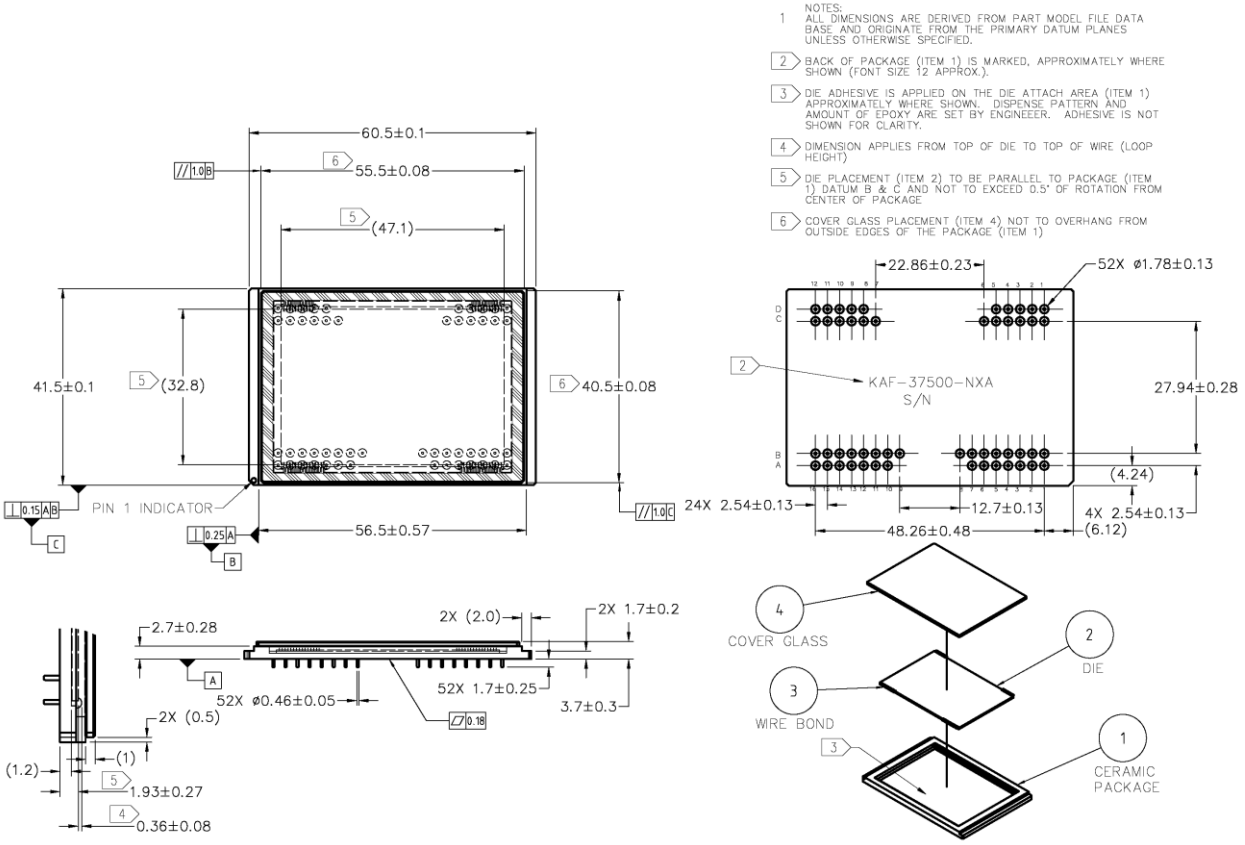


Figure 22. Completed Assembly Drawing

Cover Glass Specification

1. Scratch and Dig: 20 micron max
2. Substrate Material: Schott S−8612 @ 1 mm Thickness
3. Multilayer Anti-Reflective Coating

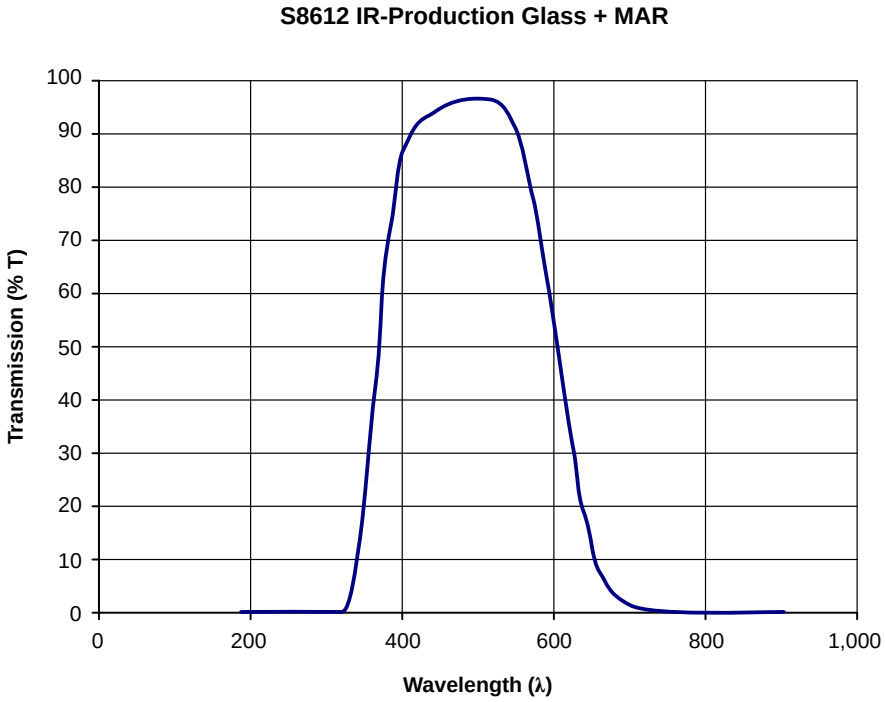


Figure 23. Cover Glass Transmission

REFERENCES

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

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