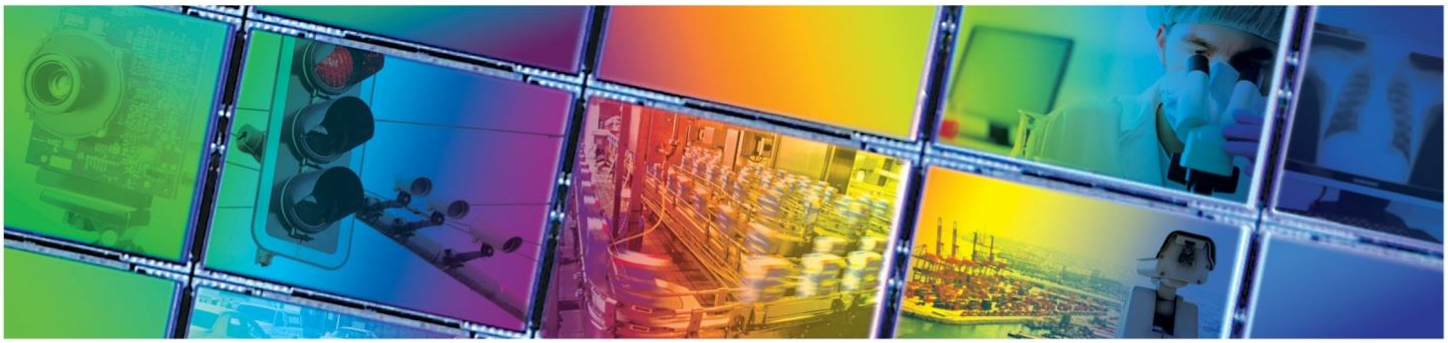
ON Semiconductor®

# KAF-4301 IMAGE SENSOR

## 2084 (H) X 2084 (V) FULL FRAME CCD IMAGE SENSOR



JUNE 18, 2014

## DEVICE PERFORMANCE SPECIFICATION

REVISION 2.1 PS-0038

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# Summary Specification

## KAF-4301 Image Sensor

### DESCRIPTION

The KAF-4301 Image Sensor is a high-density, 4.3 million pixel, full-frame CCD image sensor.

The sensor incorporates true two-phase CCD technology, simplifying the support circuits required to drive the sensor as well as reducing dark current without compromising charge capacity. The sensor also utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.

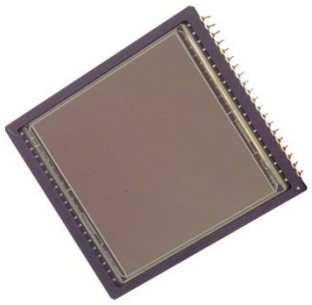
Selectable on-chip output amplifiers allow operation to be optimized for different imaging needs: Low Noise (when using the high-sensitivity output) or Maximum Dynamic Range (when using the low-sensitivity output).

### FEATURES

- True Two Phase Full Frame Architecture
- TRUESENSE Transparent Gate Electrode for high sensitivity
- 100% Fill Factor
- Low Dark Current
- Flexible readout architecture
- User-selectable outputs allow either Low Noise or High Dynamic Range operation.

### APPLICATIONS

- Scientific Imaging



| Parameter | Typical Value |
|---|---|
| Architecture | Full Frame CCD |
| Number of Active Pixels | 2084 (H) x 2084 (V) |
| Pixel Size | 24 µm (H) x 24 µm (V) |
| Active Image Size | 50.0mm (H) x 50.0mm (V) |
| Optical Fill Factor | 100% |
| Output Sensitivity<br>High Sensitivity Output<br>High Dynamic Range Output | <br>11 µV/electron<br>2 µV/electron |
| Saturation Signal<br>High Sensitivity Output<br>High Dynamic Range Output | <br>150,000 electrons<br>650,000 electrons |
| Readout Noise (1 MHz) | 15 electrons rms |
| Dark Current<br>(25 °C, Accumulation Mode) | <30pA/cm$^2$ |
| Dark Current Doubling Rate | 5-6 °C |
| Dynamic Range (Sat Sig/Dark Noise)<br>High Sensitivity Output<br>High Dynamic Range Output | <br>81 dB<br>87 dB |
| Quantum Efficiency (450, 550, 650 nm) | 40%, 55%, 65% |
| Maximum Data Rate<br>High Sensitivity Output<br>High Dynamic Range Output | <br>2.5 MHz<br>2 MHz |
| Transfer Efficiency | >0.99997 |
| Package | PGA Package |
| Cover Glass | Clear |

## Ordering Information

| Catalog Number | Product Name | Description | Marking Code |
|---|---|---|---|
| 4H0791 | KAF- 4301-AAA-JP-B1 | Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass, no coatings, Grade 1 | KAF-4301-AAA S/N |
| 4H0792 | KAF- 4301-AAA-JP-B2 | Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass, no coatings, Grade 2 | |
| 4H0169 | KAF- 4301-AAA-JP-AE | Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass, no coatings, Engineering Sample | |
| 4H0090 | KEK-4H0090-KAF-4301-12-2-5 | Evaluation Board (Complete Kit) | N/A |

See Application Note *Product Naming Convention* for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

Please address all inquiries and purchase orders to:

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E-mail: info@truesenseimaging.com

# Device Description

## ARCHITECTURE

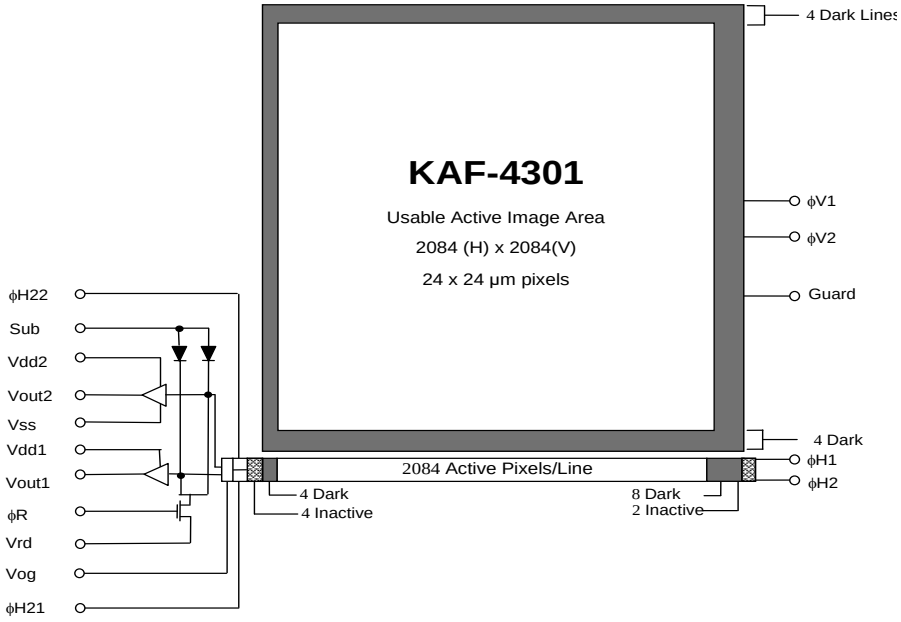



Figure 1: Block Diagram

Shaded areas represent 8 non-imaging pixels at the beginning and 10 non-imaging pixels at the end of each line. There are also 4 non-imaging lines at the top and bottom of each frame.

Refer to the block diagram in Figure 1. The KAF-4301 consists of 2092 vertical (parallel) CCD shift registers, one horizontal (serial) CCD shift register and a selectable high or low gain output amplifier. Both registers incorporate true two-phase buried channel technology. The vertical registers contain 24 µm x 24 µm photocapacitor sensing elements (pixels) that also serves as the transport mechanism. The pixels are arranged in a 2084(H) x 2084(V) array; an additional 8 columns (4 at the left and 4 at the right) and 8 rows (4 each at top and bottom) of non-imaging pixels are added as dark reference. This device must be synchronized with strobe illumination or shuttered during readout because there is no storage array.

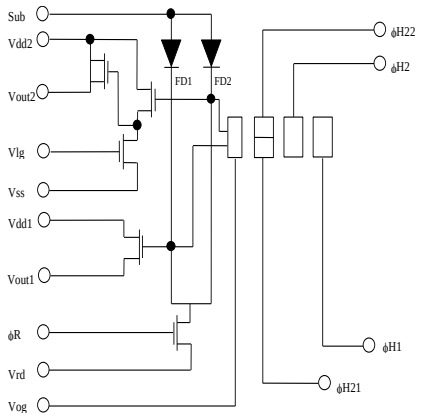



Figure 2: Output Structure

## Output Structure

The final gate of the horizontal register is split into two sections, φH21 and φH22 as shown in Figure 2. The split gate structure allows the user to select either of the two output amplifiers. To use the high dynamic range single-stage output (Vout1), φH22 is tied to a negative voltage to block charge transfer, and φH21 is tied to φH2 to transfer charge. To use the high sensitivity two-stage output (Vout2), φH21 is tied to a negative voltage and φH22 is tied to φH2. The charge packets are then dumped onto the appropriate floating diffusion output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential change is determined by the simple expression Vfd = Q/Cfd. The translation from electrons to voltages is called the output sensitivity or charge-to-voltage conversion. After the output has been sensed off-chip, the reset clock (φR) removes the charge from the floating diffusion via the reset drain (VRD). This, in turn, returns the floating diffusion potential to the reference level determined by the reset drain voltage.

## Image Acquisition

An image is acquired when incident light, in the form of photons, falls on the array of pixels in the vertical CCD register and creates electron-hole pairs (or simply electrons) within the silicon substrate. This charge is collected locally by the formation of potential wells created at each pixel site by induced voltages on the vertical register clock lines (φV1, φV2). These same clock lines are used to implement the transport mechanism as well. The amount of charge collected at each pixel is linearly dependent on light level and exposure time and non-linearly dependent on wavelength until the potential well capacity is exceeded. At this point charge will 'bloom' into vertically adjacent pixels.

## Charge Transport

Integrated charge is transported to the output in a two-step process. Rows of charge are first shifted line by line into the horizontal CCD. 'Lines' of charge are then shifted to the output pixel by pixel. Referring to the timing diagrams in Figure 8, integration of charge is performed with φV1 and φV2 held low. Transfer to the horizontal CCD begins when φV1 is brought high causing charge from the φV1 and φV2 gates to combine under the φV1 gate. φV1 and φV2 now are reversed in polarity causing the charge packets to 'spill' forward under the φV2 gate of the next pixel. The rising edge of φV2 also transfers the first line of charge into the horizontal CCD. A second phase transition places the charge packets under the φV1 electrode of the next pixel. The sequence completes when φV1 is brought low. Clocking of the vertical register in this way is known as accumulation mode clocking. Next, the horizontal CCD transfersout the first line of charge using traditional complementary clocking (using φH1 and φH2 pins) as shown. The falling edge of φH2 forces a charge packet over the output gate (OG) onto one of the output nodes (floating diffusion) that controls the output amplifier. The cycle repeats until all lines are read.

# PHYSICAL DESCRIPTION

## Pin Description and Device Orientation

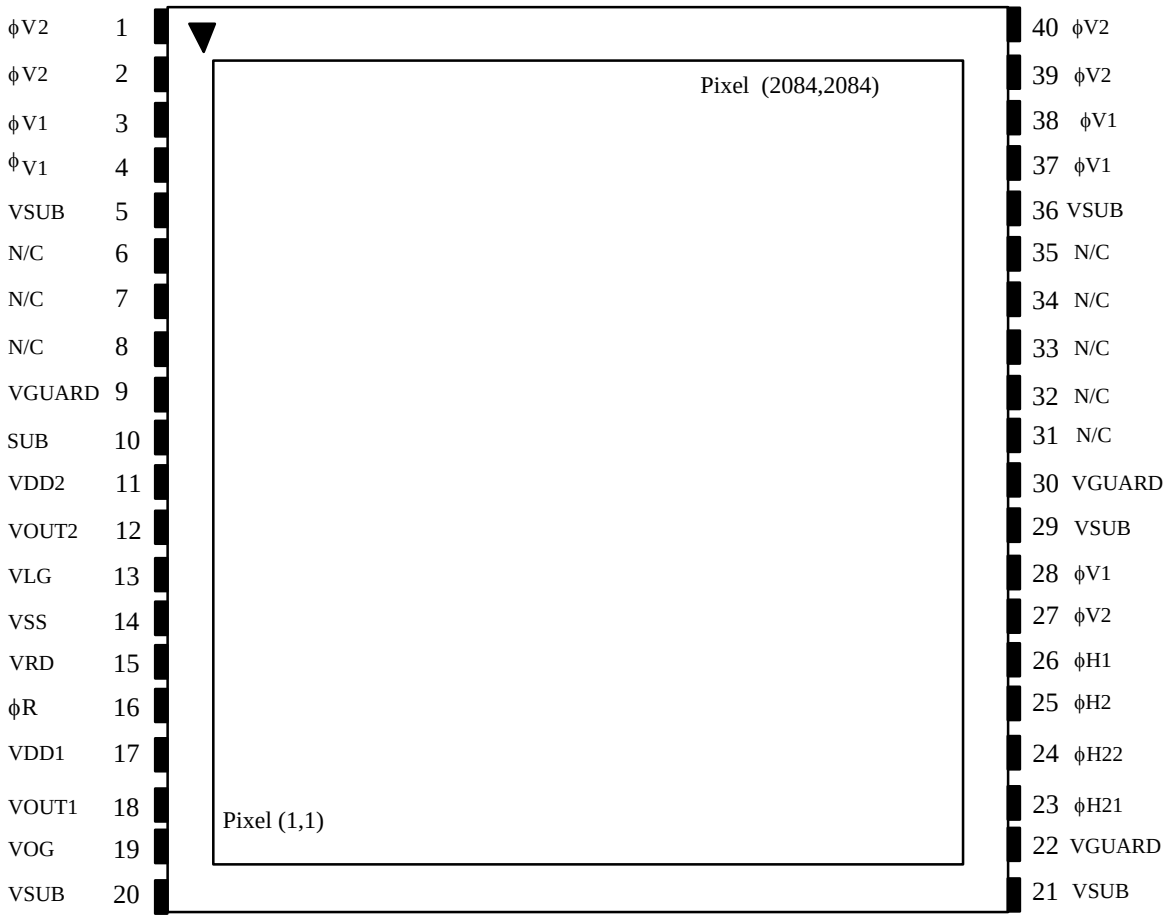



Figure 3: Pinout Diagram

| Pin | Name | Description |
|---|---|---|
| 1 | φV2 | Vertical (Parallel) CCD Clock - Phase 2 |
| 2 | φV2 | Vertical (Parallel) CCD Clock - Phase 2 |
| 3 | φV1 | Vertical (Parallel) CCD Clock - Phase 1 |
| 4 | φV1 | Vertical (Parallel) CCD Clock - Phase 1 |
| 5 | VSUB | Substrate |
| 6 | N/C | No Connection |
| 7 | N/C | No Connection |
| 8 | N/C | No Connection |
| 9 | VGUARD | Guard Ring |
| 10 | VSUB | Substrate |
| 11 | VDD2 | High Sensitivity Two-Stage Amplifier Supply |
| 12 | VOUT2 | Video Output from High Sensitivity Two-Stage Amplifier |
| 13 | VLG | First Stage Load Transistor Gate for Two-Stage Amplifier |
| 14 | VSS | High Sensitivity Two-Stage Amplifier Return |
| 15 | VRD | Reset Drain |
| 16 | φR | Reset Clock |
| 17 | VDD1 | High Dynamic Range Single-Stage Amplifier Supply |
| 18 | VOUT1 | Video Output from High Dynamic Range Single-Stage Amplifier |
| 19 | VOG | Output Gate |
| 20 | VSUB | Substrate |

| Pin | Name | Description |
|---|---|---|
| 40 | φV2 | Vertical (Parallel) CCD Clock - Phase 2 |
| 39 | φV2 | Vertical (Parallel) CCD Clock - Phase 2 |
| 38 | φV1 | Vertical (Parallel) CCD Clock - Phase 1 |
| 37 | φV1 | Vertical (Parallel) CCD Clock - Phase 1 |
| 36 | VSUB | Substrate |
| 35 | N/C | No Connection |
| 34 | N/C | No Connection |
| 33 | N/C | |
| 32 | N/C | |
| 31 | N/C | No Connection |
| 30 | VGUARD | Guard Ring |
| 29 | VSUB | Substrate |
| 28 | φV1 | Vertical (Parallel) CCD Clock - Phase 1 |
| 27 | φV2 | Vertical (Parallel) CCD Clock - Phase 2 |
| 26 | φH1 | Horizontal (Serial) CCD Clock - Phase 2 |
| 25 | φH2 | Horizontal (Serial) CCD Clock - Phase 1 |
| 24 | φH22 | Last Horizontal (Serial) CCD Phase - Split Gate |
| 23 | φH21 | Last Horizontal (Serial) CCD Phase - Split Gate |
| 22 | VGUARD | Guard Ring |
| 21 | VSUB | Substrate |

Notes:

1. Pins 1, 2, 27, 39 and 40 must be connected together - only one Phase 2-clock driver is required.
2. Pins 3, 4, 28, 37 and 38 must be connected together - only one Phase 1-clock driver is required.
3. Pins 5, 10, 20, 21, 29 and 36 should be connected to a common potential.
4. Pins 9, 22 and 30 should be connected to a common potential.

# Imaging Performance

## Typical Operational Conditions

All values derived using nominal operating conditions with the recommended timing. Correlated doubling sampling of the output is assumed and recommended. Many units are expressed in electrons - to convert to a voltage, multiply by the amplifier sensitivity, Vout/$Ne^-$.

## Specifications

### Electro-Optical

| Description | Symbol | Min. | Nom. | Max | Units | Notes | Verification Plan |
|---|---|---|---|---|---|---|---|
| Optical Fill Factor | FF | | 100 | | % | | |
| Photoresponse Non-uniformity | PRNU | | | | % rms | Full Array | die[10] |
| Quantum Efficiency (450, 550, 650 nm) | QE | | | | | SeeFigure 4 | design[11] |

### CCD Parameters Common to Both Outputs

| Description | Symbol | Min. | Nom. | Max. | Units | Notes | Verification Plan |
|---|---|---|---|---|---|---|---|
| Sat. Signal - Vccd register | Ne-sat | 510 | 570 | | $ke^-$ | 2 | design[11] |
| Dark Current | Jd | | 4.2<br>150 | 15<br>540 | $pA/cm^2$<br>$e^-$/pixel/sec | 25 °C<br>(mean of all pixels) | die[10] |
| Dark Current Doubling Temp | DCDR | 5 | 6 | 7 | °C | | design[11] |
| Dark Signal Non-uniformity | DSNU | | | 100 | $e^-$/pix/sec | 4 | die[10] |
| Charge Transfer Efficiency | CTE | | .99999 | | | 5,10 | die[10] |
| Blooming Suppression | Bs | | none | | | | |

### CCD Parameters Specific to High Gain Output Amplifier

| Description | Symbol | Min. | Nom. | Max. | Units | Notes | Verification Plan |
|---|---|---|---|---|---|---|---|
| Output Sensitivity | Vout/$Ne^-$ | 9 | 11.5 | | µV/electron | | design[11] |
| Sat. Signal | $N_{e^-sat}$ | 130 | 150 | 180 | $ke^-$ | 1 | design[11] |
| Total Sensor Noise | $n_{e^-total}$ | | 13 | 20 | $e^-$ rms | 8 | design[11] |
| Horizontal CCD Frequency | $f_H$ | | 1 | 2.5 | MHz | 6 | design[11] |
| Dynamic Range | DR | 79 | 81 | | dB | 9 | design[11] |

### CCD Parameters Specific to Low Gain (High Dynamic Range) Output Amplifier

| Description | Symbol | Min. | Nom. | Max. | Units | Notes | Verification Plan |
|---|---|---|---|---|---|---|---|
| Output Sensitivity | Vout/$Ne^-$ | 1.7 | 2 | | µV/electron | | die[10] |
| Sat. Signal | $N_{e^-sat}$ | 1400 | 1500 | 1800 | $ke^-$ | 3 | design[11] |
| Total Sensor Noise | $n_{e^-total}$ | | 22 | 30 | $e^-$ rms | 8 | die[10] |
| Horizontal CCD Frequency | $f_H$ | | 0.5 | 2 | MHz | 6 | design[11] |
| Dynamic Range | DR | 89 | 87 | | dB | 9 | design[11] |

Notes:

1. Point where the output saturates when operated with nominal voltages.
2. Signal level at the onset of blooming in the vertical (parallel) CCD register.
3. Maximum signal level at the output of the high dynamic range output. This signal level will only be achieved when binning pixels containing large signals.
4. None of 1024 sub arrays (64 x 64) will have an average dark current that exceeds the average of the entire array by this amount. (i.e. no sub array average >Jd+100$e^-$/pix/sec) Measured at room temperature (20 °C to 25 °C).
5. For 2MHz data rate and T = 30 °C to -40 °C.
6. Using maximum CCD frequency and/or minimum CCD transfer times may compromise performance.
7. Time between the rising edge of φV1 and the first falling edge of φH1.
8. At $T_{integration}$ = 0; data rate = 1 MHz; temperature = -30 °C.
9. Uses 20LOG($N_{e^- sat}$ / $n_{e^- total}$) where $N_{e^- sat}$ refers to the appropriate saturation signal,
10. CTE corresponds to a signal level of 3500-5500 $e^-$/pix at 25 °C and φH1, φH2 of 1MHz.
11. A parameter that is measured on every sensor during production testing.
12. A parameter that is quantified during the design verification activity.

## Typical Performance Curves

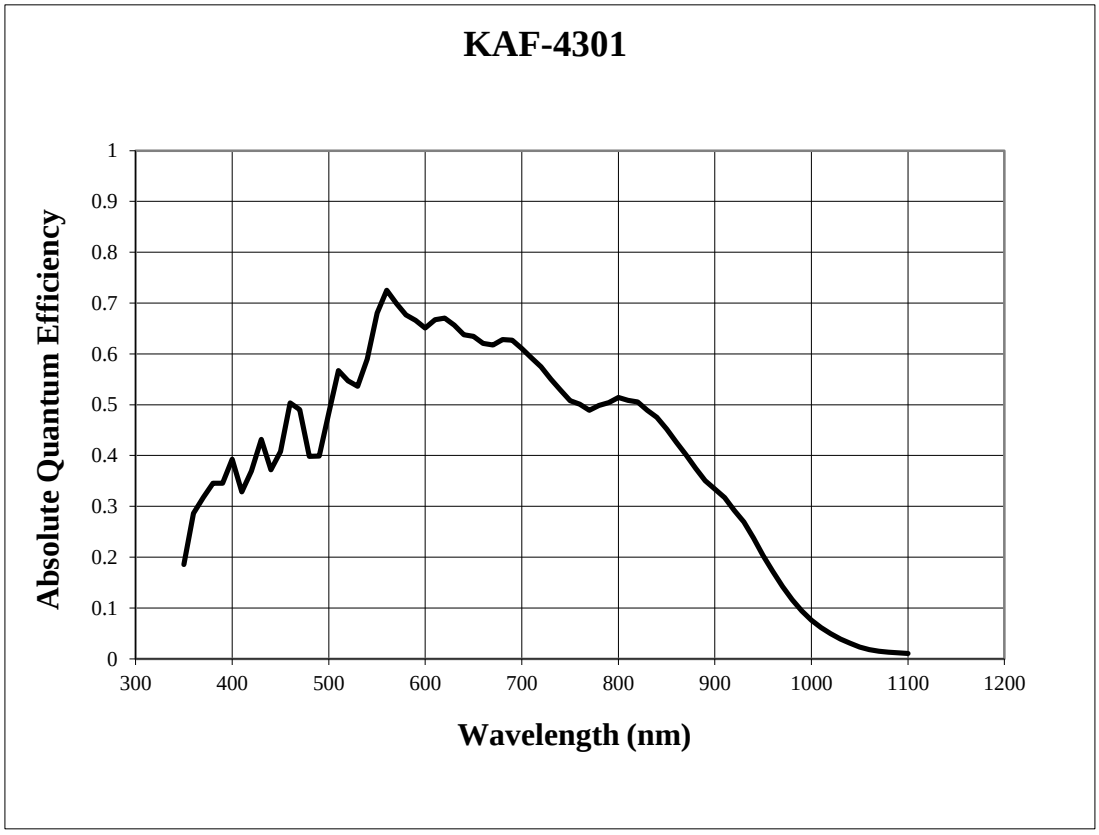



Figure 4: Spectral Response

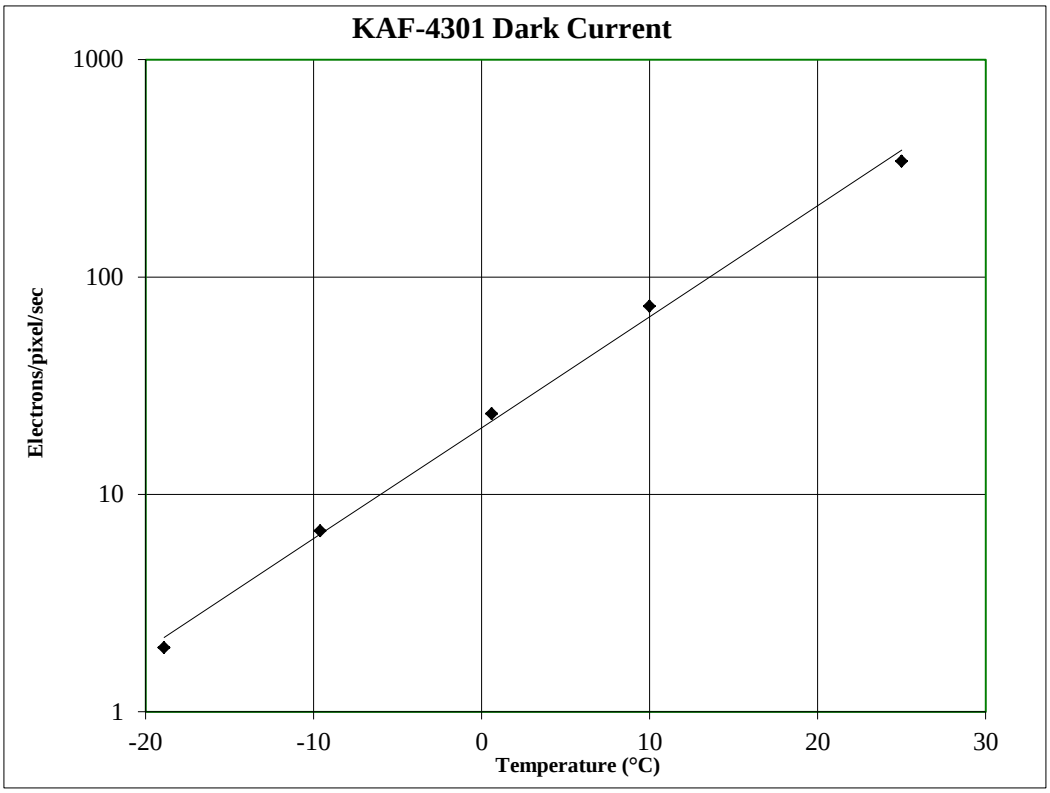



Figure 5: Dark Current

# Defect Definitions

## SPECIFICATIONS

| Classification | Point Defect | Cluster Defect | Column Defect | Double Columns |
|---|---|---|---|---|
| C1 | ≤50 | ≤10 | 2 | 0 |
| C2 | ≤100 | ≤20 | 8 | 0 |

**Dark Defects** A pixel which deviates by more than 20% from neighboring pixels when illuminated to 70% of saturation

**Bright Defect** A pixel whose dark current exceeds 4500 electrons/pixel/second at 25 °C

**Cluster Defect** A grouping of not more than 5 adjacent point defects

**Column Defect** A grouping point defects along a single column. (Dark Column)

A column that contains a pixel whose dark current exceeds 150,000 electrons/pixel/second at 25 °C. (Bright Column)

A column that does not exhibit the minimum charge capacity specification. (Low charge capacity)

A column that loses >500 electrons when the array is illuminated to a signal level of 2000 electrons/pix. (Trap like defects)

**Neighboring Pixels** The surrounding 128 x 128 pixels of ± 64 columns/rows

Cluster defects are separated by no less than 2 pixels from other column and cluster defects.

Column defects are separated by no less than 5 pixels from other column defects.

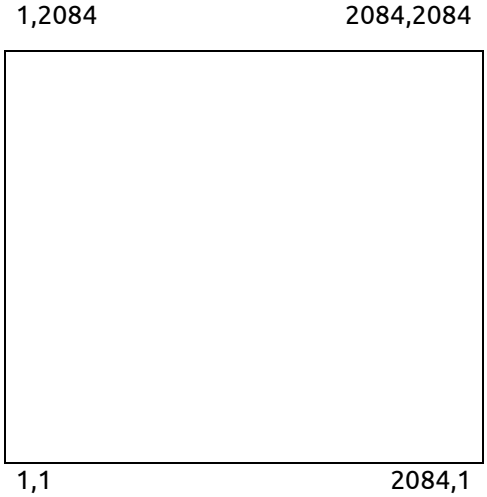



Figure 6: Active Pixel Region

# Operation

## Absolute Maximum Ratings

| Description | Symbol | Minimum | Maximum | Units | Notes |
|---|---|---|---|---|---|
| Voltage | All Clocks | -16 | +16 | V | VSUB = 0V |
| Voltage | VOG, VLG | 0 | +8 | V | VSUB = 0V |
| Voltage | VRD, VSS, VDD, GUARD | 0 | +20 | V | VSUB = 0V |
| Current | Output Bias Current (IDD) | | 10 | mA | |
| Capacitance | Output Load Capacitance (CLOAD) | | 10 | pF | |
| Frequency/Time | φV1, φV2 Pulse Width | 70 | | µs | |
| Frequency/Time | φH1, φH2 | | 2.5 | MHz | |
| Frequency/Time | φR Pulse Width | 20 | | ns | |

Warning:

For maximum performance, built-in gate protection has been added only to the VOG and VLG pin. These devices require extreme care during handling to prevent electrostatic discharge (ESD) induced damage.

## DC Bias Operating Conditions

| Description | Symbol | Minimum | Nominal | Maximum | Units | Pin Impedance |
|---|---|---|---|---|---|---|
| Substrate | VSUB | 0.0 | 0.0 | 0.0 | V | Common |
| Output Amplifier Supply | VDD | 15.0 | +17.0 | 17.5 | V | 5 pf, 2KΩ |
| Output Amplifier Return | VSS | 1.4 | +2.0 | 2.1 | V | 5 pf, 2KΩ |
| Reset Drain | VRD | 11.5 | +12 | 12.5 | V | 5 pf, 1MΩ |
| Output Gate | VOG | 4.5 | 5.0 | 5.25 | V | 5 pf, 10MΩ |
| Guard Ring | VGUARD | 9.0 | +10.0 | 15.0 | V | 350 pF, 10MΩ |
| Load Gate | VLG | Vss-1.0 | Vss | Vss+1.0 | V | |

Notes:

1. An output load sink must be applied to Vout to activate output amplifier - see Figure 7below.
2. For operation of up to 10 MHz.
3. The value of R1 depends on the desired output current according the following formula: R1 = 0.7 / Iout
4. The optimal output current depends on the capacitance that needs to be driven by the amplifier and the bandwidth required. 5 mA is recommended for capacitance of 12 pF and pixel rates up to 20 MHz.

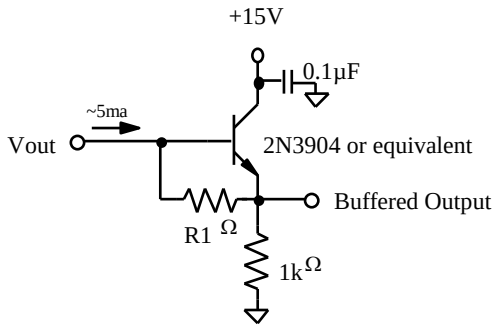



Figure 7: Typical Output Structure Load Diagram

# AC Operating Conditions

## Clock Levels

| Description | Symbol | Level | Minimum | Nominal | Maximum | Units | Pin Impedance |
|---|---|---|---|---|---|---|---|
| Vertical Clock - Phase 1 | φV1 | Low | -8.5 | -8.0 | -7.8 | V | 700 nf, 10MΩ |
| Vertical Clock - Phase 1 | φV1 | High | 1.0 | 1.0 | 2.0 | V | |
| Vertical Clock - Phase 2 | φV2 | Low | -8.5 | -8.0 | -7.8 | V | 800 nf, 10MΩ |
| Vertical Clock - Phase 2 | φV2 | High | 1.0 | 1.0 | 2.0 | V | |
| Horizontal Clock - Phase 1 | φH1 | Low | -2.2 | -2.0 | -1.8 | V | 1200 pf, 10MΩ |
| Horizontal Clock - Phase 1 | φH1 | High | 7.8 | +8.0 | 8.2 | V | |
| Horizontal Clock - Phase 2 | φH2 | Low | -2.2 | -2.0 | -1.8 | V | 1200 pf, 10MΩ |
| Horizontal Clock - Phase 2 | φH2 | High | 7.8 | +8.0 | 8.2 | V | |
| Reset Clock | φR | Low | 2.0 | 3.0 | 3.5 | V | 10 pF, 10MΩ |
| Reset Clock | φR | High | 9.5 | 10.0 | 11.0 | V | |

| | | | Using the High Gain Output (Vout2) | | | Using the High Dynamic Range Output (Vout1) | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Description | Symbol | Level | Min | Nom | Max | Min | Nom | Max | Units | Pin Impedance |
| Horizontal Clock - Phase 1 | φH21 | Low | -4 | φH2 low | φH2 low | | φH2 | | V | 10pF, 10MΩ |
| Horizontal Clock - Phase 1 | φH21 | High | -4 | φH2 low | φH2 low | | φH2 | | V | |
| Horizontal Clock - Phase 2 | φH22 | Low | | φH2 | | -4 | φH2 low | φH2 low | V | 10pF, 10MΩ |
| Horizontal Clock - Phase 2 | φH22 | High | | φH2 | | -4 | φH2 low | φH2 low | V | |

Notes:

1. When using Vout1,φH21 is clocked identically with φH2, while φH22 is held at a static level. When using Vout2,φH21 and φH22 are exchanged, so that φH22 is identical to φH2 and φH21 is held at a static level. The static level should be the same voltage as φH2 low.
2. The AC and DC operating levels are for room temperature operation. Operation at other temperatures may require adjustments of these voltages. Pins shown with impedances greater than 1 MOhm are expected resistances. These pins are only verified to 1 MOhm.
3. φV1, φV2 and φH1, φH2capacitances are accumulated gate oxide capacitance, and so are an over-estimate of the capacitance.
4. This device is suitable for a wide range of applications requiring a variety of different operating conditions. Consult Truesense Imaging in those situations in which operating conditions meet or exceed minimum or maximum levels.

# Timing

## REQUIREMENTS AND CHARACTERISTICS

### AC Timing Chart

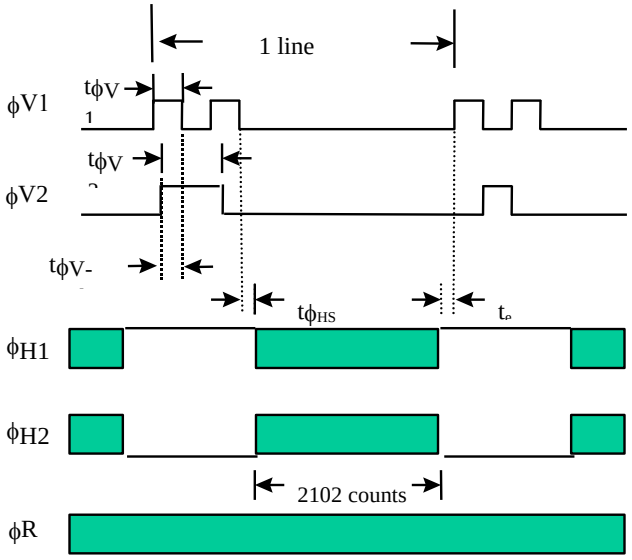
| Description | Symbol | Minimum | Nominal | Maximum | Units | Notes |
|---|---|---|---|---|---|---|
| φH1, φH2 Clock Frequency | $f_H$ | | 1 | 2.5 | MHz | 1, 2, 3 |
| Pixel Period | $t_e$ | 400 | 1000 | | ns | |
| φH1, φH2 Setup Time | $t_{\phi HS}$ | 0.5 | 1 | | µs | |
| φV1 Clock Pulse Width | $t_{\phi V1}$ | | 100 | | µs | 2 |
| φV2 Clock Pulse Width | $t_{\phi V2}$ | | 150 | | µs | 2 |
| φV1, φV2 Clock Pulse Overlap | $t_{\phi V2}$ | | 150 | | µs | 2 |
| φRReset Clock Pulse Width | $t_{\phi R}$ | 20 | 60 | | ns | 4 |
| Readout Time | $t_{readout}$ | 1751 | 5320 | | ms | 5 |

Notes:

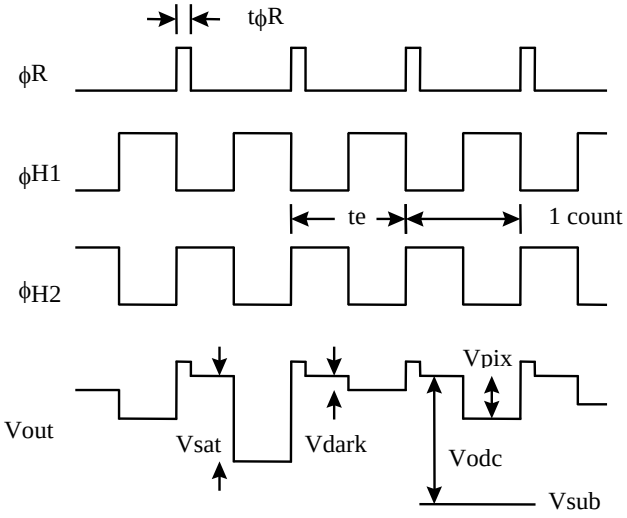
1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5-10% of clock period. Crossover of register clocks should be between 40-60% of amplitude.
4. φR should be clocked continuously.
5. $t_{readout} = (2092 * t_{line})$
6. Integration time ($t_{int}$) is user specified. Longer integration times will degrade noise performance due to dark signal fixed pattern and shot noise.
7. $t_{line} = (3 * t_{\phi V}) + t_{\phi HS} + 2102 * t_e + t_e$

## TIMING DIAGRAMS

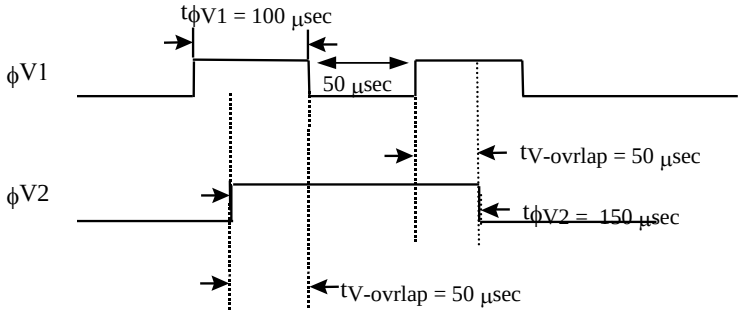
### Line Timing Detail



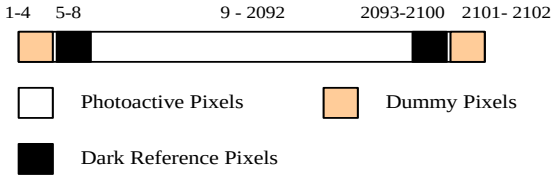

### Pixel Timing Detail




### Vertical Clock Timing Detail




**Line Content**




| | |
|---|---|
| Vsat | Saturated pixel video output signal |
| Vdark | Video output signal in no light situation, not zero due to Jdark |
| Vpix | Pixel video output signal level, more electrons =more negative* |
| Vodc | Video level offset with respect to vsub |
| Vsub | Analog Ground |

* See Image Aquisition section

Figure 8: Timing Diagrams

# Storage and Handling

## Storage Conditions

| Description | Symbol | Minimum | Maximum | Units | Notes |
|---|---|---|---|---|---|
| Storage Temperature | $T_{ST}$ | -100 | +80 | °C | At Device |
| Operating Temperature | $T_{OP}$ | -70 | +50 | °C | At Device |

Notes:
1. Image sensors with temporary cover glass should be stored at room temperature (nominally 25 °C.) in dry nitrogen

## ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

## Cover Glass Care and Cleanliness

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices*.

## Environmental Exposure

1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions*.
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

## Soldering Recommendations

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30W soldering iron. Heat each pin for less than 2 seconds duration.

# Mechanical Information

## COMPLETED ASSEMBLY

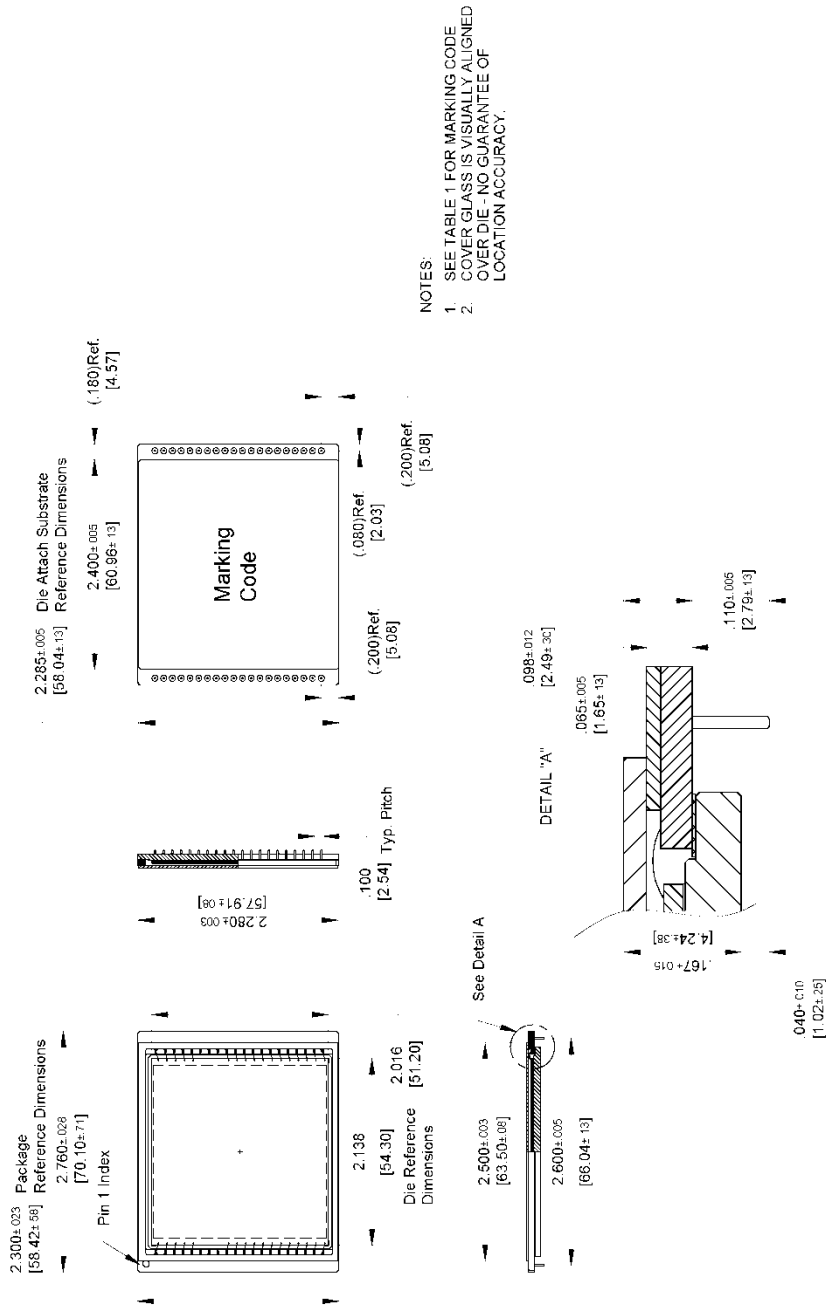



Figure 9: Completed Assembly (1 of 2)

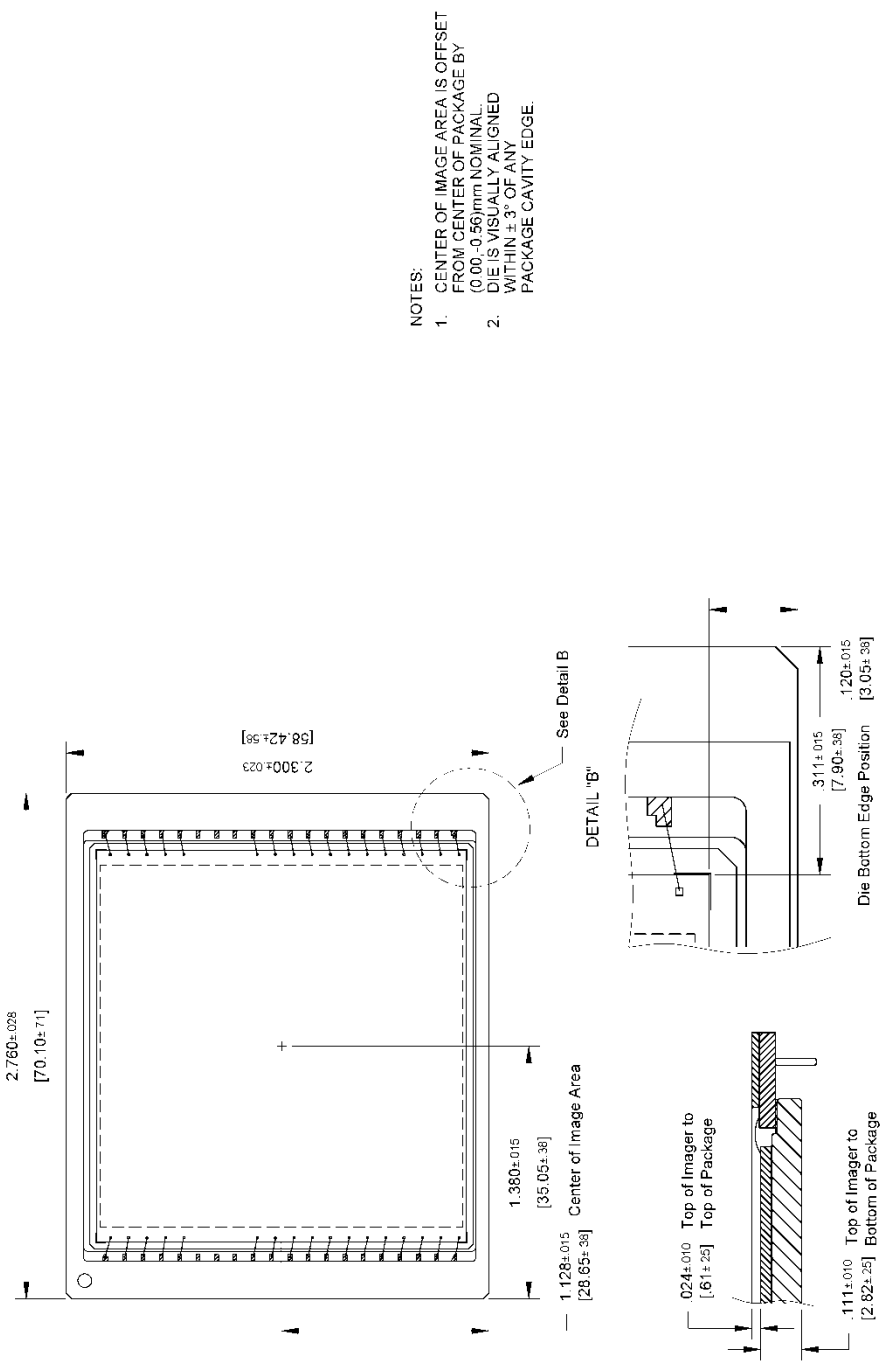



Figure 10: Completed Assembly (2 of 2)

## IMAGER FLATNESS

The flatness of the die is defined as a peak-to-peak distortion in the image sensor surface. The parallelism between the image sensor surface and any of the package components is not specified or guaranteed. The non-parallelism is removed when measuring the distortion in the image sensor surface.

| | | Minimum | Nominal | Maximum | Units |
|---|---|---|---|---|---|
| Die Flatness | Peak-to-Peak distortion | - | 8.0 | 12.0 | microns |

Some examples of profiles from typical image sensors surfaces are shown below.

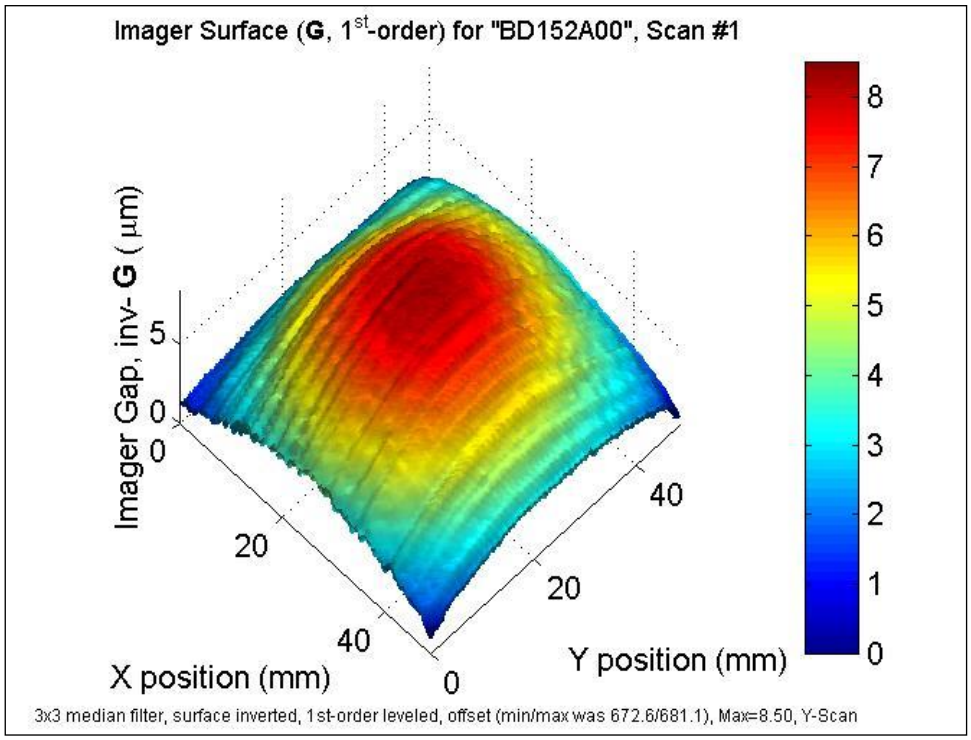



Figure 11: Surface Profile of Image Sensor Surface

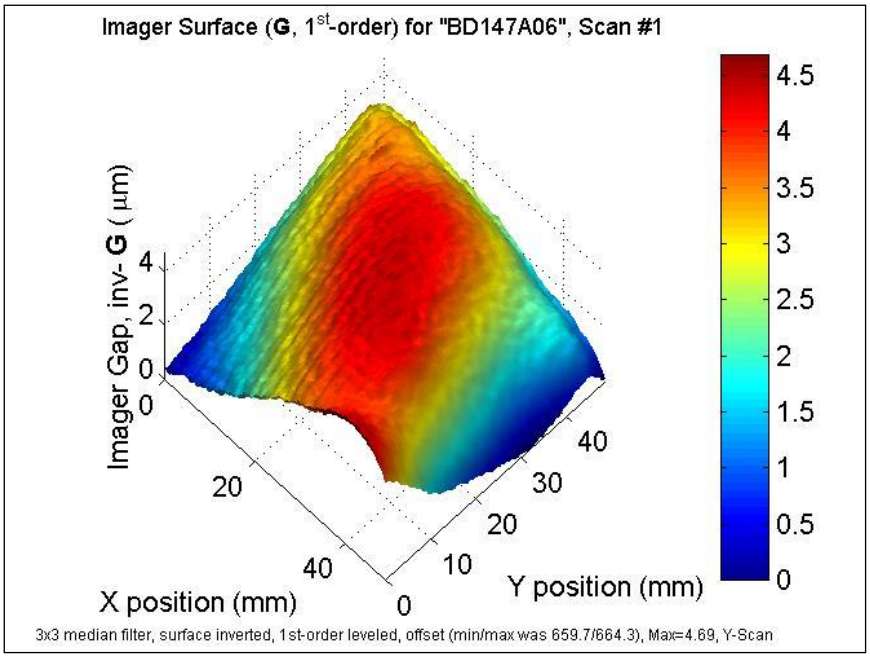



Figure 12: Surface Profile of Image Sensor Surface

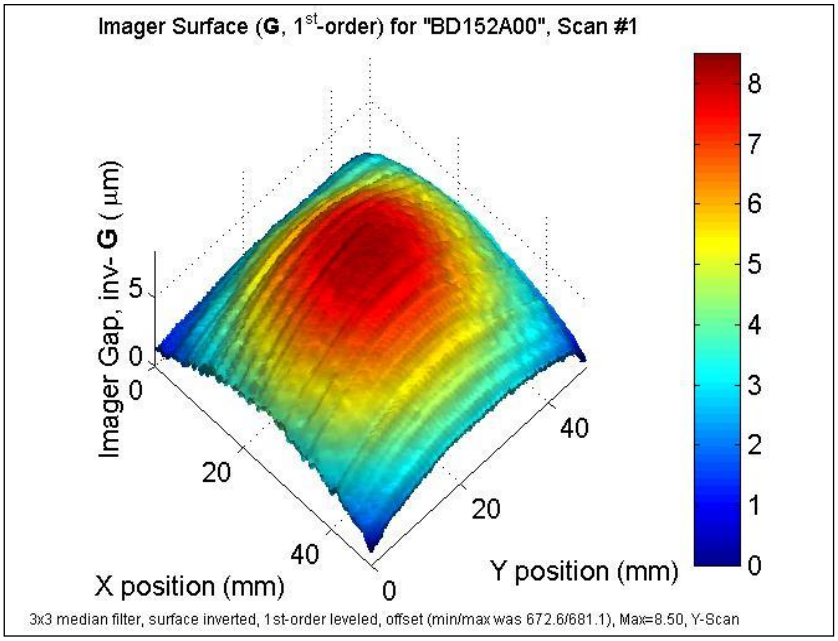



Figure 13: Surface Profile of Image Sensor Surface

# Quality Assurance and Reliability

## Quality and Reliability

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

## Replacement

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

## Liability of the Supplier

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

## Liability of the Customer

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

## Test Data Retention

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

## Mechanical

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

# Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.

# Revision Changes

## MTD/PS-0339

| Revision Number | Description of Changes |
|---|---|
| 1.0 | • Initial Release |
| 2.0 | • Added Section 6.1 Imager Flatness |
| 3.0 | • Section 2.2.1:<br>  ○ Revised DSNU maximum value and revised Note 4.<br>  ○ Eliminated TVH parameter.<br>• Section 2.3:<br>  ○ Revised Class 1 and 2 allowable points, clusters and column defects.<br>  ○ Eliminated Classes 3 and 4.<br>• Section 5.5:<br>  ○ Revised cleanliness statement. |
| 4.0 | • Update specification format<br>• Updated Completed Assembly Drawing |

## PS-0038

| Revision Number | Description of Changes |
|---|---|
| 1.0 | • Initial release with new document number, updated branding and document template<br>• Updated *Storage and Handling* and *Quality Assurance and Reliability* sections<br>• Corrected High Sensitivity Output Saturation Signal value shown in Summary Specification to be consistent with Imaging Performance table |
| 2.0 | • Updated descriptions on Ordering Information page |
| 2.1 | • Updated branding |



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