



SANYO Semiconductors

## DATA SHEET

# LA6324N

# LA6324NM

Monolithic Linear IC  
High-Performance  
Quad Operational Amplifier

## Overview

The LA6324 consists of four independent, high-performance, internally phase compensated operational amplifiers that are designed to operate from a single power supply over a wide range of voltages. These four operational amplifiers are packaged in a single package. As in case of conventional general-purpose operational amplifiers, operation from dual power supplies is also possible and the power dissipation is low. It can be applied to various uses in commercial and industrial equipment including all types of transducer amplifiers and DC amplifiers.

## Features

- No phase compensation required
- Wide operating voltage range:  
3.0 V to 30.0 V (single supply)  
 $\pm 1.5$  V to  $\pm 15.0$  V (dual supplies)
- Highly resistant to dielectric breakdown
- Input voltage range includes the neighborhood of GND level and output voltage range  $V_{OUT}$  is from 0 to  $V_{CC} - 1.5$  V.
- Small current dissipation:

$$I_{CC} = 0.6 \text{ mA typ}/V_{CC} = +5 \text{ V}, R_L = \infty$$

## Specifications

**Absolute Maximum Ratings** at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum Supply voltage	$V_{CC \text{ max}}$		32	V
Differential input voltage	$V_{ID}$		32	V
Maximum input voltage	$V_{IN \text{ max}}$		-0.3 to +32	V
Allowable power dissipation	$P_d \text{ max}$	LA6324N	720	mW
		LA6324NM	330	mW
Operating temperature	$T_{opr}$		-30 to +85	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +125	$^\circ\text{C}$

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**SANYO Semiconductor Co., Ltd.**

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# LA6324N,6324NM

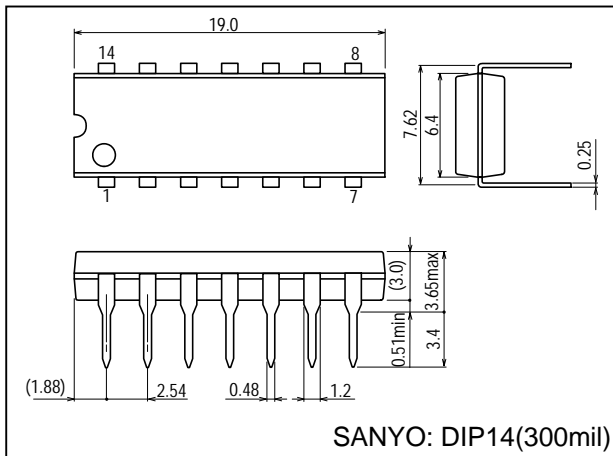
Operating Characteristics at  $T_a = 25\text{ }^\circ\text{C}$ ,  $V_{CC} = +5\text{ V}$

Parameter	Symbol	Conditions	Test circuit	Ratings			Unit
				min	typ	max	
Input offset voltage	$V_{IO}$		1		$\pm 2$	$\pm 7$	mV
Input offset current	$I_{IO}$	$I_{IN(+)} / I_{IN(-)}$	2		$\pm 5$	$\pm 50$	nA
Input bias current	$I_B$	$I_{IN(+)} / I_{IN(-)}$	3		45	250	nA
Common-mode input voltage range	$V_{ICM}$		4	0		$V_{CC} - 1.5$	V
Common-mode rejection ratio	CMR		4	65	80		dB
Voltage gain	VG	$V_{CC} = 15\text{ V}$ , $R_L \geq 2\text{ k}\Omega$	5	25	100		V/mV
Output voltage range	$V_{OUT}$			0		$V_{CC} - 1.5$	V
Supply voltage rejection ratio	SVR		6	65	100		dB
Channel separation	CS	$f = 1\text{ k}$ to $20\text{ kHz}$	7		120		dB
Current drain	$I_{CC}$		8		0.6	2	mA
	$I_{CC}$	$V_{CC} = 30\text{ V}$	8		1.5	3	mA
Output current (Source)	$I_{O\text{ source}}$	$V_{IN+} = 1\text{ V}$ , $V_{IN-} = 0\text{ V}$	9	20	40		mA
Output current (Sink)	$I_{O\text{ sink}}$	$V_{IN+} = 0\text{ V}$ , $V_{IN-} = 1\text{ V}$	10	10	20		mA

## Package Dimensions

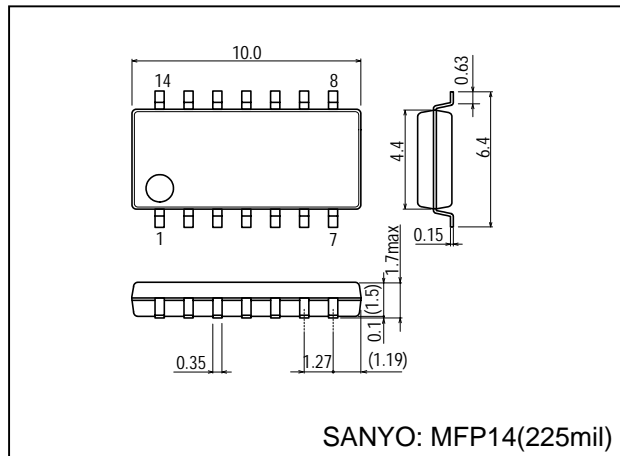
unit : mm

3003B [LA6324N]



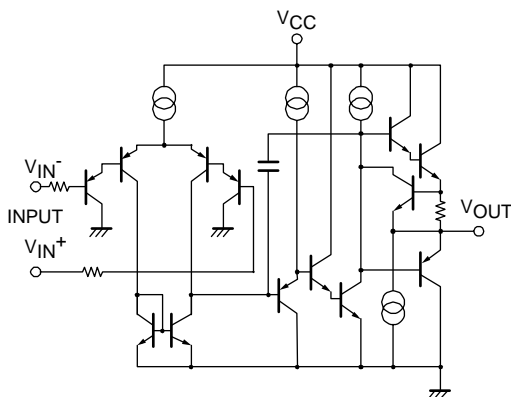
unit : mm

3034B [LA6324NM]



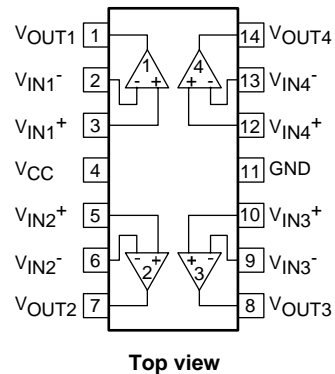
## Equivalent Circuit

(1 unit)



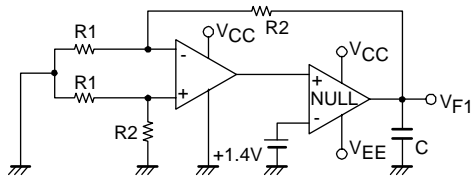
## Pin Assignment

(LA6324N, 6324NM)



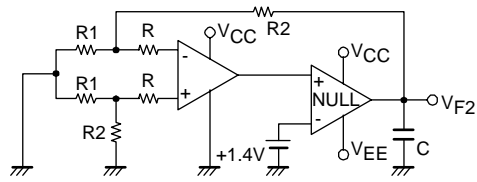
**Test Circuit**

1. Input offset voltage  $V_{IO}$



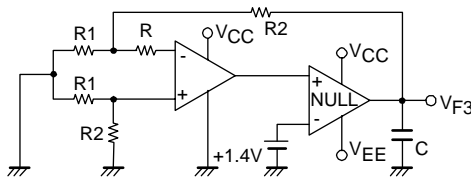
$$V_{IO} = \frac{V_{F1}}{1+R2/R1}$$

2. Input offset current  $I_{IO}$

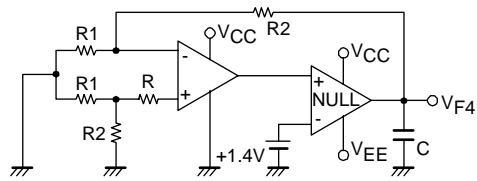


$$I_{IO} = \frac{V_{F2} - V_{F1}}{R(1+R2/R1)}$$

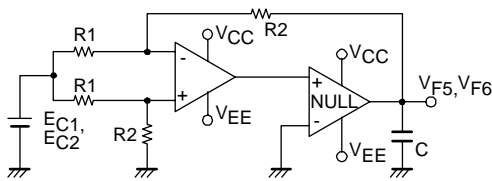
3. Input bias current  $I_B$



$$I_B = \frac{V_{F4} - V_{F3}}{2R(1+R2/R1)}$$

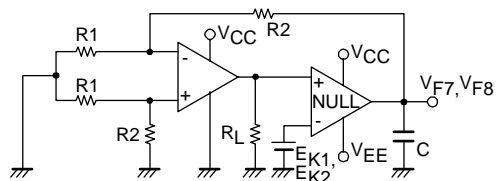


4. Common-mode rejection ratio CMR  
Common-mode input voltage range  $V_{ICM}$



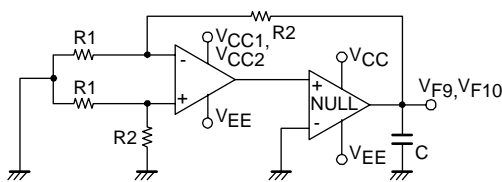
$$CMR = 20 \log \left| \frac{(E_{C1} - E_{C2})(1+R2/R1)}{V_{F5} - V_{F6}} \right|$$

5. Voltage gain  $V_G$

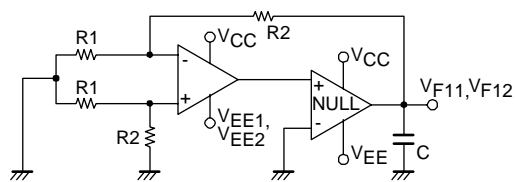


$$V_G = \frac{(E_{K1} - E_{K2})(1+R2/R1)}{V_{F8} - V_{F7}}$$

6. Supply voltage rejection ratio SVR

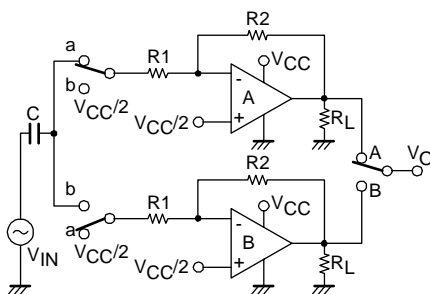


$$SVR (+) = 20 \log \left| \frac{(1+R2/R1)(V_{CC1} - V_{CC2})}{V_{F9} - V_{F10}} \right|$$



$$SVR (-) = 20 \log \left| \frac{(1+R2/R1)(V_{EE1} - V_{EE2})}{V_{F11} - V_{F12}} \right|$$

7. Channel separation CS



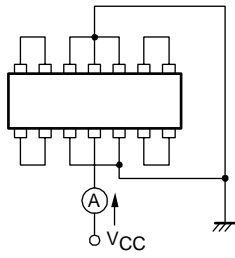
SW: a  
CS (A→B) = 20 log  $\frac{R2 V_{OA}}{R1 V_{OB}}$

SW: b  
CS (B→A) = 20 log  $\frac{R2 V_{OB}}{R1 V_{OA}}$

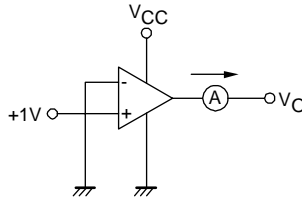
These apply also to other channels.

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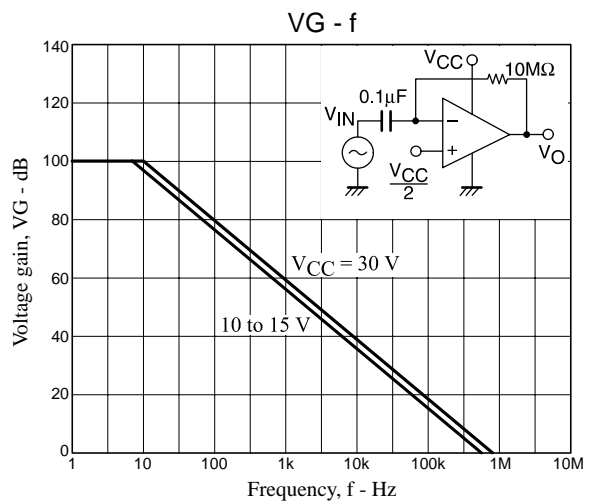
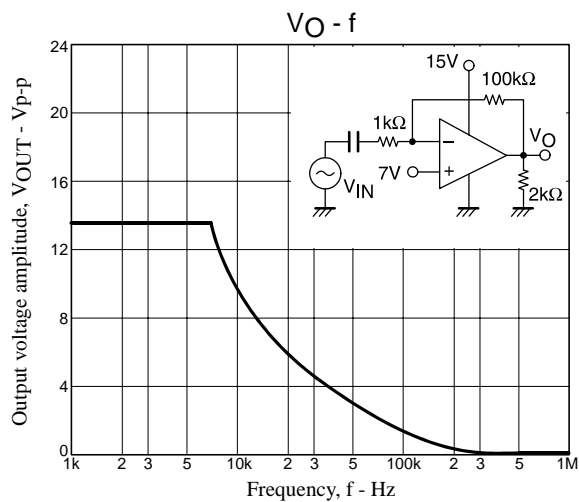
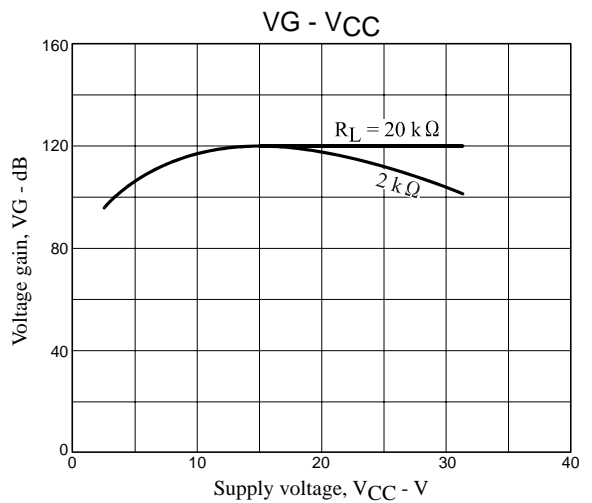
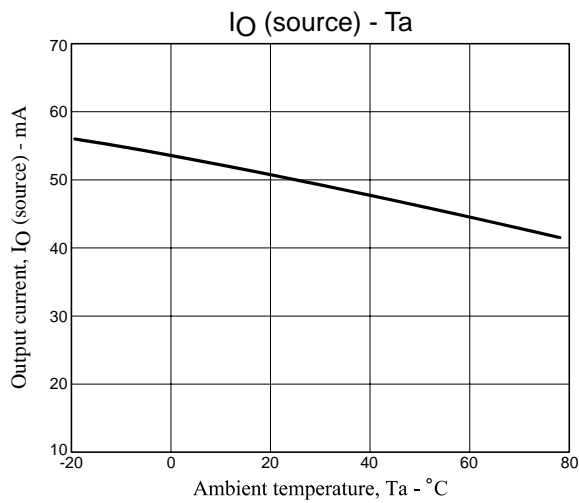
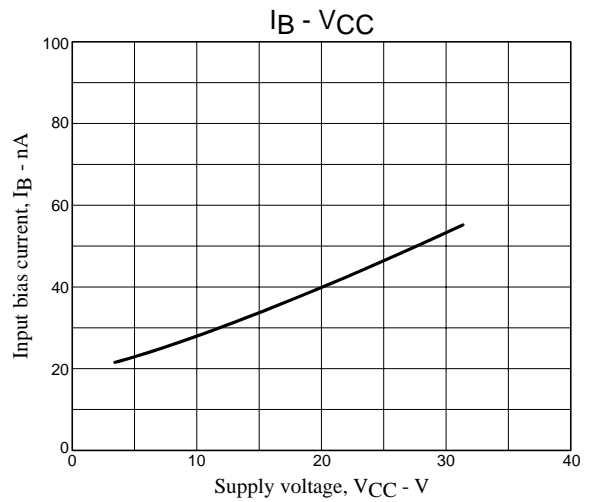
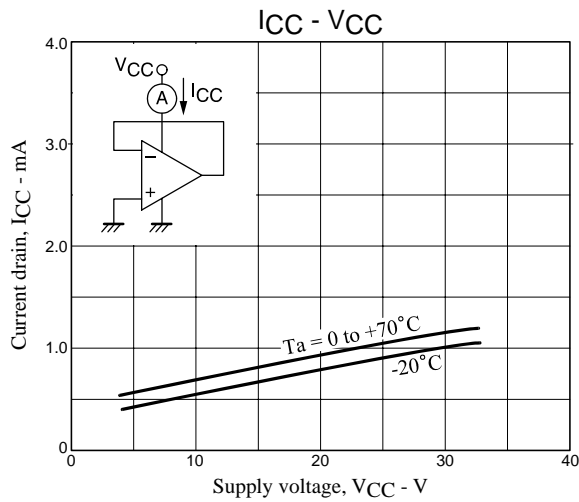
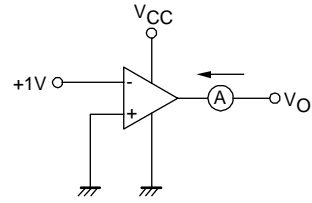
## 8. Current drain $I_{CC}$



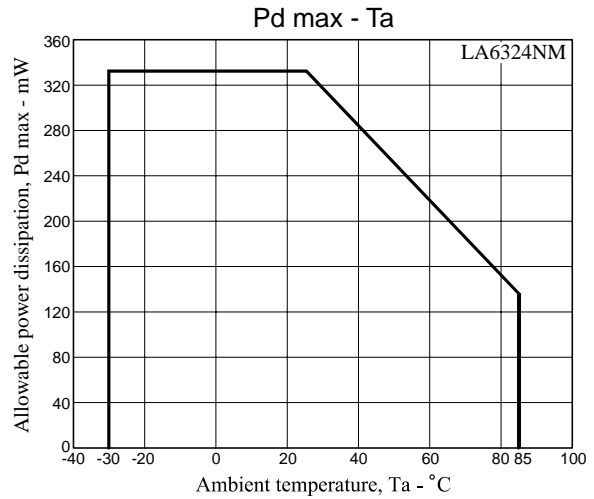
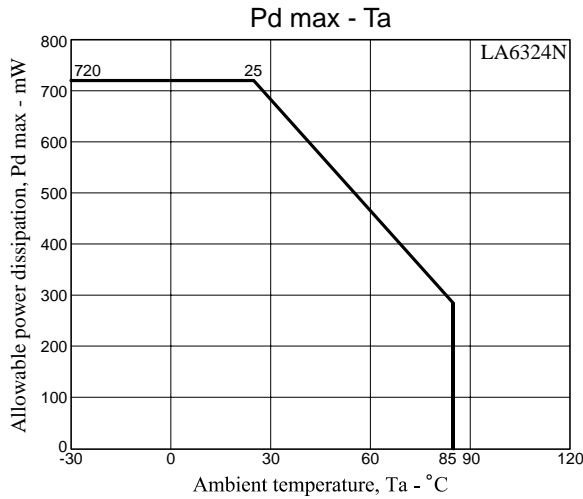
## 9. Output current $I_O$ source



## 10. Output current $I_O$ sink

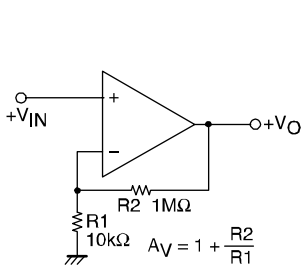


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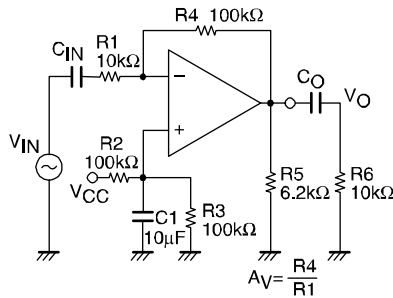


## Sample Application Circuits

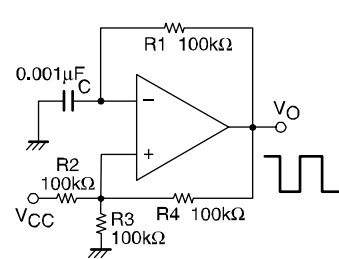
Noninverting DC amplifier



Rectangular wave oscillator



Inverting AC amplifier



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