LB11923V

Three-Phase Brushless Motor Driver

Monolithic Digital IC

ON Semiconductor®

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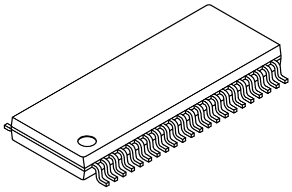
Overview

The LB11923V is a pre-driver IC designed for variable-speed control of 3-phase brushless motors. It can be used to implement a motor drive circuit with the desired output capacity (voltage, current) by using discrete transistors for the output stage. It implements direct PWM drive for minimal power loss. Since the LB11923V includes a built-in VCO circuit, applications can control the motor speed arbitrarily by varying the external clock frequency.

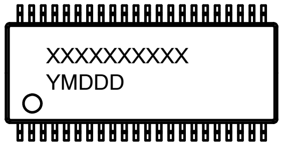
Features

- Direct PWM Drive Output
- Speed Discriminator + PLL Speed Control Circuit
- Speed Lock Detection Output
- Built-in Crystal Oscillator Circuit
- Forward/Reverse Switching Circuit
- Braking Circuit (Short Braking)
- Full Complement of On-chip Protection Circuits, Including Lock Protection, Current Limiter, and Thermal Shutdown Protection Circuits



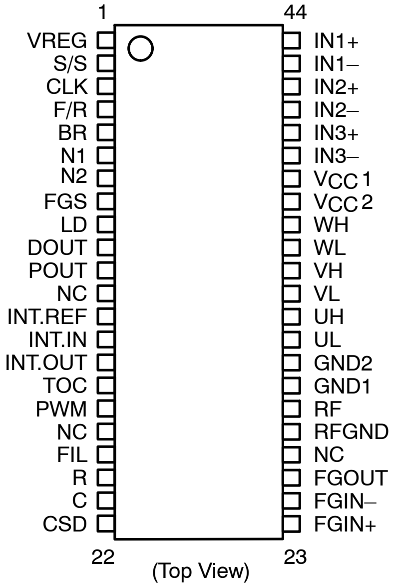
SSOP44
CASE 565AW

MARKING DIAGRAM



XXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 20 of this data sheet.

December, 2018 − Rev. 2

Publication Order Number:
LB11923V/D

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC} max	Maximum Supply Voltage		8	V
I_{REG} max	Maximum Input Current	V_{REG} pin	2	mA
I_O max	Output Current	UH, VH, WH, UL, VL, and WL outputs	30	mA
P_d max1	Allowable Power Dissipation 1	Independent IC	0.62	W
P_d max2	Allowable Power Dissipation 2	When mounted on the specified PCB (Note 1)	1.79	W
T_{opr}	Operating Temperature		–20 to +80	°C
T_{stg}	Storage Temperature		–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Specified PCB: 114.3 × 76.1 × 1.6 mm glass epoxy PCB

ALLOWABLE OPERATING RANGES (T_A = 25°C)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply Voltage		4.4 to 7.0	V
I_{REG}	Input Current Range	V_{REG} pin (7 V)	0.2 to 1.5	mA
V_{FGS}	FG Schmitt Output Applied Voltage		0 to 7	V
I_{FGS}	FG Schmitt Output Current		0 to 5	mA
V_{LD}	Lock Detection Applied Voltage		0 to 7	V
I_{LD}	Lock Detection Output Current		0 to 20	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 6.3 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{CC}1$	Supply Current		–	21	29.5	mA
$I_{CC}2$		In stop mode	–	2.3	3.3	mA
$I_{CC}3$		V_{CC} = 5 V	–	20	28	mA
$I_{CC}4$		V_{CC} = 5 V, In stop mode	–	2.1	2.9	mA
V_O sat1–1	Output Saturation Voltage 1–1	At low level: I_O = 400 μA	–	0.1	0.3	V
V_O sat1–2	Output Saturation Voltage 1–2	At low level: I_O = 10 mA	–	0.8	1.2	V
V_O sat2	Output Saturation Voltage 2	At high level: I_O = –20 mA	V_{CC} – 1.2	V_{CC} – 0.9	–	V

[Hall Amplifier]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{HB(HA)}$	Input Bias Current		–2	–0.1	–	μA
$V_{ICM}1$	Common-mode Input Voltage Range 1	When Hall-effect sensors are used	0.5	–	V_{CC} – 2.0	V
$V_{ICM}2$	Common-mode Input Voltage Range 2	When one-side biased inputs are used (Hall-effect IC applications)	0	–	V_{CC}	V
	Hall Input Sensitivity	Sine wave	100	–	–	mVp–p
$\Delta V_{IN(HA)}$	Hysteresis		25	35	52	mV

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 6.3 V) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
[Hall Amplifier]						
V_{SLH}	Input Voltage Low → High		9	17	29	mV
V_{SHL}	Input Voltage High → Low		–29	–18	–9	mV
[PWM Oscillator]						
$V_{OH(PWM)}1$	Output High-level Voltage 1		3.5	3.8	4.1	V
$V_{OH(PWM)}2$	Output High-level Voltage 2	V_{CC} = 5 V	2.75	3.0	3.25	V
$V_{OL(PWM)}1$	Output Low-level Voltage 1		1.8	2.1	2.4	V
$V_{OL(PWM)}2$	Output Low-level Voltage 2	V_{CC} = 5 V	1.45	1.65	1.9	V
$f_{(PWM)}$	Oscillator Frequency	C = 560 pF	–	22	–	kHz
$V_{(PWM)}1$	Amplitude 1		1.4	1.7	2.0	Vp–p
$V_{(PWM)}2$	Amplitude 2	V_{cc} = 5 V	1.1	1.35	1.6	Vp–p
[CSD Oscillator]						
$V_{OH(CSD)}1$	Output High-level Voltage 1		3.95	4.4	4.85	V
$V_{OH(CSD)}2$	Output High-level Voltage 2	V_{CC} = 5 V	3.15	3.5	3.85	V
$V_{OL(CSD)}1$	Output Low-level Voltage 1		1.1	1.4	1.7	V
$V_{OL(CSD)}2$	Output Low-level Voltage 2	V_{CC} = 5 V	0.9	1.1	1.3	V
$I_{CHG}1$	External Capacitor Charge Current		–13	–9	–6	μA
$I_{CHG}2$	External Capacitor Discharge Current		8	12	16	μA
$f_{(RK)}$	Oscillator Frequency	C = 0.068 μF	–	22	–	Hz
$V_{(RK)}1$	Amplitude 1		2.65	3.0	3.35	Vp–p
$V_{(RK)}2$	Amplitude 2	V_{CC} = 5 V	2.1	2.4	2.65	Vp–p
[VCO Oscillator C pin]						
$V_{OH(C)}1$	Output High-level Voltage 1		2.10	2.40	2.65	V
$V_{OH(C)}2$	Output High-level Voltage 2	V_{CC} = 5 V	2.00	2.30	2.55	V
$V_{OL(C)}1$	Output Low-level Voltage 1		1.60	1.90	2.10	V
$V_{OL(C)}2$	Output Low-level Voltage 2	V_{CC} = 5 V	1.55	1.80	2.05	V
$f_{(C)}$	Oscillator Frequency		–	–	1.0	MHz
$V_{(C)}1$	Amplitude 1		0.3	0.5	0.7	Vp–p
$V_{(C)}2$	Amplitude 2	V_{CC} = 5 V	0.3	0.5	0.7	Vp–p
[Current Limiter Operation]						
V_{RF}	Limiter		0.235	0.260	0.285	V
[Thermal Shutdown Operation]						
TTSD	Thermal Shutdown Operating Temperature	Design target value (Note 2)	150	180	–	°C
ΔTSD	Hysteresis	Design target value (Note 2)	–	30	–	°C
[V_{REG} Pin]						
V_{REG}	V_{REG} Pin Voltage	I = 500 μA	6.6	7.0	7.4	V

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 6.3 V) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
[Low-voltage Protection Circuit]						
V_{SDL}	Operating Voltage		3.55	3.75	4.00	V
V_{SDH}	Release Voltage		3.85	4.03	4.25	V
ΔVSD	Hysteresis		0.18	0.28	0.38	V
[FG Amplifier]						
$V_{IO(FG)}$	Input Offset Voltage		–10	–	+10	mV
$I_{B(FG)}$	Input Bias Current		–1	–	+1	μA
$V_{OH(FG)}1$	Output High-level Voltage 1	IFGI = –0.1 mA, No load	4.2	4.6	5.0	V
$V_{OH(FG)}2$	Output High-level Voltage 2	IFGI = –0.1 mA, No load, V_{CC} = 5 V	3.6	3.95	4.3	V
$V_{OL(FG)}1$	Output Low-level Voltage 1	IFGI = 0.1 mA, No load	1.3	1.7	2.1	V
$V_{OL(FG)}2$	Output Low-level Voltage 2	IFGI = 0.1 mA, No load, V_{CC} = 5 V	0.7	1.05	1.4	V
	FG Input Sensitivity	Gain: 100×	3	–	–	mV
	Schmitt Amplitude for the Next Stage		100	180	250	mV
	Operating Frequency Range		–	–	4	kHz
	Open-loop Gain	$f_{(FG)}$ = 2 kHz	45	51	–	dB
$V_{B(FG)}$	Reference Voltage		–5%	$V_{CC}/2$	5%	V
[FGS Output]						
$V_{O(FGS)}$	Output Saturation Voltage	$I_{O(FGS)}$ = 2 mA	–	0.2	0.4	V
$I_{L(FGS)}$	Output Leakage Current	$V_O = V_{CC}$	–	–	10	μA
[Speed Discriminator Output]						
$V_{OH(D)}$	Output High-level Voltage		V_{CC} – 1.0	V_{CC} – 0.7	–	V
$V_{OL(D)}$	Output Low-level Voltage		–	0.8	1.1	V
[Speed Control PLL Output]						
$V_{OH(P)}1$	Output High-level Voltage		4.05	4.30	4.65	V
$V_{OH(P)}2$		V_{CC} = 5 V	3.25	3.50	3.85	V
$V_{OL(P)}1$	Output Low-level Voltage		1.85	2.15	2.45	V
$V_{OL(P)}2$		V_{CC} = 5 V	1.25	1.60	1.85	V
[Lock Detection]						
$V_{OL(LD)}$	Output Saturation Voltage	I_{LD} = 10 mA	–	0.25	0.4	V
$I_{L(LD)}$	Output Leakage Current	$V_O = V_{CC}$	–	–	10	μA
	Lock Range		–6.25	–	+6.25	%
[Integrator]						
$V_{IO(INT)}$	Input Offset Voltage		–10	–	+10	mV
$I_{B(INT)}$	Input Bias Current		–0.4	–	+0.4	μA
$V_{OH(INT)}1$	Output High-level Voltage 1	IINTI = –0.1 mA, No load	4.1	4.4	4.7	V
$V_{OH(INT)}2$	Output High-level Voltage 2	IINTI = –0.1 mA, No load, V_{CC} = 5 V	3.45	3.7	3.95	V

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 6.3 V) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
[Integrator]						
$V_{OL(INT)}1$	Output Low-level Voltage 1	IINTI = 0.1 mA, No load	1.2	1.4	1.65	V
$V_{OL(INT)}2$	Output Low-level Voltage 2	IINTI = 0.1 mA, No load, V_{CC} = 5 V	1.1	1.3	1.5	V
	Open-loop Gain		45	51	–	dB
	Gain-bandwidth Product	Design target value (Note 2)	–	1.0	–	MHz
$V_{B(INT)}$	Reference Voltage		–5%	$V_{CC}/2$	5%	V
[FIL Output]						
$I_{OH(FIL)}$	Output Source Current		–17	–13	–7	μA
$I_{OL(FIL)}$	Output Sink Current		7	12	17	μA
[S/S Pin]						
$V_{IH(S/S)}$	Input High-level Voltage	V_{CC} = 6.3 V, 5 V	2.0	–	V_{CC}	V
$V_{IL(S/S)}$	Input Low-level Voltage	V_{CC} = 6.3 V, 5 V	0	–	1.0	V
$V_{IO(S/S)}$	Input Open Voltage		$V_{CC} - 0.5$	–	V_{CC}	V
$\Delta V_{IN(S/S)}$	Hysteresis	V_{CC} = 6.3 V, 5 V	0.13	0.22	0.31	V
$I_{IH(S/S)}$	Input High-level Current	$V_{S/S} = V_{CC}$	–10	0	+10	μA
$I_{IL(S/S)}$	Input Low-level Current	$V_{S/S}$ = 0 V	–170	–118	–	μA
$R_{U(S/S)}$	Pull-up Resistance		37	53.5	70	kΩ
[F/R Pin]						
$V_{IH(F/R)}$	Input High-level Voltage	V_{CC} = 6.3 V, 5 V	2.0	–	V_{CC}	V
$V_{IL(F/R)}$	Input Low-level Voltage	V_{CC} = 6.3 V, 5 V	0	–	1.0	V
$V_{IO(F/R)}$	Input Open Voltage		$V_{CC} - 0.5$	–	V_{CC}	V
$\Delta V_{IN(F/R)}$	Hysteresis	V_{CC} = 6.3 V, 5 V	0.13	0.22	0.31	V
$I_{IH(F/R)}$	Input High-level Current	$V_{F/R} = V_{CC}$	–10	0	+10	μA
$I_{IL(F/R)}$	Input Low-level Current	$V_{F/R}$ = 0 V	–170	–118	–	μA
$R_{U(F/R)}$	Pull-up resistance		37	53.5	70	kΩ
[BR Pin]						
$V_{IH(BR)}$	Input High-level Voltage	V_{CC} = 6.3 V, 5 V	2.0	–	V_{CC}	V
$V_{IL(BR)}$	Input Low-level Voltage	V_{CC} = 6.3 V, 5 V	0	–	1.0	V
$V_{IO(BR)}$	Input Open Voltage		$V_{CC} - 0.5$	–	V_{CC}	V
$\Delta V_{IN(BR)}$	Hysteresis	V_{CC} = 6.3 V, 5 V	0.13	0.22	0.31	V
$I_{IH(BR)}$	Input High-level Current	$V_{BR} = V_{CC}$	–10	0	+10	μA
$I_{IL(BR)}$	Input Low-level Current	V_{BR} = 0 V	–170	–118	–	μA
$R_{U(BR)}$	Pull-up Resistance		37	53.5	70	kΩ
[CLK Pin]						
$V_{IH(CLK)}$	Input High-level Voltage	V_{CC} = 6.3 V, 5 V	2.0	–	V_{CC}	V
$V_{IL(CLK)}$	Input Low-level Voltage	V_{CC} = 6.3 V, 5 V	0	–	1.0	V
$V_{IO(CLK)}$	Input open voltage		$V_{CC} - 0.5$	–	V_{CC}	V

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 6.3 V) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
[CLK Pin]						
$\Delta V_{IN(CLK)}$	Hysteresis	V_{CC} = 6.3 V, 5 V, design target value (Note 2)	0.13	0.22	0.31	V
$I_{IH(CLK)}$	Input High-level Current	$V_{CLK} = V_{CC}$	–10	0	+10	μA
$I_{IL(CLK)}$	Input Low-level Current	V_{CLK} = 0 V	–170	–118	–	μA
$f_{(CLK)}$	Input Frequency		–	–	3.9	kHz
$R_{U(CLK)}$	Pull-up Resistance		37	53.5	70	kΩ
[N1 Pin]						
$V_{IH(N1)}$	Input High-level Voltage	V_{CC} = 6.3 V, 5 V	2.0		V_{CC}	V
$V_{IL(N1)}$	Input Low-level Voltage	V_{CC} = 6.3 V, 5 V	0		1.0	V
$V_{IO(N1)}$	Input Open Voltage		$V_{CC} - 0.5$		V_{CC}	V
$\Delta V_{IN(N1)}$	Hysteresis	V_{CC} = 6.3 V, 5 V, design target value (Note 2)	0.13	0.22	0.31	V
$I_{IH(N1)}$	Input High-level Current	$V_N1 = V_{CC}$	–10	0	+10	μA
$I_{IL(N1)}$	Input Low-level Current	V_N1 = 0 V	–170	–118		μA
$R_{U(N1)}$	Pull-up Resistance		37	53.5	70	kΩ
[N2 Pin]						
$V_{IH(N2)}$	Input High-level Voltage	V_{CC} = 6.3 V, 5 V	2.0	–	V_{CC}	V
$V_{IL(N2)}$	Input Low-level Voltage	V_{CC} = 6.3 V, 5 V	0	–	1.0	V
$V_{IO(N2)}$	Input Open Voltage		$V_{CC} - 0.5$	–	V_{CC}	V
$\Delta V_{IN(N2)}$	Hysteresis	V_{CC} = 6.3 V, 5 V, design target value (Note 2)	0.13	0.22	0.31	V
$I_{IH(N2)}$	Input High-level Current	$V_N2 = V_{CC}$	–10	0	+10	μA
$I_{IL(N2)}$	Input Low-level Current	V_N2 = 0 V	–170	–118	–	μA
$R_{U(N2)}$	Pull-up Resistance		37	53.5	70	kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Not tested.

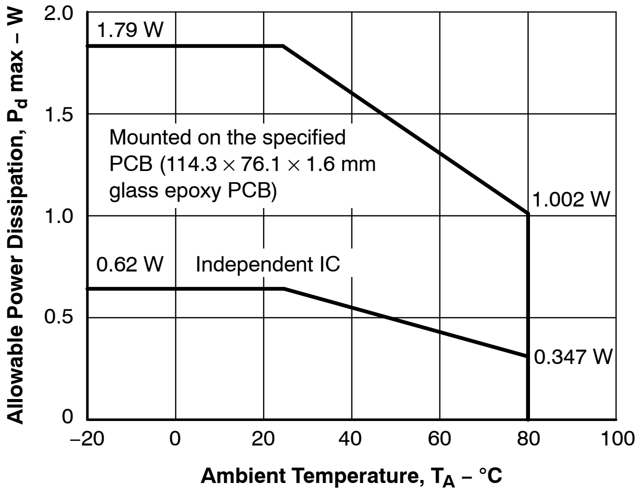


Figure 1. P_d max – T_A

SPEED DISCRIMINATOR COUNT AND VCO DIVISOR

N1	N2	Count	Divisor
High or Open	High or Open	1024	1024
High or Open	Low	1024	512
Low	High or Open	256	256
Low	Low	512	512

$$f_{FG} = \frac{\text{Divisor}}{\text{Count}} \times f_{CLK} \qquad \text{(eq. 1)}$$

THREE-PHASE LOGIC TRUTH TABLE (A HIGH (H) INPUT IS THE STATE WHERE IN+ > IN−)

Item	F/R = L			F/R = H			Output	
	IN1	IN2	IN3	IN1	IN2	IN3	PWM	–
1	H	L	H	L	H	L	VH	UL
2	H	L	L	L	H	H	WH	UL
3	H	H	L	L	L	H	WH	VL
4	L	H	L	H	L	H	UH	VL
5	L	H	H	H	L	L	UH	WL
6	L	L	H	H	H	L	VH	WL

S/S PIN

Input State	State
High or Low	Stop
Low	Start

BR PIN

Input State	State
High or Open	Brake
Low	Released

BLOCK DIAGRAM

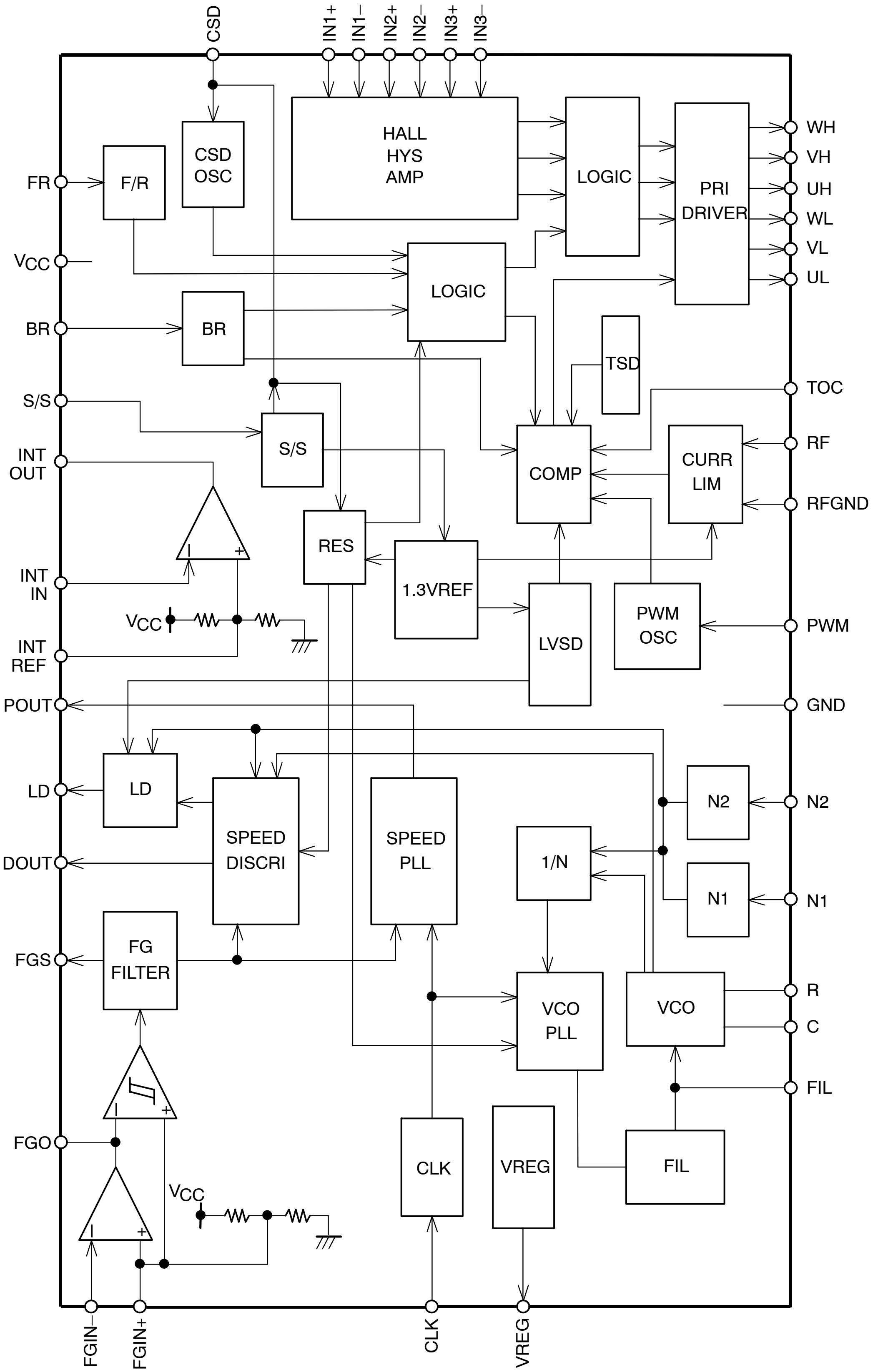
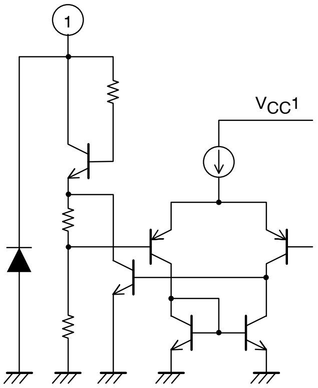
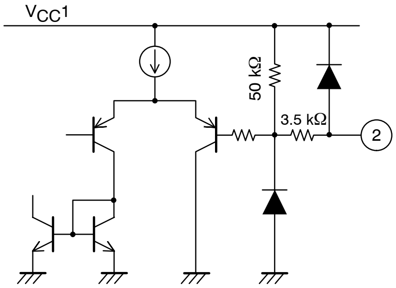
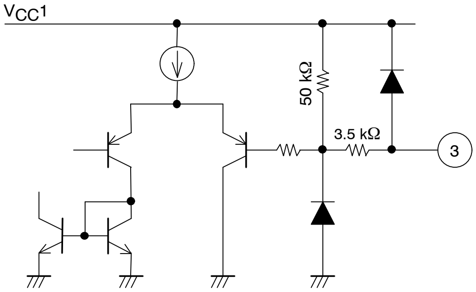
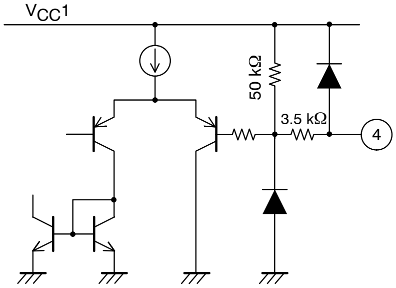


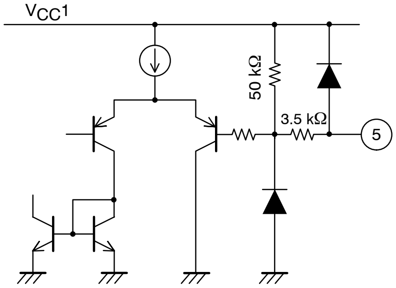
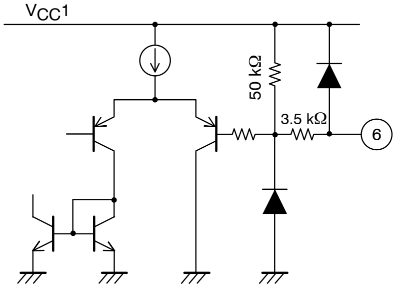
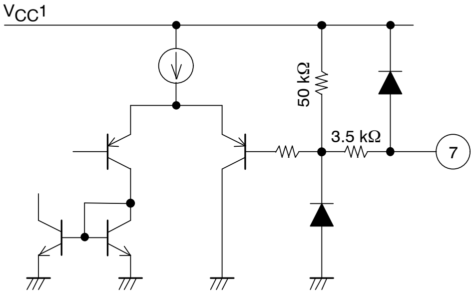
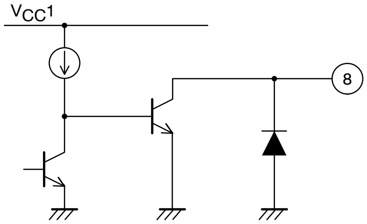
Figure 2. Block Diagram

PIN FUNCTIONS

PIN FUNCTIONS

Pin No.	Pin	Functions	Equivalent Circuit
1	VREG	7-V shunt regulator output	
2	S/S	Start/stop control Low: 0 V to 1.0 V High: 2.0 V to V_{CC} Goes high when left open. Low for start. High or open for stop. The hysteresis is about 0.22 V.	
3	CLK	External clock signal input Low: 0 V to 1.0 V High: 2.0 V to V_{CC} Goes high when left open. The hysteresis is about 0.22 V. f = 3.9 kHz, maximum	
4	F/R	Forward/reverse control Low: 0 V to 1.0 V High: 2.0 V to V_{CC} Goes high when left open. Low for forward. High or open for reverse. The hysteresis is about 0.22 V.	

PIN FUNCTIONS (continued)

<table>
<tr><th>Pin No.</th><th>Pin</th><th>Functions</th><th>Equivalent Circuit</th></tr>
<tr><td>5</td><td>BR</td><td>Brake control (short braking operation)
Low: 0 V to 1.0 V
High: 2.0 V to V_{CC}
Goes high when left open.
High or open for brake mode operation.
The hysteresis is about 0.22 V.</td><td>
</td></tr>
<tr><td>6</td><td>N1</td><td>Switches the speed discriminator VCO divisor count.
Low: 0 V to 1.0 V
High: 2.0 V to V_{CC}
Goes high when left open.
The hysteresis is about 0.22 V.</td><td>
</td></tr>
<tr><td>7</td><td>N2</td><td>The speed discriminator count switching.
Low: 0 V to 1.0 V
High: 2.0 V to V_{CC}
Goes high when left open.
The hysteresis is about 0.22 V.</td><td>
</td></tr>
<tr><td>8</td><td>FGS</td><td>FG amplifier output (after the Schmitt circuit)
This is an open collector output.</td><td>
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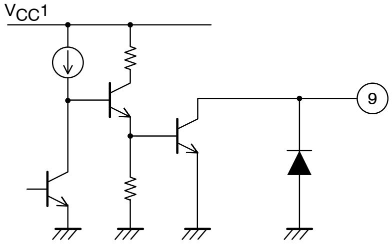
<tr><td>9</td><td>LD</td><td>Speed lock detection output
This is an open collector output.
Goes low when the motor speed is within the speed lock range (±6.25%).</td><td>
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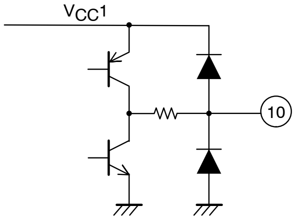
<tr><td>10</td><td>DOUT</td><td>Speed discriminator output
Acceleration → high, deceleration → low</td><td>
</td></tr>
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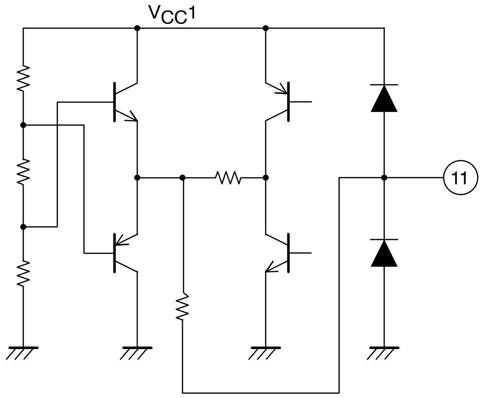
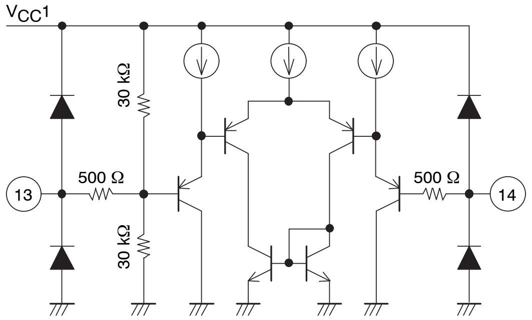
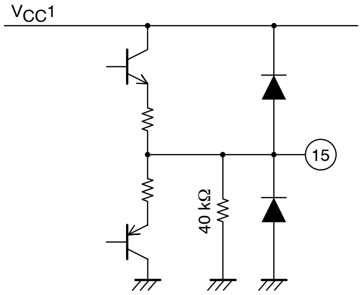
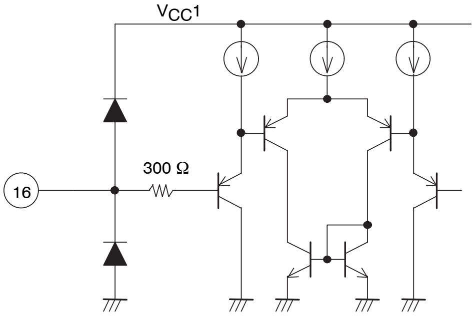
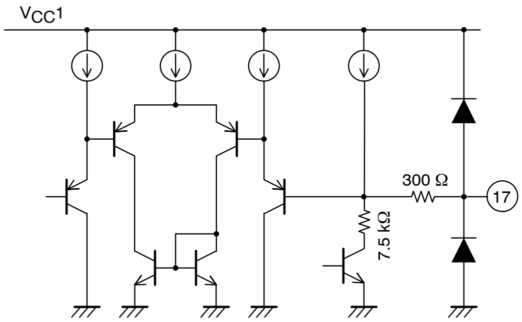
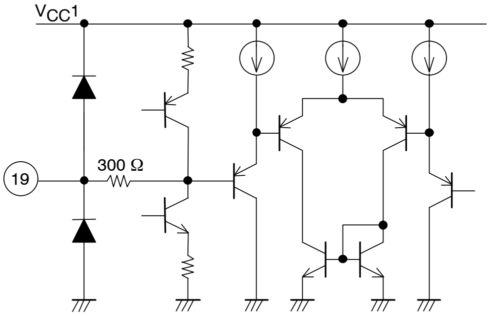
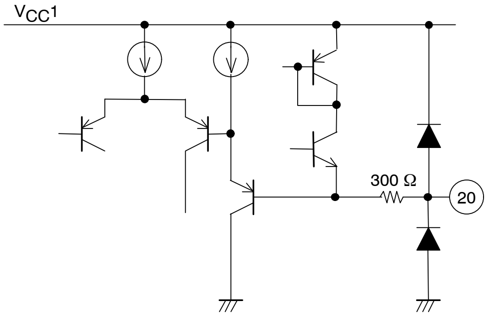
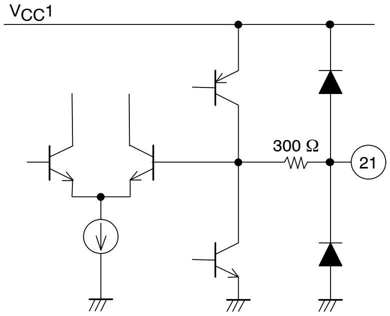
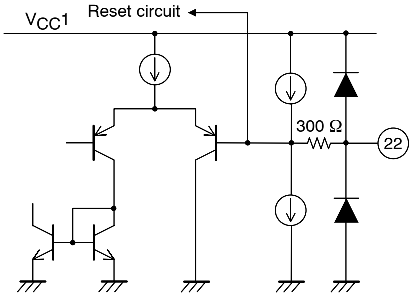
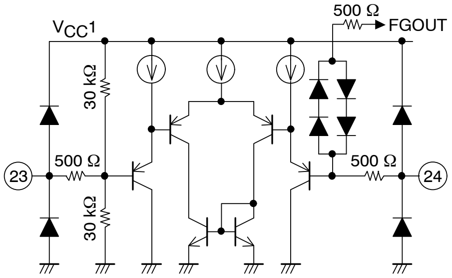
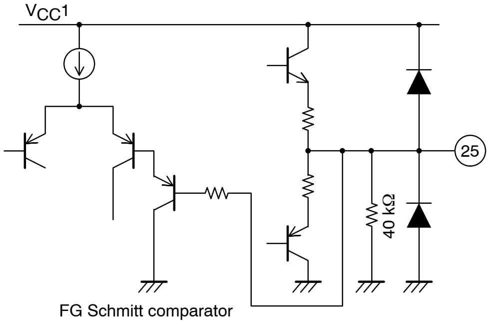
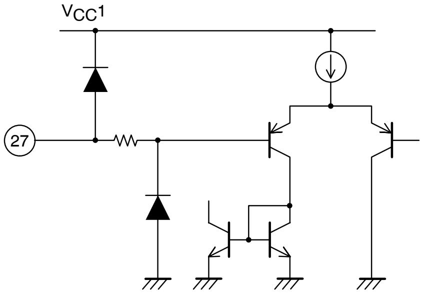
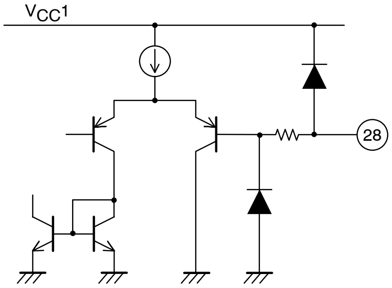
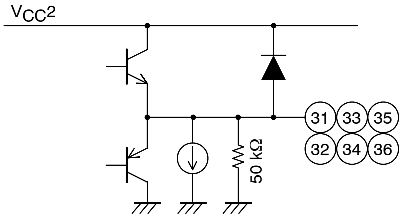
PIN FUNCTIONS (continued)

Pin No.	Pin	Functions	Equivalent Circuit
11	POUT	Speed control system PLL output Outputs the phase comparison result for CLK and FG.	
13	INT REF	Integrating amplifier non-inverting input (1/2 V_{CC} potential)	
14	INT IN	Integrating amplifier inverting input	
15	INT OUT	Integrating amplifier output (speed control)	
16	TOC	Torque command input Normally, this pin is connected to the INT.OUT pin. The PWM duty is increased when the TOC pin voltage falls. Do not apply a voltage that exceeds $V_{CC} - 0.5$ V to this pin. (An input from a normal operational amplifier is desirable.)	

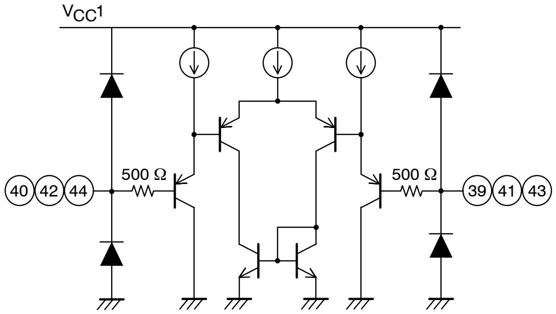
PIN FUNCTIONS (continued)

Pin No.	Pin	Functions	Equivalent Circuit
17	PWM	PWM oscillator frequency setting. Connect a capacitor between this pin and ground.	
19	FIL	VCO PLL filter connection	
20	R	Sets the value of the charge current from the VCO circuit C pin. Insert a resistor between this pin and ground.	
21	C	VCO oscillator connection This pin sets the VCO frequency. Insert a capacitor between this pin and ground. Set the value of the capacitor so that the oscillator frequency does not exceed 1 MHz.	
22	CSD	Sets the operating time of the constrained-rotor protection circuit. Reference signal oscillator used when the clock signal is cut off and to prevent malfunctions. The protection function operating time can be set by connecting a capacitor between this pin and ground. This pin also functions as the logic circuit block power-on reset pin.	

PIN FUNCTIONS (continued)

Pin No.	Pin	Functions	Equivalent Circuit
23 24	FGIN+ FGIN−	FG amplifier input	
25	FGOUT	FG amplifier output This pin is connected to the FG Schmitt comparator circuit internally in the IC.	
27	RF GND	Output current detection Connect a resistor between this pin and ground.	
28	RF	Output current detection Connect a resistor between this pin and ground. The output limitation maximum current, I_{OUT}, is set to be $0.26/R_f$ by this resistor.	
29	GND1	Control block ground	
30	GND2	Output block ground	
31 32 33 34 35 36	UL UH VL VH WL WH	Outputs (that are used to drive external transistors). The PWM duty is controlled on the UH, VH, and WH side of these outputs.	
37 38	$V_{CC}2$ $V_{CC}1$	Output block power supply Control block power supply Short $V_{CC}1$ to $V_{CC}2$ and, for stability, insert a capacitor between these pins and ground.	

PIN FUNCTIONS (continued)

Pin No.	Pin	Functions	Equivalent Circuit
39 40 41 42 43 44	IN3− IN3+ IN2− IN2+ IN1− IN1+	Hall−effect device inputs. The input is seen as a high-level input when IN+ > IN–, and as a low-level input for the opposite state. If noise on the Hall-effect device signals is a problem, insert capacitors between the corresponding IN+ and IN– inputs. The logic high state indicates that VIN+ > VIN–	
12 18 26	NC	These are unconnected pins, and can be used for wiring.	

SAMPLE APPLICATION CIRCUIT 1
(P-channel + N-channel, Hall-effect Sensor Application)

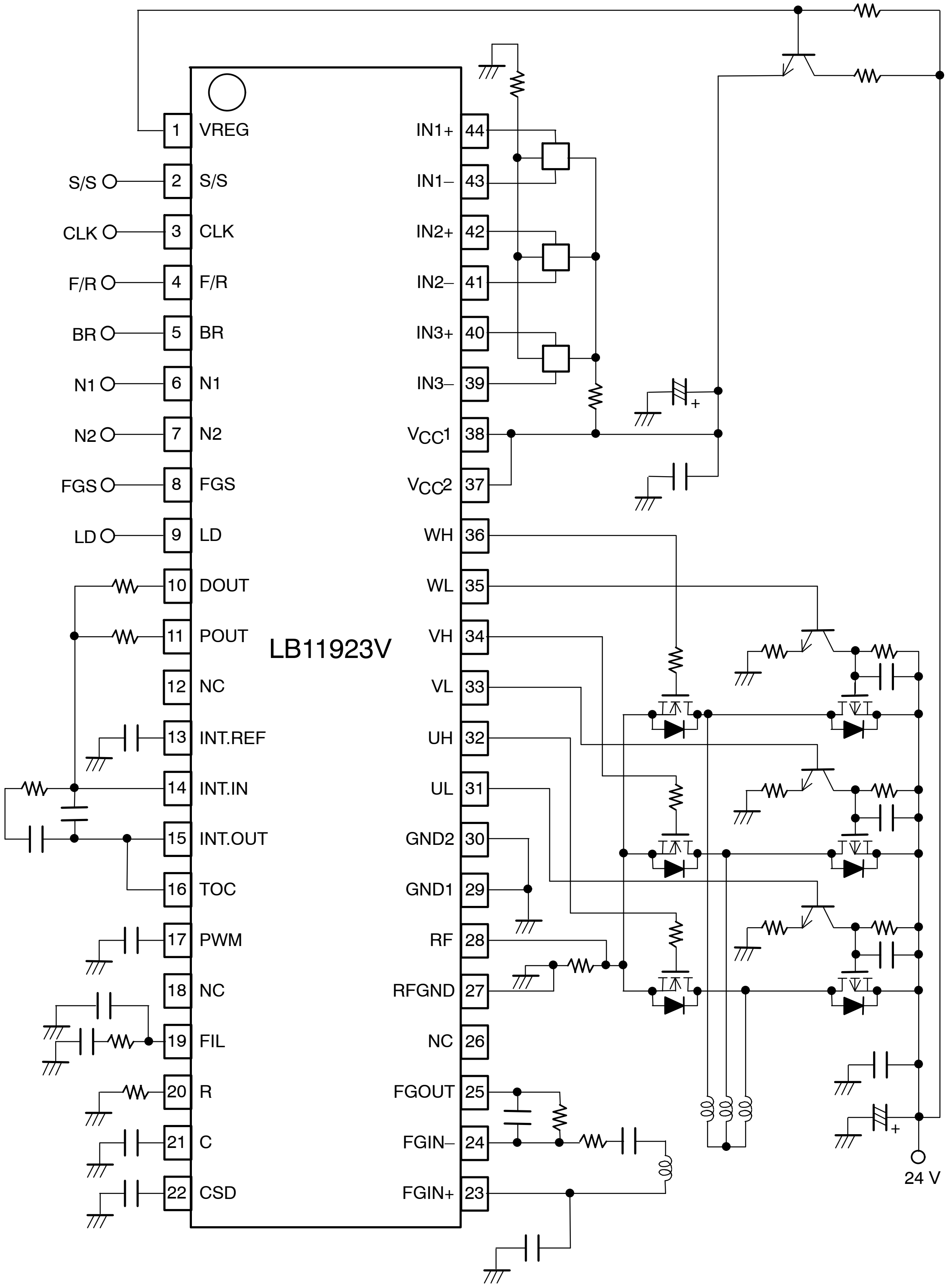


Figure 3. Sample Application Circuit 1

SAMPLE APPLICATION CIRCUIT 2
(PNP + NPN, Hall-effect Sensor Application)

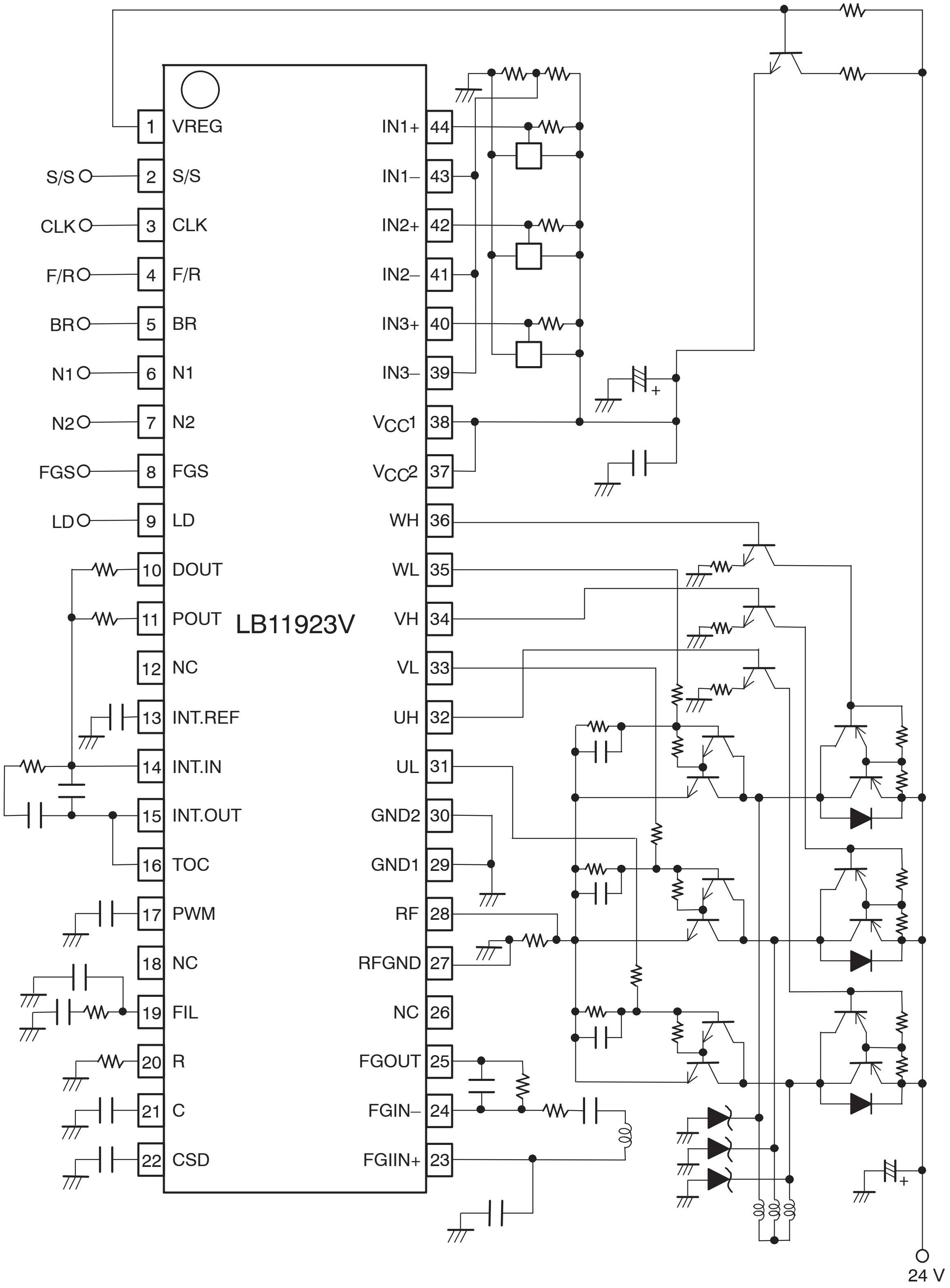


Figure 4. Sample Application Circuit 2

IC OPERATION DESCRIPTION

1. Speed Control Circuit:
   This IC implements speed control using the combination of a speed discriminator circuit and a PLL circuit. The speed discriminator circuit outputs (This counts a single FG period.) an error signal once every two FG periods. The PLL circuit outputs an error signal once every one FG Period. As compared to the earlier technique in which only a speed discriminator circuit was used, the combination of a speed discriminator and a PLL circuit allows variations in motor speed to be better suppressed when a motor that has large load variations is used. The FG servo frequency (f_{FG}) is determined by the frequency relationship shown below and by the clock signal (f_{CLK}) input to the CCLK pin.

$$f_{FG} = \frac{\text{VCO Divisor}}{\text{Speed Discriminator Count}} \times f_{CLK} \qquad \text{(eq. 2)}$$

N1	N2	Count	Divisor
High or Open	High or Open	1024	1024
High or Open	Low	1024	512
Low	High or Open	256	256
Low	Low	512	512

   Therefore it is possible to implement half−speed control without switching the clock frequency by using combinations of the N1 = high, N2 = low state and other setting states.

2. VCO Circuit:
   The LB11923V includes a built-in VCO circuit to generate the speed discriminator circuit reference signal. The reference signal frequency is given by the following formula.

$$f_{VCO} = f_{CLK} \times \text{Divisor} \qquad \text{(eq. 3)}$$

   f_{VCO}: Reference signal frequency
   f_{CLK}: Externally input clock frequency

   The range over which the reference signal frequency can be varied is determined by the resistor and capacitor components connected to the R and C pins (pins 20 and 21) and by the VCO loop filter constant (the values of the external components connected to pin 19).

Supply Voltage	R (kΩ)	C (pF)
When V_{CC} is 5 V	7.5	200
When V_{CC} is 6.3 V	11	200

   To acquire the widest possible range, it is better to use 6.3 V than 5 V as the supply voltage. It is also possible to handle an even wider range than is possible with fixed counts by making the speed discriminator count and the VCO divisor switchable. The components connected to the R, C, and FIL pins must be connected with lines to their ground pins (pins 29 and 30) that are as short as possible.

3. Output Drive Circuit:
   To reduce power loss in the output, this IC adopts the direct PWM drive technique. The output transistors (which are external to the IC) are always saturated when on, and the motor drive output is adjusted by changing the duty with which the output is on. The PWM switching is performed on the high side for each phase (UH, VH, and WH). The PWM switching side in the output can be selected to be either the high or low side depending on how the external transistors are connected.

4. Current Limiter Circuit:
   The current limiter circuit limits the (peak) current at the value $I = V_{RF}/R_f$ ($V_{RF} = 0.26$ V (typical), R_f: current detection resistor). The current limitation operation consists of reducing the output duty to suppress the current.
   High accuracy detection can be achieved by connecting the RF and RFGND pin lines near the ends of the current detection resistor (R_f).

5. Speed Lock Range:
   The speed lock range is ±6.25% of the fixed speed. When the motor speed is in the lock range, the LD pin (an open collector output) goes low. If the motor speed goes out of the lock range, the motor on duty is adjusted according to the speed error to control the motor speed to be within the lock range.

6. Notes on the PWM Frequency:
   The PWM frequency is determined by the capacitor (F) connected to the PWM pin.

$$\text{When } V_{CC} = 6.3\text{ V: } f_{PWM} \approx \frac{1}{82000 \times C} \qquad \text{(eq. 4)}$$

$$\text{When } V_{CC} = 5.0\text{ V: } f_{PWM} \approx \frac{1}{66000 \times C} \qquad \text{(eq. 5)}$$

   A PWM frequency of between 15 and 25 kHz is desirable. If the PWM frequency is too low, the motor may resonate at the PWM frequency during motor control, and if that frequency is in the audible range, that resonation may result in audible noise. If the PWM frequency is too high, the output transistor switching loss will increase. To make the circuit less susceptible to noise, the connected capacitors must be connected to the GND pin (pin 29 and pin 30) with lines that are as short as possible.

7. Hall Effect Sensor Input Signals:
   An input amplitude of over 100 mV p-p is desirable in the Hall effect sensor inputs. The closer the input waveform is to a square wave, the lower the required input amplitude. Inversely, a higher input amplitude is required the closer the input waveform is to a triangular wave. Also note that the input DC voltage must be set to be within the common-mode input voltage range.
   If noise on the Hall inputs is a problem, that noise must be excluded by inserting capacitors across the inputs. Those capacitors must be located as close as possible to the input pins.
   When the Hall inputs for all three phases are in the same state, all the outputs will be in the off state.
   If a Hall sensor IC is used to provide the Hall inputs, those signals can be input to one side (either the + or − side) of the Hall effect sensor signal inputs as 0 to VCC level signals if the other side is held fixed at a voltage within the common-mode input voltage range that applies when a Hall effect sensors are used.
8. Forward/Reverse Switching:
   The motor rotation direction can be switched using the F/R pin. However, the following notes must be observed if the motor direction is switched while the motor is turning.
   - This IC is designed to avoid through currents when switching directions. However, increases in the motor supply voltage (due to instantaneous return of motor current to the power supply) during direction switching may cause problems. The values of the capacitors inserted between power and ground must be increased if this increase is excessive.
   - If the motor current after direction switching exceeds the current limit value, the PWM drive side outputs will be turned off, but the opposite side output will be in the short-circuit braking state, and a current determined by the motor back EMF voltage and the coil resistance will flow. Applications must be designed so that this current does not exceed the ratings of the output transistors used. (The higher the motor speed at which the direction is switched, the more severe this problem becomes.)
9. Brake Switching:
   The LB11923V provides short-circuit braking implemented by turning the output transistors for the high side for all phases (UH, VH, and WH) on. (The opposite side transistors are turned off for all phases.) Note that the current limiter does not operate during braking. During braking, the duty is set to 100%, regardless of the motor speed. The current that flows in the output transistors during braking is determined by the motor back EMF voltage and the coil resistance. Applications must be designed so that this current does not exceed the ratings of the output transistors used. (The higher the motor speed at which braking is applied, the more severe this problem becomes.)
   The braking function can be applied and released with the IC in the start state. This means that motor startup and stop control can be performed using the brake pin with the S/S pin held at the low level (the start state). If the startup time becomes excessive, it can be reduced by controlling motor startup and stop with the brake pin rather than with the S/S pin. (Since the IC goes to the power saving state when stopped, enough time for the VCO circuit to stabilize will be required at the beginning of the motor start operation.)
10. Constraint Protection Circuit:
    The LB11923V includes an on-chip constraint protection circuit to protect the IC and the motor in motor constraint mode. If the LD output remains high (indicating the locked state) for a fixed period in the start state, the upper side (external) transistors are turned off. This time is set by the capacitance of the capacitor attached to the CROCK pin. A time of a few seconds can be set with a capacitance of under 0.1 μF.

    When $V_{CC} = 6.3$ V:
    The set time (in seconds) is $37 \times C$ (μF) (eq. 6)

    When $V_{CC} = 5.0$ V:
    The set time (in seconds) is $30 \times C$ (μF) (eq. 7)

    To clear the rotor constrained protection state, the application must either switch to the stop state for a fixed period (about 1 ms or longer) or turn off and reapply power.
    If the rotor constrained protection circuit is not used, a 220 kΩ resistor and a 1500 pF capacitor must be connected in parallel between the CSD pin and ground. However, in that case, the clock disconnect protection circuit described below will no longer function. Since the CSD pin also functions as the power-on reset pin, if the CSD pin were connected directly to ground, the IC would go to the power-on reset state and motor drive operation would remain off. The power-on reset state is cleared when the CSD pin voltage rises above a level of about 0.64 V.
11. Clock Disconnect Protection Circuit:
    If the clock input goes to the no input state when the IC is in the start state, this protection circuit will operate and turn off the PWM output. If the clock is resupplied before the motor constraint protection circuit operates, the IC will return to the drive state, but if the motor constraint protection circuit does operate, the IC must either be set temporarily (approximately 1 ms or over) to the

stop or brake state, or the power must be turned off and reapplied.

12. Low-voltage Protection Circuit:
    The LB11923V includes a low-voltage protection circuit to protect against incorrect operation when power is first applied or if the power-supply voltage (V_{CC}) falls. The (external) all output transistors are turned off if V_{CC} falls under about 3.75 V, and this function is cleared at about 4.0 V.
13. Power Supply Stabilization:
    Since this IC is used in applications that draw large output currents, the power-supply line is subject to fluctuations. Therefore, capacitors with capacitances adequate to stabilize the power-supply voltage must be connected between the V_{CC} pin and ground. If diodes are inserted in the power-supply line to prevent IC destruction due to reverse power supply connection, since this makes the power-supply voltage even more subject to fluctuations, even larger capacitors will be required.
14. Ground Lines:
    The signal system ground and the output system ground must be separated and a single ground point must be taken at the connector. Since the output system ground carries large currents, this ground line must be made as short as possible.
    - Output system ground ... Ground for R_f and the output diodes
    - Signal system ground ... Ground for the IC and the IC external components
15. V_{REG} Pin:
    If a motor drive system is formed from a single power supply, the V_{REG} pin (pin 1) can be used to create the power-supply voltage (about 6.3 V) for this IC. The V_{REG} pin is a shunt regulator and generates a voltage of about 7 volts by passing a current through an external resistor. A stable voltage can be generated by setting the current to value in the range 0.2 to 1.5 mA. The external transistors must have current capacities of at least 80 mA (to cover the I_{CC} + Hall bias current + output current <source> requirements) and they must have voltage handling capacities in excess of the motor power−supply voltage. Since the heat generated by these transistor may be a problem, heat sinks may be required depending on the packages used. If the IC power-supply voltage (4.4 to 7.0 V) is provided from an external circuit, apply that voltage directly to the V_{CC} pin (pin 37 and pin 38). In that case, the V_{REG} pin must either be left open or connected to ground.
16. FG Amplifier:
    The FG amplifier is normally implemented as a filter amplifier such as that shown in the application circuits to reject noise. Since a clamp circuit has been added at the FG amplifier output, the output amplitude is clamped at about 3 V p-p, even if the gain is increased.
    Since a Schmitt comparator is inserted after the FG amplifier, applications must set the gain so that the amplifier output amplitude is at least 250 mV p-p. (It is desirable that the gain be set so that the amplitude is over 0.5 V p-p at the lowest controlled speed to be used.)
    The capacitor inserted between the $FGIN^+$ pin (pin 23) and ground is required for bias voltage stabilization. To make the connected capacitor as immune from noise as possible, connect this capacitor to the GND pin (pin 29 and pin 30) with a line that is as short as possible.
17. Integrating Amplifier:
    The integrating amplifier integrates the speed error pulses and the phase error pulses and converts them to a speed command voltage. At the same time it also sets the control loop gain and frequency characteristics using external components.
    The integrating amplifier output (pin 15) is normally connected to the TOC pin (pin 16) using external wiring. In cases where it is necessary to switch the integration constant in an application that uses a wide speed range by isolating the integrating amplifier output and the PWM control circuit, this type of constant switching application can be implemented by adding external operational amplifier, analog switch, and other components.
    In either case, the basic idea is that the operational amplifier output is connected to the TOC pin. (Note that voltages in excess of $V_{CC} - 0.5$ V must not be applied to the TOC pin.)
18. FIL Pin External Components:
    The capacitor inserted between the FIL pin and ground is used to suppress ripple on the FIL pin voltage. Therefore, application designers must select a capacitance value that provides fully adequate smoothing of the FIL pin voltage even at the lowest external clock input frequency used.
    Also, the FIL pin voltage convergence time (the time until the reference signal stabilizes) when the input clock frequency is switched is shortened by connecting a resistor and a capacitor in series between the FIL pin and ground. Therefore, designers must select values for the resistor and capacitor that give the required convergence time.
19. R and C Pin External Components:
    The maximum range over which the reference signal frequency f_{VCO} can be varied when 5 V is used as the V_{CC} supply voltage is about a factor of three.
    When it is desirable to make this range as wide as

possible, since the values of the R pin external resistor (R) and the C pin external capacitor (C) are determined by the maximum value of the reference signal frequency ($f_{VCO}1$) and the minimum value ($V_{CC}L$) of the V_{CC} power supply due to unit-to-unit variations, R and C can be determined using the following procedure as a reference.

(1) Calculate R1 and C1 using the following formulas and determine values for R and C such that the conditions R ≤ R1 and C ≤ C1 will hold taking the sample-to-sample variations (including other issues such as temperature characteristics) into account.

$$R1 = \frac{(V_{CC} - 2.2\ V)}{280\ \mu A} \qquad \text{(eq. 8)}$$

$$C1 = \frac{280\ \mu A}{0.9\ V} \times \frac{1}{f_{VCOL}} \times 0.7 \qquad \text{(eq. 9)}$$

(2) The minimum value ($f_{VCO}2$) for the reference signal frequency that can be set for the R and C values determined in step (1) can be calculated from the following formula if we let R2 and C2 be the smallest values for R and C due to the sample-to-sample variations (including other issues such as temperature characteristics). Therefore, the range over which the reference signal frequency can be set is $f_{VCO}1$ to $f_{VCO}2$.

$$f_{VCO}2 = \frac{0.38}{R2 \times C2} \qquad \text{(eq. 10)}$$

(3) The following are the conditions that must be met and the points that require care when determining the values of the external components connected to the R and C pins.

a. The maximum value of the set reference signal frequency must not exceed 1 MHz.

b. The R pin voltage and the FIL pin voltage must be in the range 0.3 V to ($V_{CC}L$ – 2.2 V). ($V_{CC}L$ is the lowest value of the V_{CC} supply voltage given the unit-to-unit variations. $V_{CC}L$ is always greater than or equal to 4.4 V.) However, the lower the R pin voltage, the more susceptible the system will be to ground line noise, and the reference signal frequency may become unstable as a result. Therefore the lower end of the R pin voltage range must not be used if there is much ground line noise in the system.

c. Set the value of the R pin external resistor to a value in the range 6.8 kΩ to 15 kΩ. Also, assure that the R pin current remains under 280 μA.

d. Set the value of the C pin external capacitor to a value in the range 150 pF to 1000 pF.

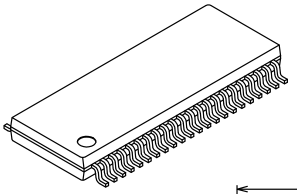
e. When it is desirable to make the range of the reference signal frequency as wide as possible, set the values of R and C to the largest possible values. (However, those values must be lower than the calculated values R1 and C1.) Use components with the smallest sample-to-sample variations possible. The V_{CC} voltage must be made as much higher than 5 V as possible by, for example, using this IC's VREG pin (7 V shunt regulator), to acquire the widest possible range for the reference signal frequency.

20. NC Pin:
Since the NC pins are electrically open with respect to the IC itself, they can be used as intermediate connection points for lines in the PCB pattern.

ORDERING INFORMATION

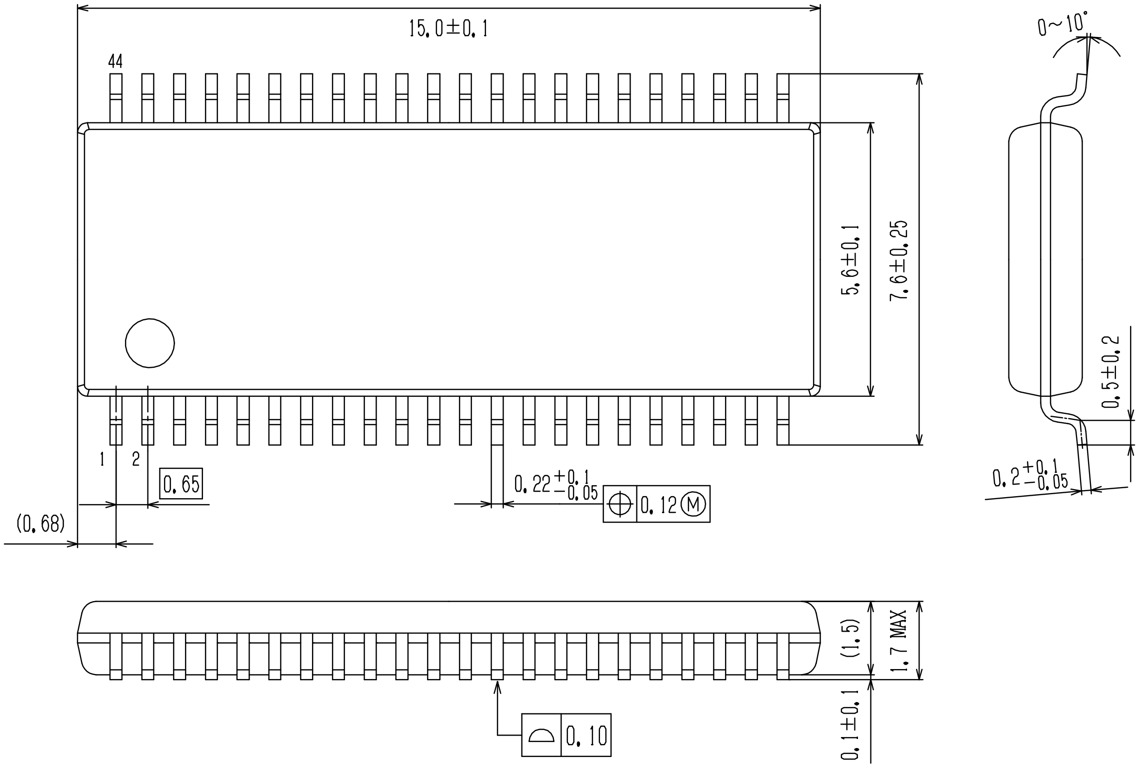
Device	Package	Wire Bond	Shipping† (Qty / Packing)
LB11923V−TLM−E	SSOP44 (275mil) (Pb−Free)	Au−wire	2,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

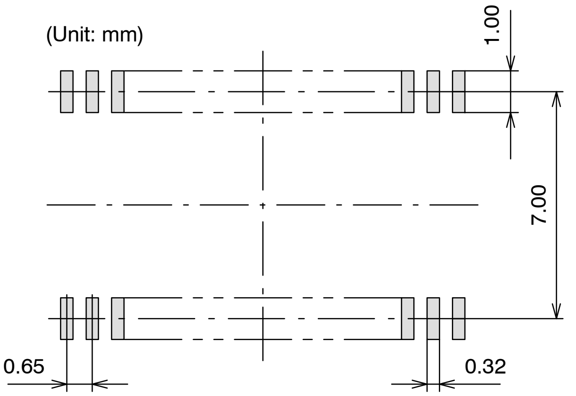


SSOP44 (275mil)
CASE 565AW
ISSUE A

DATE 25 NOV 2013



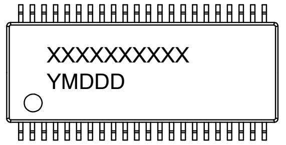
SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**SSOP44 (275MIL)**	**PAGE 1 OF 2**

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION FROM SANYO ENACT# S−225 TO ON SEMICONDUCTOR. REQ. BY D. TRUHITTE.	30 JAN 2012
A	ADDED MARKING AND SOLDER FOOTPRINT INFORMATION. REQ. BY D. TRUHITTE	25 NOV 2013

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