LC051281XA

CMOS LSI 2-Cell Lithium-Ion Secondary Battery Protection IC

ON Semiconductor®

www.onsemi.com

WLCSP8, 1.01x1.11
CASE 567GR

MARKING DIAGRAM

○ = Index Mark
D5 = Specific Device Code
Y = Year Code
ID = ID Code (2 Characters)

ORDERING INFORMATION

Device	Package	Shipping†
LC051281XA−MH	WLCSP8,1.01x1.11 (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Overview

LC051281XA is a battery protection IC for 2−Cell Lithium−Ion secondary battery.

This IC integrates high accuracy voltage detectors and delay time circuits, and protects battery from over−charge, over−discharge, discharge over−current (2 steps), Charge over−current, and Short circuit.

Charge alarm function which is compliant with PSE (Product Safety Electrical Appliance & Material) is also built in. It outputs the signal to control charger ahead of over−charge detecting.

Package is Flip−Chip.

Features

- High Accuracy Detection / Release Voltage (Laser Trimming)

Symbol	Parameter	Typical Value	Accuracy (Ta = 25°C)
Voc	Over−charge detection voltage	4.210 V	±25 mV
Vochys	Over−charge release hysteresis voltage	0.200 V	+25% of setting
Vchg	Charger alarm detection voltage	4.100 V	±25 mV
Vodc	Over−discharge detection voltage	2.300 V	±100 mV
Vodca1	Discharge over−current1 detection voltage	0.100 V	±20 mV
Vodca2	Discharge over−current2 detection voltage	0.300 V	±20 mV
Vsh	Short circuit detection voltage	0.700 V	±15% of setting
Voca	Charge over−current detection voltage	−0.200 V	±20 mV

- Over−charge /Over−charge Release
  Release Hysteresis is Canceled when VM Pin Voltage is more than Discharge Over−current2 Detection Voltage by Load Connection. Discharge Release is Done only by Connecting Charger and does not Have Release Hysteresis.

- Safety Design in Overlap Detection
  In Overlap Detection of Over−charge and Over−discharge, Over−charge has Priority.
  In Overlap Detection of Over−charge and Discharge Over−current, both Detections are Made in Parallel.
  In Overlap Detection of Over−discharge and Discharge Over−current, Both Detections are Made in Parallel,and this IC will Go on to Stand−by Mode after Over−discharge Detection.
  Short Circuit Detection is Done Independently.
- Discharge Over−current Detection has Three Steps, Two Steps of Discharge Over−current Detection and Short Circuit Detection
- Charge Alarm Detectors are Independent from Over−charge Detectors. (CHG Output is Nch Open Drain)
- Selectable 0 V Battery Charging Function is Enabled
- Absolute Maximum Ratings 25 V (VM, CO)
- In Reversed Charge, it has a Function that Turns Off DO Terminal Rapidly
- Small Design Footprint

- Delay Times (Mask Option)

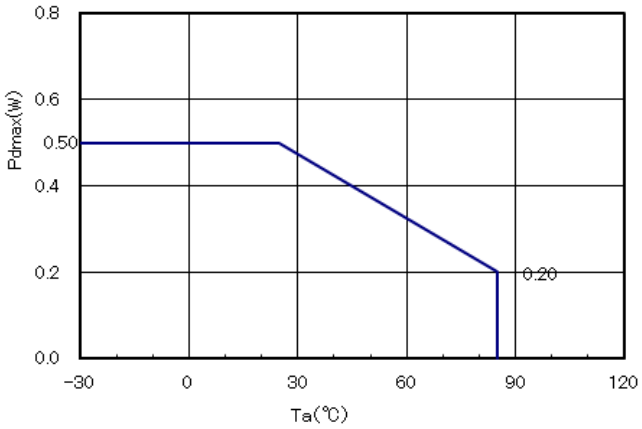
Symbol	Parameter	Typical Value	Accurancy (Ta = 25°C)
Toc	Over−charge detection delay time	1 sec	±0.3 sec
Tocr	Over−charge release delay time	16 msec	±4.8 msec
Tchg	Charge alarm detection delay time	50 msec	±15 msec
Tchgr	Charge alarm release delay time	50 msec	±15 msec
Todc	Over−discharge detection delay time	100 msec	±30 msec
Todcr	Over−discharge release delay time	1 msec	±0.3 msec
Todca1	Discharge over−current1 detection delay time	20 msec	±6 msec
Todca2	Discharge over−current2 detection delay time	1 msec	±0.3 msec
Todcar	Discharge over−current release time	1 msec	±0.3 msec
Tsh	Short circuit detection delay time	375 μsec	±120 μsec
Toca	Charge over−current detection delay time	8 msec	±2.4 msec
Tocar	Charge over−current release time	1 msec	±0.3 msec

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Symbol	Parameter	Rating	Unit
VDD	Power supply voltage	VSS − 0.3 to VSS + 12.0	V
VM	VM pin input voltage	VDD − 25 to VDD + 0.3	V
VCO	CO pin output voltage	VM − 0.3 to VDD + 0.3	V
VDO	DO pin output voltage	VSS − 0.3 to VDD + 0.3	V
PD	Allowable power dissipation	500	mW
Topr	Operating ambient temperature	−30 to +85	°C
Tstg	Storage temperature	−40 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Absolute maximum ratings represent the values which cannot be exceeded for any length of time.
2. Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.



Size: 30.2 x 13.7 x 0.8 mm: 2 layers of glass epoxysubstrate

Figure 1. Pdmax−Ta

RECOMMENDED OPERATION CONDITIONS (Ta = 25°C)

Symbol	Parameter	Rating	Unit
VDD	Power supply voltage	6.0 to 8.0	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (Topr = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Circuit
DETECTION VOLTAGE (VcellH = VDD − VC, VcellL = VC − VSS)							
Voc	Over−charge detection voltage		4.185	4.210	4.235	V	1
Vochys	Over−charge release hysteresis voltage		0.150	0.200	0.250	V	1
Vchg	Charger alarm detection voltage		4.075	4.100	4.125	V	1
Vodc	Over−discharge detection voltage		2.200	2.300	2.400	V	1
Vodcr	Over−discharge release voltage		2.200	2.300	2.400		
Vodca1	Discharge over−current1 detection voltage	VcellH = 3.5 V, VcellL = 3.5 V	0.080	0.100	0.120	V	1
Vodca2	Discharge over−current2 detection voltage	VcellH = 3.5 V, VcellL = 3.5 V	0.280	0.300	0.320	V	1
Vsh	Short circuit detection voltage	VcellH = 3.5 V, VcellL = 3.5 V	0.595	0.700	0.805	V	1
Voca	Charge over−current detection voltage	VcellH = 3.5 V, VcellL = 3.5 V	−0.220	−0.200	−0.180	V	1
DELAY TIME							
Toc	Over−charge detection delay time		0.7	1	1.3	sec	2
Tocr	Over−charge release delay time		11.2	16	20.8	msec	2
Tchg	Charge alarm detection delay time		35	50	65	msec	2
Tchgr	Charge alarm release delay time		35	50	65	msec	2
Todc	Over−discharge detection delay time		70	100	130	msec	2
Todcr	Over−discharge release delay time		0.7	1	1.3	msec	2
Todca1	Discharge over−current1 detection delay time	VcellH = 3.5 V, VcellL = 3.5 V	14	20	26	msec	2
Todca2	Discharge over−current2 detection delay time	VcellH = 3.5 V, VcellL = 3.5 V	0.7	1	1.3	msec	2
Todcar	Discharge over−current release time	VcellH = 3.5 V, VcellL = 3.5 V	0.7	1	1.3	msec	2
Tsh	Short circuit detection delay time	VcellH = 3.5 V, VcellL = 3.5 V	255	375	495	μsec	2
Toca	Charge over−current detection delay time	VcellH = 3.5 V, VcellL = 3.5 V	5.6	8	10.4	msec	2
Tocar	Charge over−current release time	VcellH = 3.5 V, VcellL = 3.5 V	0.7	1	1.3	msec	2
OTHERS							
Idd	Operating current	VcellH = 3.5 V, VcellL = 3.5 V	−	7	10	μA	3
Istb	Standby current	VcellH = 1.9 V, VcellL = 4.0 V	−	−	0.1	μA	3
Ivc	VC input current	VcellH = 3.5 V, VcellL = 3.5 V	−	−	0.1	μA	3
Ivm	VM output current	VcellH = 3.5 V, VcellL = 3.5 V VM = 0 V	70	150	270	μA	3
Vinl	Operating input voltage	VDD − VSS voltage Judged by whether short circuit can work even in the rapid fall of VDD.	2.0	−	10	V	1
Vmr	VM reverse charge detection voltage	VcellH = 3.5 V, VcellL = 3.5 V (VM voltage = VDD + Vmr)	0.15	0.25	0.35	V	1
Vz1	0 V cell charging minimum operation voltage	VDD − VSS = 0 V, VDD − VM voltage (0 V cell charging enabled)	1.5	−	−	V	1
Vstb	Standby release voltage	VcellH = 1.9 V, VcellL = 2.1 V VM − VSS voltage	VDD x 0.35	VDD x 0.5	VDD x 0.65	V	1

ELECTRICAL CHARACTERISTICS (Topr = 25°C, unless otherwise noted) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Circuit
OTHERS							
Vtest	TEST mode threshold voltage	VcellH = 3.5 V, VcellL = 3.5 V (Test mode: TEST = VDD)	VDD x 0.35	VDD x 0.5	VDD x 0.65	V	1
Rtest	TEST pin internal pull up resistance		250	500	750	kΩ	1
Rdd	Rdd pull up resistance		100	200	300	kΩ	3
Rss	Rss pull down resistance		15	30	45	kΩ	3
Voncn	CO pin voltage with Nch ON	VcellH = 4.4 V, VcellL = 4.4 V Iol = 50 μA	–	–	VM + 0.5	V	4
Voncp	CO pin voltage with Pch ON	VcellH = 3.9 V, VcellL = 3.9 V Iol = −50 μA	VDD − 0.5	–	–	V	4
Vondn	DO pin voltage with Nch ON	VcellH = 1.9 V, VcellL = 1.9 V Iol = 50 μA	–	–	0.5	V	4
Vondp	DO pin voltage with Pch ON	VcellH = 3.9 V, VcellL = 3.9 V Iol = −50 μA	VDD − 0.5	–	–	V	4
Vonchg	CHG pin voltage with Nch ON	VcellH = 4.4 V, VcellL = 4.4 V Iol = 50 μA	–	–	VM + 0.5	V	4
Ichg	CHG pin Nch leak current	VcellH = 3.9 V, VcellL = 3.9 V	–	–	0.1	μA	4

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ELECTRICAL CHARACTERISTICS (Topr = 0 to 60°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Circuit
DETECTION VOLTAGE (VcellH = VDD − VC, VcellL = VC − VSS)							
Voc	Over−charge detection voltage		4.185	4.210	4.235	V	1
Vochys	Over−charge release hysteresis voltage		0.150	0.200	0.250	V	1
Vchg	Charger alarm detection voltage		4.075	4.100	4.125	V	1
Vodc	Over−discharge detection voltage		2.200	2.300	2.400	V	1
Vodcr	Over−discharge release voltage		2.200	2.300	2.400		
Vodca1	Discharge over−current1 detection voltage	VcellH = 3.5 V, VcellL = 3.5V	0.075	0.100	0.125	V	1
Vodca2	Discharge over−current2 detection voltage	VcellH = 3.5 V, VcellL = 3.5V	0.275	0.300	0.325	V	1
Vsh	Short circuit detection voltage	VcellH = 3.5 V, VcellL = 3.5V	0.585	0.700	0.815	V	1
Voca	Charge over−current detection voltage	VcellH = 3.5 V, VcellL = 3.5V	−0.225	−0.200	−0.175	V	1
DELAY TIME							
Toc	Over−charge detection delay time		0.55	1	1.45	sec	2
Tocr	Over−charge release delay time		8.8	16	23.2	msec	2
Tchg	Charge alarm detection delay time		27.5	50	72.5	msec	2
Tchgr	Charge alarm release delay time		27.5	50	72.5	msec	2
Todc	Over−discharge detection delay time		55	100	145	msec	2
Todcr	Over−discharge release delay time		0.55	1	1.45	msec	2
Todca1	Discharge over−current1 detection delay time	VcellH = 3.5 V, VcellL = 3.5 V	11	20	29	msec	2
Todca2	Discharge over−current2 detection delay time	VcellH = 3.5 V, VcellL = 3.5 V	0.55	1	1.45	msec	2

ELECTRICAL CHARACTERISTICS (Topr = 0 to 60°C) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Circuit
DELAY TIME							
Todcar	Discharge over−current release time	VcellH = 3.5 V, VcellL = 3.5 V	0.55	1	1.45	msec	2
Tsh	Short circuit detection delay time	VcellH = 3.5 V, VcellL = 3.5 V	205	375	545	μsec	2
Toca	Charge over−current detection delay time	VcellH = 3.5 V, VcellL = 3.5 V	4.4	8	11.6	msec	2
Tocar	Charge over−current release time	VcellH = 3.5 V, VcellL = 3.5 V	0.55	1	1.45	msec	2
OTHERS							
Idd	Operating current	VcellH = 3.5 V, VcellL = 3.5 V	−	7	10	μA	3
Istb	Standby current	VcellH = 1.9 V, VcellL = 4.0 V	−	−	0.1	μA	3
Ivc	VC input current	VcellH = 3.5 V, VcellL = 3.5 V	−	−	0.1	μA	3
Ivm	VM output current	VcellH = 3.5 V, VcellL = 3.5 V VM = 0 V	40	150	300	μA	3
Vinl	Operating input voltage	VDD − VSS voltage Judged by whether short circuit can work even in the rapid fall of VDD.	2.2	−	10	V	1
Vmr	VM reverse charge detection voltage	VcellH = 3.5 V, VcellL = 3.5 V (VM voltage = VDD + Vmr)	0.1	0.25	0.4	V	1
Vz1	0 V cell charging minimum operation voltage	VDD − VSS = 0 V, VDD − VM voltage (0 V cell charging enabled)	1.7	−	−	V	1
Vstb	Standby release voltage	VcellH = 1.9 V, VcellL = 2.1 V VM − VSS voltage	VDD x 0.3	VDD x 0.5	VDD x 0.7	V	1
Vtest	TEST mode threshold voltage	VcellH = 3.5 V, VcellL = 3.5 V (Test mode: TEST = VDD)	VDD x 0.3	VDD x 0.5	VDD x 0.7	V	1
Rtest	TEST pin internal pull up resistance		200	500	900	kΩ	1
Rdd	Rdd pull up resistance		80	200	360	kΩ	3
Rss	Rss pull down resistance		12	30	54	kΩ	3
Voncn	CO pin voltage with Nch ON	VcellH = 4.4 V, VcellL = 4.4 V Iol = 50 μA	−	−	VM + 0.5	V	4
Voncp	CO pin voltage with Pch ON	VcellH = 3.9 V, VcellL = 3.9 V Iol = −50 μA	VDD − 0.5	−	−	V	4
Vondn	DO pin voltage with Nch ON	VcellH = 1.9 V, VcellL = 1.9 V Iol = 50 μA	−	−	0.5	V	4
Vondp	DO pin voltage with Pch ON	VcellH = 3.9 V, VcellL = 3.9 V Iol = −50 μA	VDD − 0.5	−	−	V	4
Vonchg	CHG pin voltage with Nch ON	VcellH = 4.4 V, VcellL = 4.4 V Iol = 50 μA	−	−	VM + 0.5	V	4
Ichg	CHG pin Nch leak current	VcellH = 3.9 V, VcellL = 3.9 V	−	−	0.1	μA	4

*These values are all design target and not to be guaranteed.
*These are not measured at this temperature range before shipment.
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ELECTRICAL CHARACTERISTICS (Topr = −20 to 60°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Circuit
DETECTION VOLTAGE (VcellH = VDD − VC, VcellL = VC − VSS)							
Voc	Over−charge detection voltage		4.175	4.210	4.245	V	1
Vochys	Over−charge release hysteresis voltage		0.150	0.200	0.250	V	1
Vchg	Charger alarm detection voltage		4.065	4.100	4.135	V	1
Vodc	Over−discharge detection voltage		2.200	2.300	2.400	V	1
Vodcr	Over−discharge release voltage		2.200	2.300	2.400		
Vodca1	Discharge over−current1 detection voltage	VcellH = 3.5 V, VcellL = 3.5 V	0.070	0.100	0.130	V	1
Vodca2	Discharge over−current2 detection voltage	VcellH = 3.5 V, VcellL = 3.5 V	0.270	0.300	0.330	V	1
Vsh	Short circuit detection voltage	VcellH = 3.5 V, VcellL = 3.5 V	0.580	0.700	0.820	V	1
Voca	Charge over−current detection voltage	VcellH = 3.5 V, VcellL = 3.5 V	−0.230	−0.200	−0.170	V	1
DELAY TIME							
Toc	Over−charge detection delay time		0.5	1	1.5	sec	2
Tocr	Over−charge release delay time		8	16	24	msec	2
Tchg	Charge alarm detection delay time		25	50	75	msec	2
Tchgr	Charge alarm release delay time		25	50	75	msec	2
Todc	Over−discharge detection delay time		50	100	150	msec	2
Todcr	Over−discharge release delay time		0.5	1	1.5	msec	2
Todca1	Discharge over−current1 detection delay time	VcellH = 3.5 V, VcellL = 3.5 V	10	20	30	msec	2
Todca2	Discharge over−current2 detection delay time	VcellH = 3.5 V, VcellL = 3.5 V	0.5	1	1.5	msec	2
Todcar	Discharge over−current release time	VcellH = 3.5 V, VcellL = 3.5 V	0.5	1	1.5	msec	2
Tsh	Short circuit detection delay time	VcellH = 3.5 V, VcellL = 3.5 V	187	375	563	μsec	2
Toca	Charge over−current detection delay time	VcellH = 3.5 V, VcellL = 3.5 V	4	8	12	msec	2
Tocar	Charge over−current release time	VcellH = 3.5 V, VcellL = 3.5 V	0.5	1	1.5	msec	2
OTHERS							
Idd	Operating current	VcellH = 3.5 V, VcellL = 3.5 V	−	7	10	μA	3
Istb	Standby current	VcellH = 1.9 V, VcellL = 4.0 V	−	−	0.1	μA	3
Ivc	VC input current	VcellH = 3.5 V, VcellL = 3.5 V	−	−	0.1	μA	3
Ivm	VM output current	VcellH = 3.5 V, VcellL = 3.5 V VM = 0 V	20	150	300	μA	3
Vinl	Operating input voltage	VDD − VSS voltage Judged by whether short circuit can work even in the rapid fall of VDD.	2.3	−	10	V	1
Vmr	VM reverse charge detection voltage	VcellH = 3.5 V, VcellL = 3.5 V (VM voltage = VDD + Vmr)	0.1	0.25	0.4	V	1
Vz1	0 V cell charging minimum operation voltage	VDD − VSS = 0 V, VDD − VM voltage (0 V cell charging enabled)	1.8	−	−	V	1
Vstb	Standby release voltage	VcellH = 1.9 V, VcellL = 2.1 V VM − VSS voltage	VDD x 0.3	VDD x 0.5	VDD x 0.7	V	1

ELECTRICAL CHARACTERISTICS (Topr = −20 to 60°C) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Circuit
OTHERS							
Vtest	TEST mode threshold voltage	VcellH = 3.5 V, VcellL = 3.5 V (Test mode: TEST = VDD)	VDD x 0.3	VDD x 0.5	VDD x 0.7	V	1
Rtest	TEST pin internal pull up resistance		200	500	1000	kΩ	1
Rdd	Rdd pull up resistance		80	200	400	kΩ	3
Rss	Rss pull down resistance		12	30	T60	kΩ	3
Voncn	CO pin voltage with Nch ON	VcellH = 4.4 V, VcellL = 4.4 V Iol = 50 μA	−	−	VM + 0.5	V	4
Voncp	CO pin voltage with Pch ON	VcellH = 3.9 V, VcellL = 3.9 V Iol = −50 μA	VDD − 0.5	−	−	V	4
Vondn	DO pin voltage with Nch ON	VcellH = 1.9 V, VcellL = 1.9 V Iol = 50 μA	−	−	0.5	V	4
Vondp	DO pin voltage with Pch ON	VcellH = 3.9 V, VcellL = 3.9 V Iol = −50 μA	VDD − 0.5	−	−	V	4
Vonchg	CHG pin voltage with Nch ON	VcellH = 4.4 V, VcellL = 4.4 V Iol = 50 μA	−	−	VM + 0.5	V	4
Ichg	CHG pin Nch leak current	VcellH = 3.9 V, VcellL = 3.9 V	−	−	0.1	μA	4

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
*These values are all design target and not to be guaranteed.
*These are not measured at this temperature range before shipment.

MEASUREMENT CONDITIONS

1. *Over−charge detection voltage, Over−charge release hysteresis voltage (Circuit1)*
   Set V1 = V2 = 3.5 V, V3 = 0 V, V4 = 0 V and increase V1 gradually.
   V1 voltage which CO pin is turned to “L” is defined as over−charge detection voltage (Voc−upper).
   From this over−charge state, decrease V1 gradually. V1 voltage which CO pin is returned to “H” is defined as over−charge release voltage (Vocr−upper). Then, Over−charge release hysteresis voltage (Vochys−upper) is defined as (Voc−upper) − (Vocr−upper).
   Equally on the initial conditions, increase V2 gradually.
   V2 voltage which CO pin is turned to “L” is defined as over−charge detection voltage (Voc−lower).
   From over−charge state, decrease V2 gradually. V2 voltage which CO pin is returned to “H” is defined as over−charge release voltage (Vocr−lower). Then, Over−charge release hysteresis voltage (Vochys−lower) is defined as (Voc−lower) − (Vocr−lower).
2. *Charge alarm detection voltage (Circuit 1)*
   Set V1 = V2 = 3.5 V, V3 = 0 V, V4 = 0 V and increase V1 gradually.
   V1 voltage which CHG pin is turned to “L” is defined as charge alarm detection voltage (Vchg−upper).
   Equally on the initial conditions, increase V2 gradually. V2 voltage which CHG pin is turned to “L” is defined as charge alarm detection voltage (Vchg−lower).
3. *Over−discharge detection voltage (Circuit 1)*
   Set V1 = V2 = 3.5 V, V3 = 0 V, V4 = 0 V and decrease V1 gradually.
   V1 voltage which DO pin is turned to “L” is defined as over−discharge detection voltage (Vodc−upper).
   Equally on the initial conditions, decrease V2 gradually. V2 voltage which DO pin is turned to “L” is defined as over−discharge detection voltage (Vodc−lower).
4. *Discharge over−current1 detection voltage (Circuit 1)*
   Set V1 = V2 = 3.5 V, V3 = 0 V, V4 = 0 V and increase V3 gradually.
   V3 voltage which DO pin is turned to “L” after delay time (Todca1) is defined as discharge over−current1 detection voltage (Vodca1).
5. *Discharge over−current2 detection voltage (Circuit 1)*
   Set V1 = V2 = 3.5 V, V3 = 0 V, V4 = 0 V and increase V3 rapidly.
   V3 voltage which DO pin is turned to “L” after delay time (Todca2) is defined as discharge over−current2 detection voltage (Vodca2).

6. *Short circuit detection voltage (Circuit 1)*
   Set V1 = V2 = 3.5 V, V3 = 0 V, V4 = 0 V and increase V3 rapidly.
   V3 voltage which DO pin is turned to “L” after delay time (Tsh) is defined as short circuit detection voltage (Vsh).
7. *Charge over−current detection voltage (Circuit 1)*
   Set V1 = V2 = 3.5 V, V3 = 0 V, V4 = 0 V and decrease V3 gradually.
   V3 voltage which CO pin is turned to “L” after delay time (Toca) is defined as charge over−current detection voltage (Voca).
8. *Over−charge detection delay time, Over−charge release delay time (Circuit 2)*
   Set V1 = 3.5 V, V2 = 4.26 V, V3 = 0 V, and V4 = 0 V.
   Time after changing V2 from 4.26 V to 4.4 V rapidly until CO pin is turned to “L” is defined as over−charge detection delay time (Toc).
   From this state, set V3 = 0.4 V in order to cancel release hysteresis.
   Time after changing V2 from 4.4 V to 4.26 V rapidly until CO pin is returned to “H” is defined as over−charge release delay time (Tocr).
9. *Charge alarm detection delay time, Charge alarm release delay time (Circuit 2)*
   Set V1 = 3.5 V, V2 = 4.1 V, V3 = 0 V, and V4 = 0 V.
   Time after changing V2 from 4.1 V to 4.26 V rapidly until CHG pin is turned to “L” is defined as charge alarm detection delay time (Tchg).
   Then, time after changing V2 from 4.26 V to 4.1 V rapidly until CHG pin is returned to “H” is defined as charge alarm release delay time (Tocr).
10. *Over−discharge detection delay time, Over−discharge release delay time (Circuit 2)*
    Set V1 = 3.5 V, V2 = 2.2 V, V3 = 0 V, and V4 = 0 V.
    Time after changing V2 from 2.2 V to 1.8 V rapidly until DO pin is turned to “L” is defined as over−discharge detection delay time (Todc).
    Then, time after changing V2 from 1.8 V to 2.2 V rapidly until DO pin is returned to “H” is defined as over−discharge release delay time (Todcr).
11. *Discharge over−current1 detection delay time, Discharge over−current release time (Circuit 2)*
    Set V1 = 3.5 V, V2 = 3.5 V, V3 = 0 V, and V4 = 0 V.
    Time after changing V3 from 0 V to 1.5 V rapidly until DO pin is turned to “L” is defined as discharge over−current1 detection delay time (Todca1).
    Then, time after changing V3 from 1.5 V to 0 V rapidly until DO pin is returned to “H” is defined as discharge over−current release delay time (Todcar).
12. *Discharge over−current2 detection delay time (Circuit 2)*
    Set V1 = 3.5 V, V2 = 3.5 V, V3 = 0 V, and V4 = 0 V.
    Time after changing V3 from 0 V to 0.4 V rapidly until DO pin is turned to “L” is defined as discharge over−current2 detection delay time (Todca2).
13. *Short circuit detection delay time (Circuit 2)*
    Set V1 = 3.5 V, V2 = 3.5 V, V3 = 0 V, and V4 = 0 V.
    Time after changing V3 from 0 V to 1.0 V rapidly until DO pin is turned to “L” is defined as short circuit detection delay time (Tsh).
14. *Charge over−current detection delay time, Charge over−current release time (Circuit 2)*
    Set V1 = 3.5 V, V2 = 3.5 V, V3 = 0 V, and V4 = 0 V.
    Time after changing V3 from 0 V to −0.2 V rapidly until CO pin is turned to “L” is defined as charge over−current detection delay time (Toca).
    Then, time after changing V3 from −0.2 V to 0 V rapidly until DO pin is returned to “H” is defined as charge over−current release delay time (Tocar).
15. *Operating current, VC input current, VM output current (Circuit 3)*
    Set V1 = 3.5 V, V2 = 3.5 V, and V3 = 0 V.
    Operating current (Idd) is defined as VDD pin current. VC input current (Ivc) is defined as VC pin current. VM output current (Ivm) is defined as VM pin current.
16. *Standby current (Circuit 3)*
    Set V1 = 1.8 V, V2 = 2.2 V, and V3 = 4 V as over−discharge state.
    Standby current (Istb) is defined as VDD pin current.
17. *Operating input voltage (Circuit 1)*
    Set V1 = 3.5 V, V2 = 3.5 V, V3 = 0 V, and V3 = 0 V.
    Minimum side of operating input voltage (Vinl) is defined as VDD voltage which short circuit can work even in the rapid fall of VDD.
    And maximum side of operating input voltage (Vinl) is defined as VDD which over−charge and charge alarm detection operate normally within absolute maximum rating of VDD.
18. *VM reverse charge detection voltage (Circuit 1)*
    Set V1 = V2 = 3.5 V, V3 = 0 V, V4 = 0 V and increase V3 0 V to (VDD + Vmr) rapidly.
    V3 voltage − VDD which DO pin is turned to “L” within Tsh is defined as VM reverse charge detection voltage (Vmr).
19. *0 V cell charging minimum operation voltage (Circuit 1) (LC051281XA select enable.)*
    Set V1 = V2 = V3 = V4 = 0 V and decrease V3 gradually.
    VDD − VM voltage which CO pin is turned to “H” (VDD level) is defined as 0 V cell charging minimum operation voltage (Vz1).
20. *0 V cell charging prohibition voltage (Circuit 1) *(reference)*
    Set V1 = V2 = 2 V, V3 = −4 V, V4 = 0 V and decrease V1 and V2 gradually.
    VDD voltage which CO pin is turned to “L” is defined as 0 V cell charging prohibition voltage (Vz2).

21. *Standby release voltage (Circuit 3)*
    Set V1 = 1.8 V, V2 = 2.2 V, and V3 = 4 V as standby state.
    Standby current (Istb) is defined as VDD pin current. When VM voltage is decreased, VM current flows out through Rdd pulled down. Operating current Idd is got by subtracting VM current from VDD current. Standby release voltage (Vstb) is defined as VM voltage that Idd starts to flow when decreasing VM.
22. *TEST mode threshold voltage (Circuit 1)*
    Set V1 = 3.5 V, V2 = (Vchg − 0.1 V), V3 = 0 V, V4 = 0 V, and increase V4 gradually.
    When V2 is changed from (Vchg − 0.1 V) to (Vchg + 0.1 V), V4 voltage which delay time of CHG pin is cancelled, is defined as test mode threshold voltage (Vtest).
23. *Rdd pull up resistance (Circuit 3)*
    Set V1 = 1.8 V, V2 = 2.2 V, and V3 = 4 V as standby mode.
    VM current at VM = 3 V is defined as I1 and VM current at VM = 2.9 V is defined as I2.
    The value calculated by 0.1 / (I2 − I1) is defined as Rdd pull up resistance (Rdd).
24. *Rss pull down resistance (Circuit 3)*
    Set V1 = V2 = 3.5 V, and V3 = V4 = 0 V.
    VM current at VM = 1 V is defined as I1 and VM current at VM = 1.1 V is defined as I2.
    The value calculated by 0.1 / (I2 − I1) is defined as Rss pull down resistance (Rss).
25. *CO pin voltage with Nch ON and CHG pin voltage with Nch ON (Circuit 4)*
    Set V1 = V2 = 4.4 V, and V3 = V4 = 0 V.
    CO pin voltage with 50 μA current impressed is defined as CO pin voltage with Nch ON (Voncn).
    Also CHG pin voltage with 50 μA current impressed is defined as CHG pin voltage with Nch ON (Vonchg).
26. *CO pin voltage with Pch ON CHG pin voltage with Nch ON (Circuit 4)*
    Set V1 = V2 = 3.9 V, and V3 = V4 = 0 V.
    CO pin voltage with 50 μA pulled is defined as CO pin voltage with Pch ON (Voncp).
    Also CHG pin voltage with 50 μA pulled is defined as DO pin voltage with Pch ON (Vondp).
27. *CO pin voltage with Nch ON voltage (Circuit 4)*
    Set V1 = 1.8 V, V2 = 2.0 V, and V3 = V4 = 0 V.
    DO pin voltage with 50 μA impressed is defined as DO pin voltage with Nch ON (Vondn).
28. *CHG Nch leak current(Circuit 4)*
    Set V1 = V2 = 3.9 V, V3 = V4 = 0 V, and V3 = 7.8 V.
    Leak current which flows out from CHG pin is defined as CHG Nch leak current (Ichg).

MEASUREMENT CIRCUITS

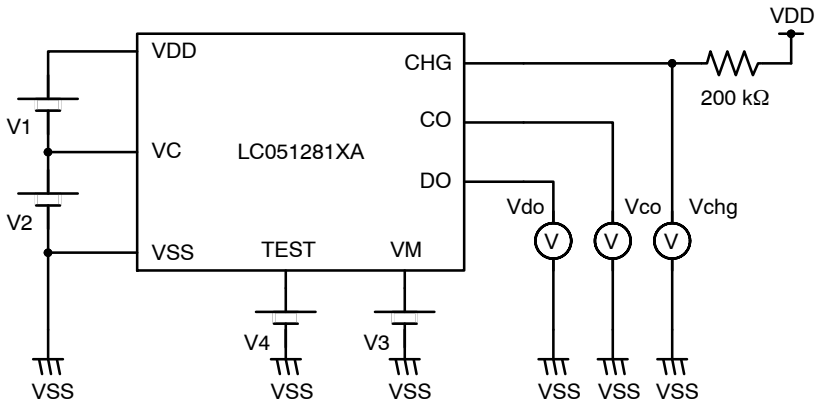


Figure 2. Circuit 1

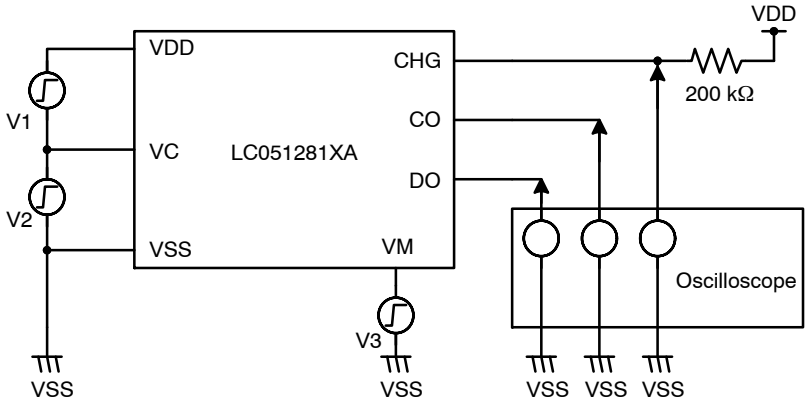


Figure 5. Circuit 2

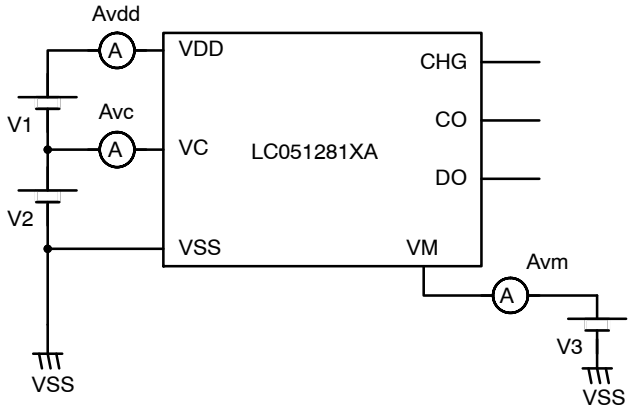


Figure 3. Circuit 3

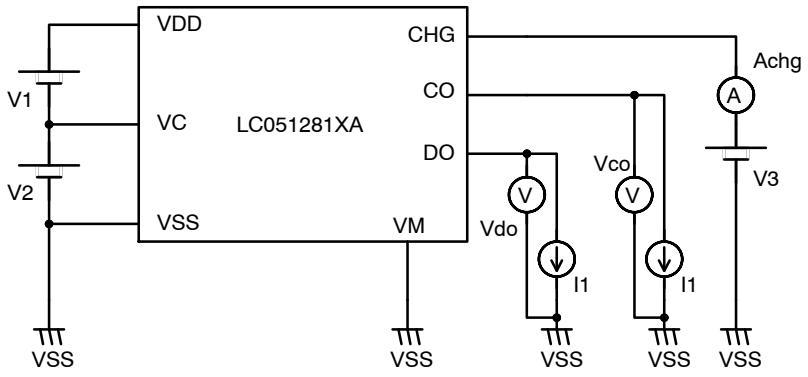


Figure 4. Circuit 4

DESCRIPTION OF OPERATION

Normal State

This IC controls over−charge and over−discharge by monitoring both of cell voltages.

(VcellH = VDD − VC, VcellL = VS − VSS) and VM pin voltage.

If both of cell voltages are between over−discharge detection voltage (Vodc) and over−charge detection voltage (Voc), and VM pin voltage is between charge over−current detection voltage (Voca) and discharge over−current1 detection voltage (Vodca1), CO and DO pin are set to “H”. Then external FET for charging and discharging is turned on. Therefore both of charging and discharging are possible.

This is called normal state.

Over−charge Detection / Release

If either of cell voltages is equal to or higher than over−charge detection voltage (Voc) at charging normal state battery cell, CO pin will turned to “L” after over−charge detection delay time (Toc). And then charging will stopped by charging control FET turned off. This is called over−charge detection state.

Release from over−charge detection will be done as shown below.

(1) In case that VM pin voltage is lower than Vodca2, if both of cell voltages are lower than over−charge release voltage (= Voc − Vochys) for over−charge release delay time (Tocr), CO pin will be turned to “H” and also charge control FET will be turned on. In this case, release hysteresis is enabled.

(2) When load is connected, VM pin voltage will go up by the current through the parasitic diode of external charge control FET. If VM pin voltage remains higher than over−current detection2 voltage (Vodca2), and both of cell voltages are lower than Voc for over−charge release delay time (Tocr), CO pin will be turned to “H” and also charge control FET will be turned on. In this case, release hysteresis is cancelled.

Charge Alarm Detection / Release

Charge alarm output (CHG pin) is Nch open drain transistor based on VM level. In normal state, output transistor will be turned off and CHG pin becomes “H” by connecting external pull−up resistor. If either of cell voltages is equal to or higher than the charge alarm voltage (Vchg) at charging for charger alarm detection delay time (Tchg), Nch open drain transistor will be turned on and CHG pin will be “L” as VM level. When both of cell voltages are lower than charge alarm voltage (Vchg) for charge alarm release delay time (Tchgr), Nch open drain transistor will be turned off and charge alarm is released.

*About over−charge detection and charger alarm detection delay time

Over−charge detection starts after the charge alarm detection delay is finished.

If cell voltages go up gradually and the time which cell voltages increase from Vchg to Voc is longer than Tchg, delay time will be Toc until CO pin is turned to “L” after cell voltages is beyond Voc.

When charge alarm and over−charge detect at the same time, delay time will be (Tchg + Toc) until CO terminal is turned to ”L.”

Similarly in release, when over−charge release and charger alarm release occurs at the same time, delay time will be (Tocr + Tchgr) at the maximum.

Over−discharge Detection / Release

If either of cell voltages is equal to or lower than over−discharge detection voltage (Vodc) for over−discharge detection delay time (Todc), DO pin will be turned to “L” and also discharge control FET will be turned off. Then discharging will be stopped. At this time VM pin is pulled up by resistor between VM and VDD (Rdd). This is called over−discharge detection state.

After over−discharge detection is made and VM pin goes up to VDD by Rdd, all internal circuits are stopped and operating current is cut down as standby state.

Release from over−discharge is done as follows. Both of cell voltages is higher than Vodc for over−discharge release delay time (Todcr) by charger connected, DO pin will be turned to “H” and discharge control FET will be turned on.

When charger is connected at over−discharge, VM voltage falls down by a parasitic diode Vf of discharge control FET from VSS.

If charger is connected, and either of or both of cell voltages are in over−discharge, and VM pin voltage is lower than Voca, then VM pull−up resistor (Rdd) does not pulled up.

Charge Over−current Detection / Release

If VM pin voltage is lower than charge over−current detection voltage (Voca) for charge over−current detection delay time (Toca) in charging normal state battery cell, CO pin will be turned to “L” and also charge control FET will be turned off. Then charging will be stopped. This is called charge over−current detection state.

Release from charge over−current is done as follows. If VM pin voltage is higher than Voca for charge over−current release delay time (Tocar), charge over−current will be released. Then CO pin will be turned to “H” and also charge control FET will be turned on. After over−discharge detection, charge over−current detection does not work because charging makes VM pin voltage goes up to Vf as parasitic diode of discharge control FET.

Discharge Over−current1, Discharge Over−current2, Short Circuit Detection / Release

If VM pin voltage is equal to or higher than discharge over−current detection1 voltage (Vodca1), and is lower than discharge over−current2 detection voltage (Vodca2) for discharge over−current detection delay1 time (Todca1) in discharging normal state battery cell, DO pin will be turned to “L” and also discharge control FET will be turned off. Then discharging will be stopped. This is called discharge over−current detection 1.

If VM pin is equal to or higher than discharge over−current detection2 voltage (Vodca2), and is lower than short circuit detection voltage (Vsh) for discharge over−current detection delay2 time (Todca2) in discharging normal state battery cell, DO pin will be turned to “L” and also discharge control FET will be turned off. Then discharging will be stopped. This is called discharge over−current detection 2.

Furthermore if VM pin voltage is equal to or higher than short circuit detection voltage (Vsh) for short circuit detection delay time (Tsh), DO pin will be turned to “L” and also discharge control FET will be turned off. Then discharging will be stopped. This is called short circuit detection state.

When over discharge−current2 or short circuit detection occurs before discharge over−current detection1 delay time (Todca1) elapsed, DO pin will be turned to “L” in the each detection delay time.

And when over discharge−current2 or short circuit detection releases before discharge over−current detection delay time (Todca1) elapsed, there is no release time. And discharge over−current detection1 / 2 don’t work after over−charge detection. But, short circuit detection is done independently.

When discharge over−current1 / 2 or short circuit is detected, VM terminal is pulled down to VSS by resistor between VM and Vss (Rss).

Release from discharge over−current1 / 2 or short circuit are as follows.

1. Load is detached.
2. Battery pack resistance between (+) and (−) is equal to or higher than automatic releasable impedance (VM terminal is pulled down to Vss by Rss in load detached.)
3. VM terminal voltage is lower than discharge over−current detection1 voltage (Vodca1)

*Automatic releasable impedance value of between (+) and (−) is depend on VDD, discharge over−current detection1 voltage (Vodc1), and external resistance R4. It is defined by the following equation.

*Automatic Releasable Impedance = Rss * (VDD / Vodc1) − (Rss + R4)*

0 V Battery Charging

0 V battery charging enabled function

This function can charge 0V battery cell by self discharge.

When charger which voltage is equal to or higher than 0 V cell charging minimum operation voltage (Vz1) is connected between (+) and (−), charging is enabled by charge control FET turned on.

Both of cell voltages will go up equal to or higher than Vodc, charging will be stopped and will be in normal state.

Reverse Charging

When VM pin voltage is higher than (VDD + Vmr) by charger applied in reverse, DO pin will turned to “L” rapidly.

TEST Mode Function

TEST pin would be better to be connected to VSS in order to prevent malfunction, although the terminal is pulled down to VSS by 500 kΩ internally.

OPERATION IN CASE OF OVERLAP DETECTION

Table 1.

Condition 1	Condition 2	Operation in Case of Overlap Detection	States after Detection
During over−charge detection	Over −discharge detection occurs	Over−charge detection has priority. (over−discharge detection is interrupted)	CO pin is turned off. If over−charge detection is fixed, Todc is started to count and DO pin is turned to “L” after Todc is counted up. And then VM pin is pulled up by Rdd. However, IC does not go on to standby mode
	Discharge over−current 1 / 2 occurs	Detect in parallel (Discharge over−current detection 1 / 2 does not work after over−charge detection is fixed)	If discharge over−current detection is fixed first, DO pin is turned off and VM pin is pulled down by Rss. After that, if over−charge detection is fixed, CO pin is turned to “L”.
			If over−charge detection is fixed first, CO pin is turned to “L”. In this case, discharge over−current detection 1 / 2 is cancelled.
	Charge over−current detection occurs	Detect in parallel	CO pin is turned off.
During over −discharge detection	Over−charge detection occurs	Over−charge detection has priority. (over−discharge detection is interrupted)	CO pin is turned off. If over−charge detection is fixed, Todc is started to count and DO pin is turned to “L” after Todc is counted up. And then VM pin is pulled up by Rdd. However, IC does not go on to standby mode.
	Discharge over−current 1 / 2 occurs	Detect in parallel	If discharge over−current detection is fixed first, DO pin is turned off and VM pin is pulled down by Rss. After that, if over−discharge detection is fixed, VM pin is pulled up by Rdd, and pull down by Rss is cancelled. And IC goes on to standby mode.
			If over−discharge detection is fixed first, VM pin is pulled up by Rdd and IC goes on to standby mode.
	Charge over−current detection occurs	Detect in parallel (Charge over−current detection doesn’t work after over−discharge detection is fixed)	If charge over−current detection is fixed first, CO pin is turned to “L”. After that, if over−discharge detection is fixed, DO pin is turned to “L” and VM pin is pulled up by Rdd. (Since charger should be connected in detecting charge over−current, IC does not go on to standby mode.)
			If over−discharge detection is fixed first, DO pin is turned to “L” and VM pin is pulled up by Rdd. However, IC does not go on to standby mode for the reason mentioned above. Charge over−current detection is cancelled after over−discharge detection is fixed.
During discharge over−current 1 / 2 detection	Over−charge detection occurs	Detect in parallel (Discharge over−current detection 1 / 2 are canceled after over−charge detection is fixed)	If discharge over−current detection is fixed first, DO pin is turned to “L” and VM pin is pulled down by Rss. After that, if over−charge detection is determined, CO pin is turned to “L”.
			If over−charge detection is fixed first, CO pin is turned to “L”. Discharge over−current detection 1 / 2 is cancelled after over−charge detection is fixed.
	Over −discharge detection occurs	Detect in parallel	If discharge over−current is fixed first, DO pin is turned to “L” and VM pin is pulled down by Rss. After that, if over−discharge detection is fixed, VM pin is pulled up by Rdd, and pull down by Rss is cancelled. And IC goes on to standby mode.
			If over−discharge detection is fixed first, VM pin is pulled up by Rdd and IC goes on to standby mode.

Table 1. (continued)

Condition 1	Condition 2	Operation in Case of Overlap Detection	States after Detection
During charge over−current detection	Over−charge detection occurs	Detect in parallel	CO pin is turned off.
	Over −discharge detection occurs	Detect in parallel (Charge over−current detection doesn't work after over−discharge detection is fixed)	If charge over−current detection is fixed first, CO pin is turned to "L". After that, if over−discharge detection is fixed, DO pin is turned to "L" and VM pin is pulled up by Rdd. (Since charger should be connected in detecting charge over−current, IC does not go on to standby mode.)
			If over−discharge detection is fixed first, DO pin is turned to "L" and VM pin is pulled up by Rdd. However, IC does not go on to standby mode for the reason mentioned above. Charge over−current detection is cancelled after over−discharge detection is fixed.

3. Short circuit detection is done independently.
4. VM pin voltage rises after over−charge detection, because internal current flows out through the parasitic diode of external charge control FET.
   (At this time, discharge over−current1 / 2 do not work.)
   Unexpected short circuit detection may be caused when VM pin voltage rises remarkably by unusual current flowing through the parasitic diode of external charge control FET.

TIMING CHART 1

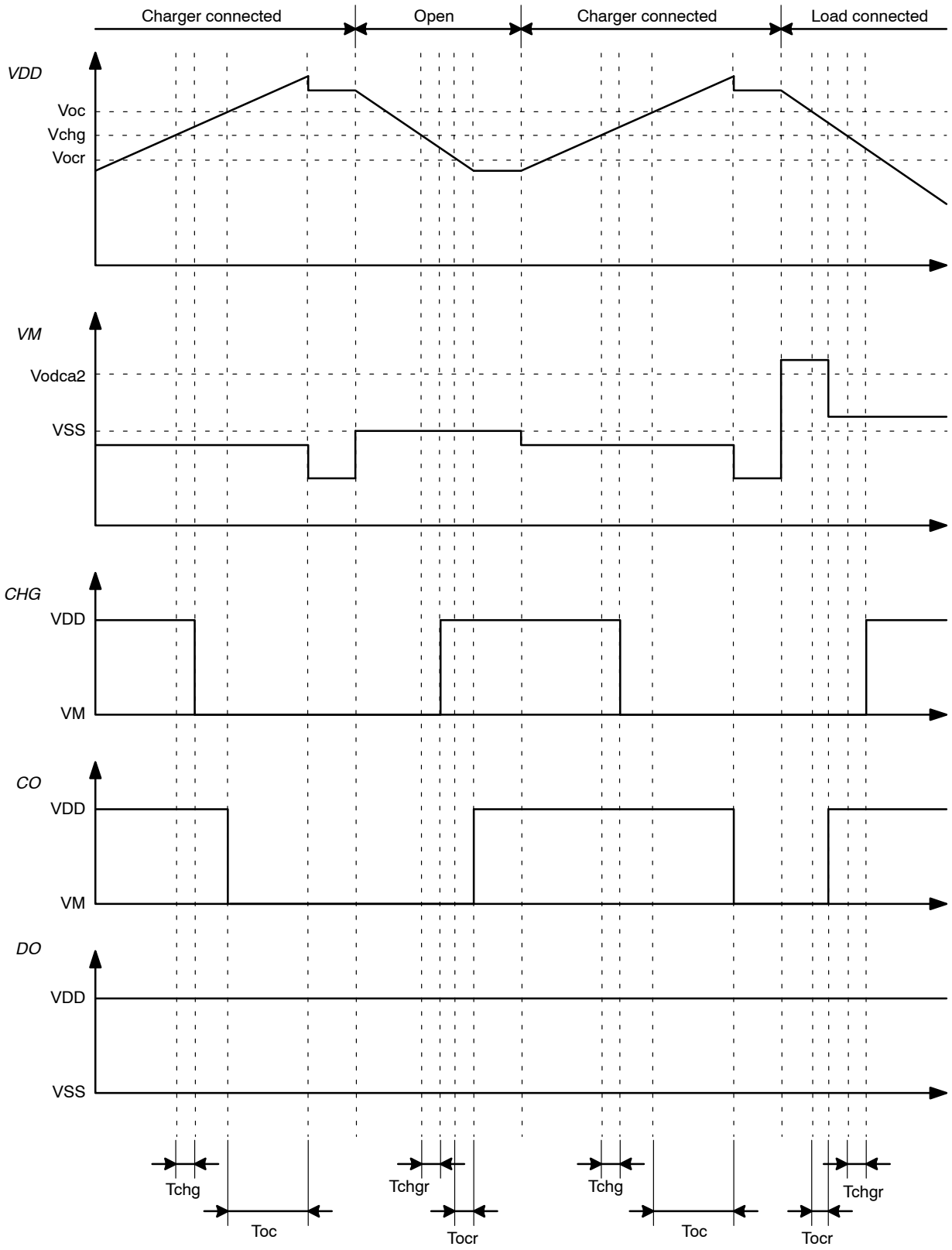


Figure 6. Over−charge Detection, Charger Alarm Detection

TIMING CHART 2

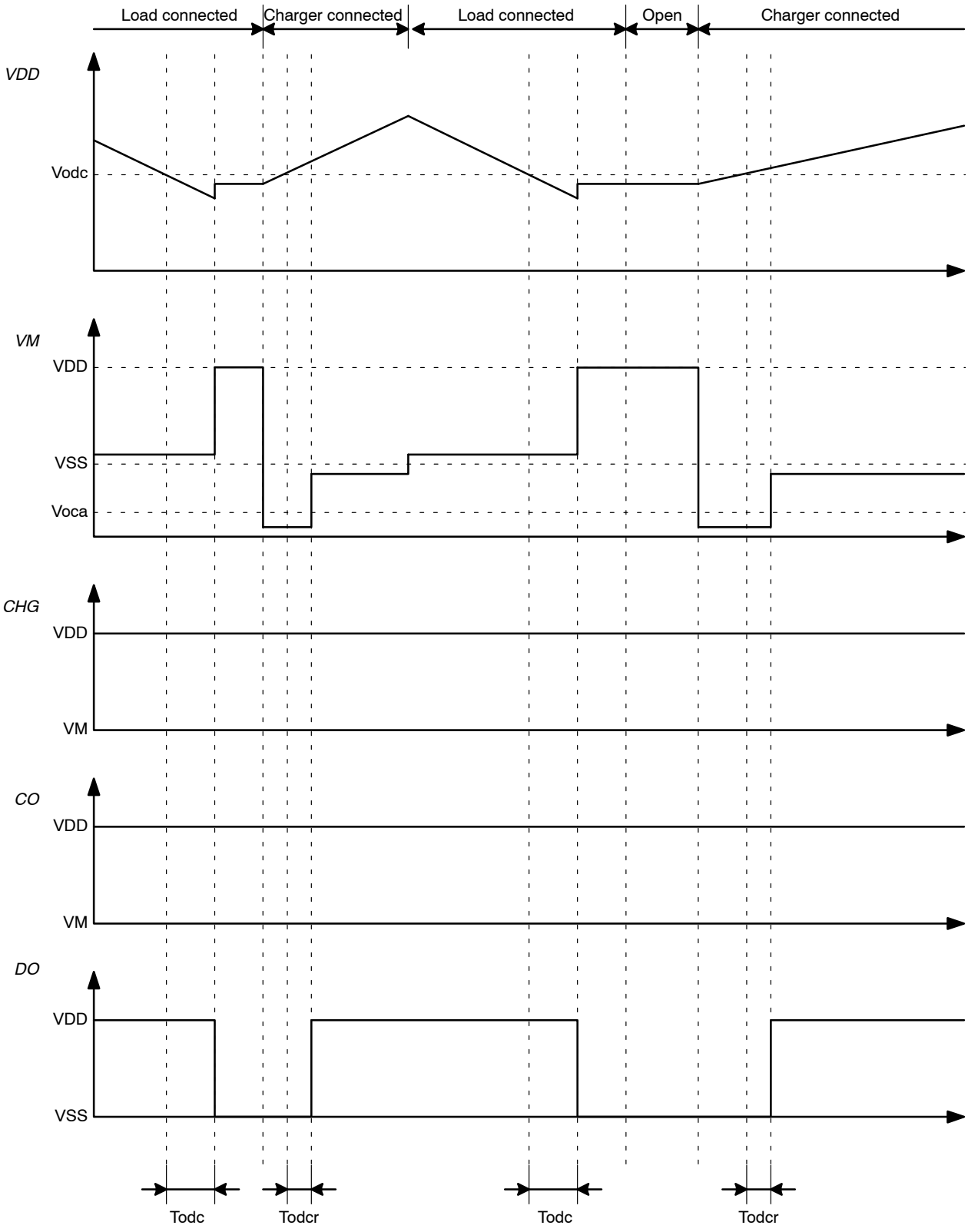


Figure 7. Over−charge Detection

TIMING CHART 3

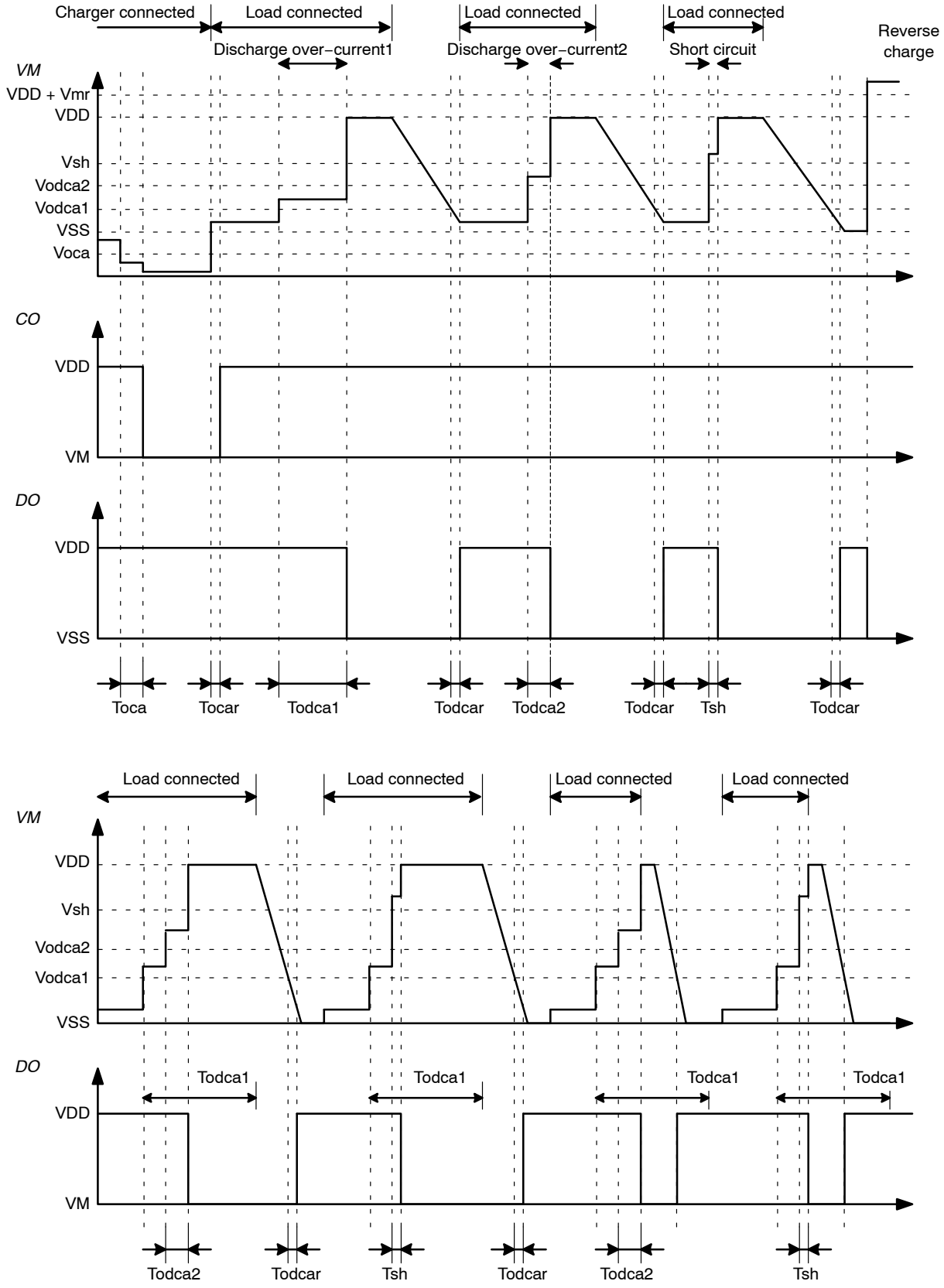


Figure 8. Charge Over−current, Discharge Over−current1 / 2, Short Circuit Detection, Reverse Charger Detection

PACKAGE

Flip−Chip
Solder ball pitch: 380 μm
Diameter: 200 μm

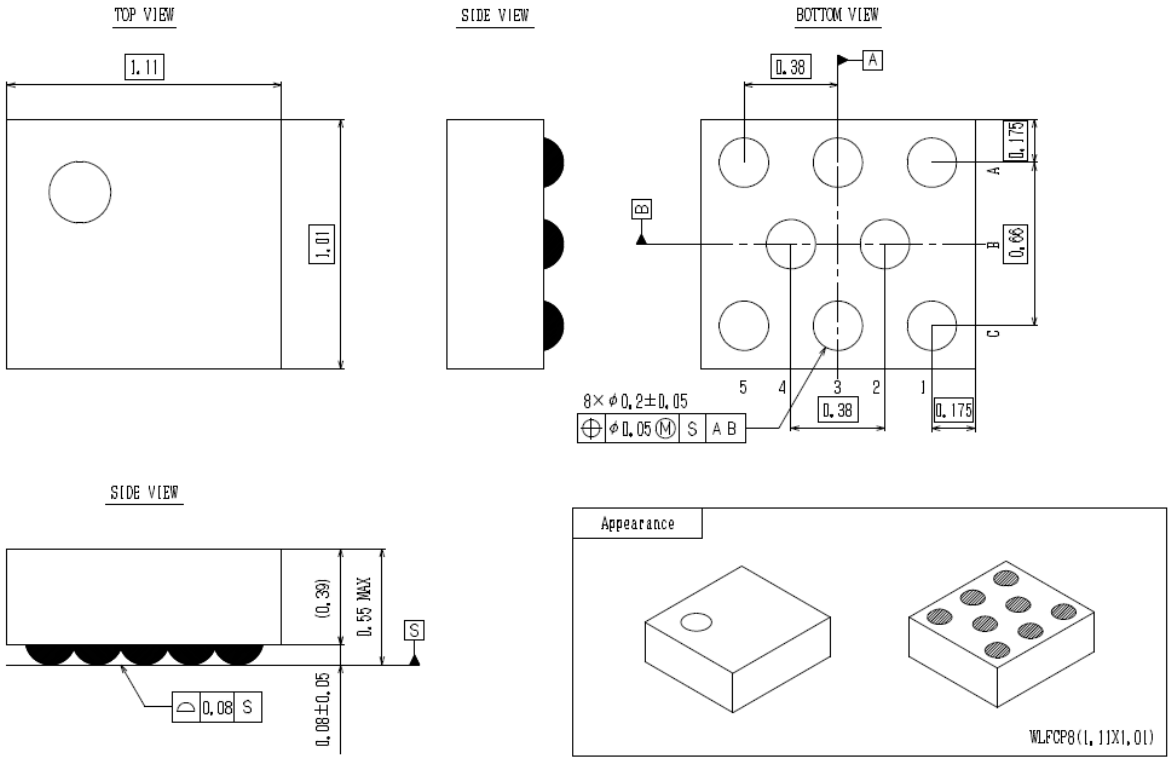


Figure 9.

PACKAGE

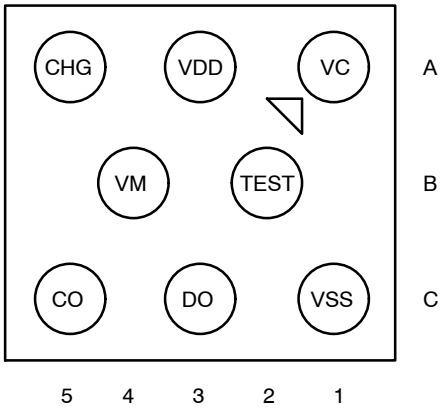


Figure 10. Bottom View (Solder Ball Side)

PIN ASSIGNMENT

	Pin Name	Pin Function
A1	VC	Negative voltage input pin of VcellH / Positive voltage input pin of VcellL
A3	VDD	Power pin/Positive voltage input pin of VcellH
A5	CHG	Charger alarm signal output pin
B2	TEST	TEST mode setting pin
B4	VM	Charger minus voltage input pin
C1	VSS	Negative voltage input pin of VcellL/GND pin
C3	DO	To be connected FET gate for discharge control
C5	CO	To be connected FET gate for charge control

BLOCK DIAGRAM

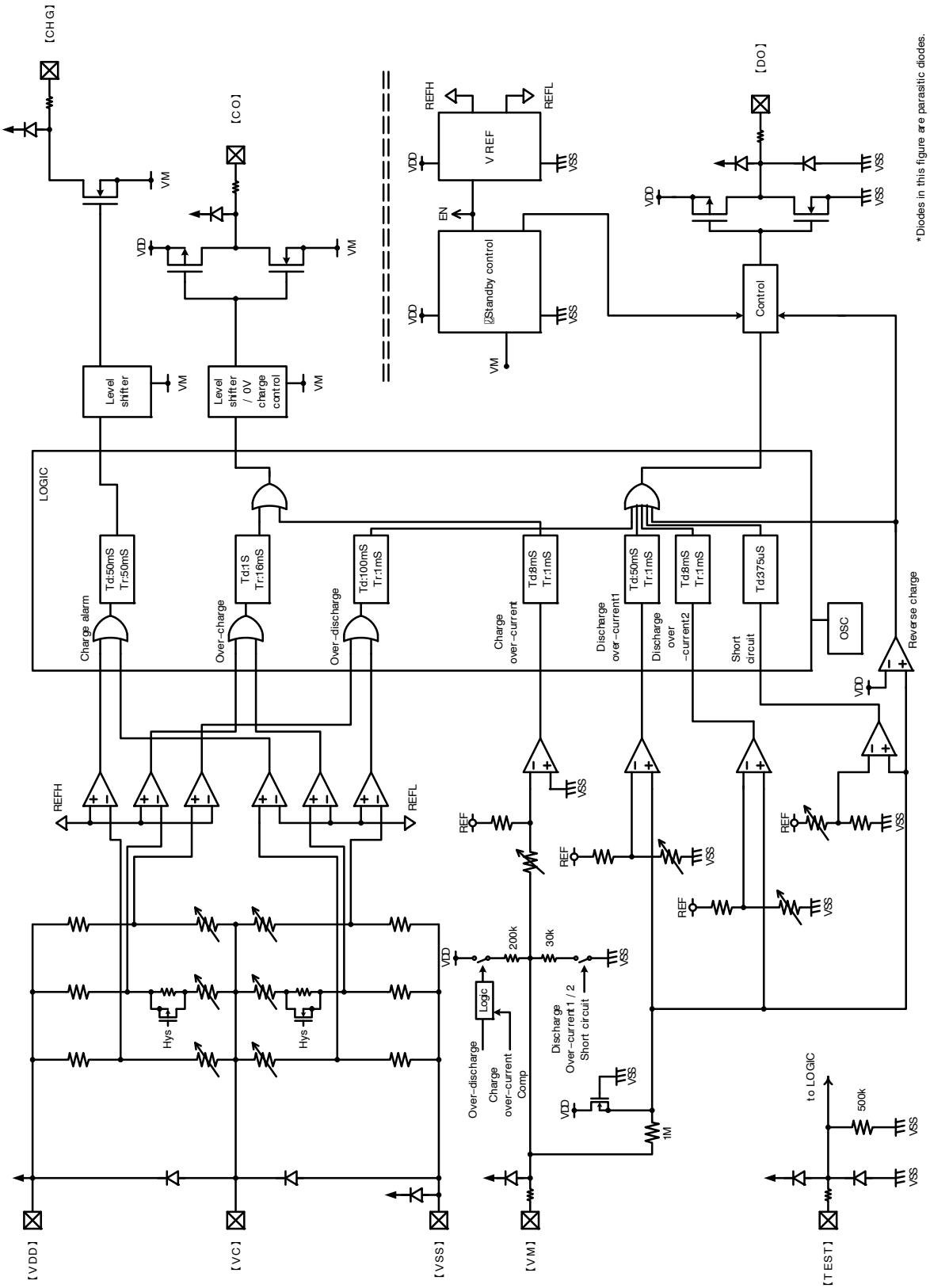


Figure 11. Block Diagram

APPLICATION CIRCUIT EXAMPLE

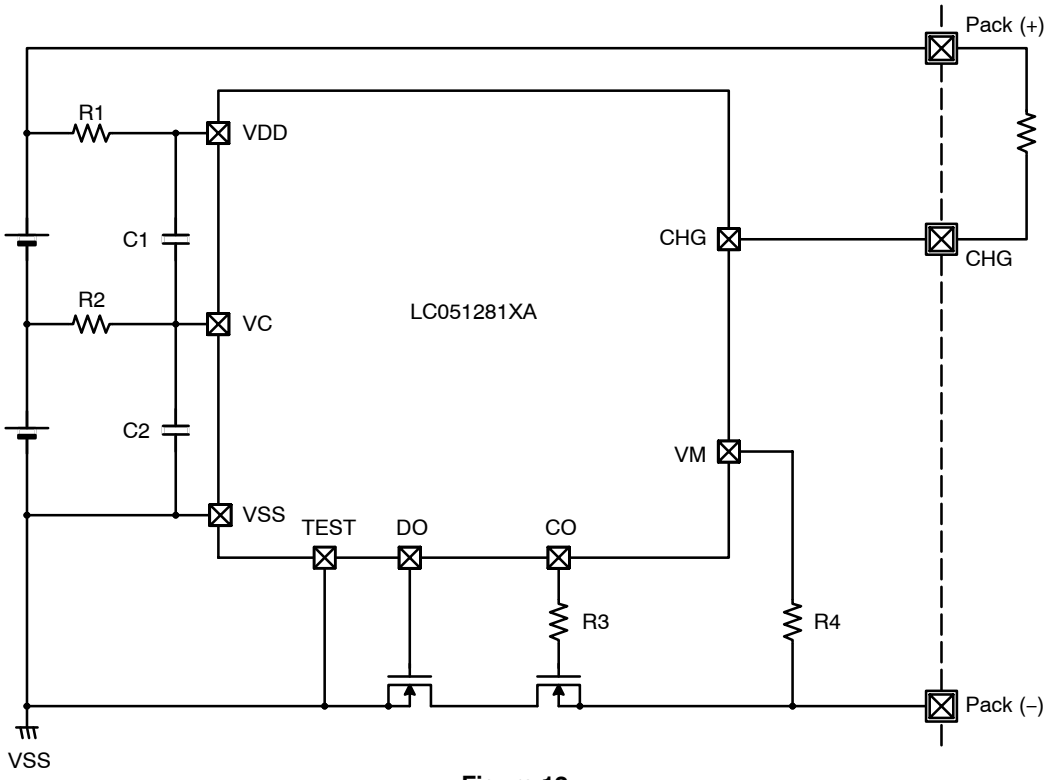


Figure 12.

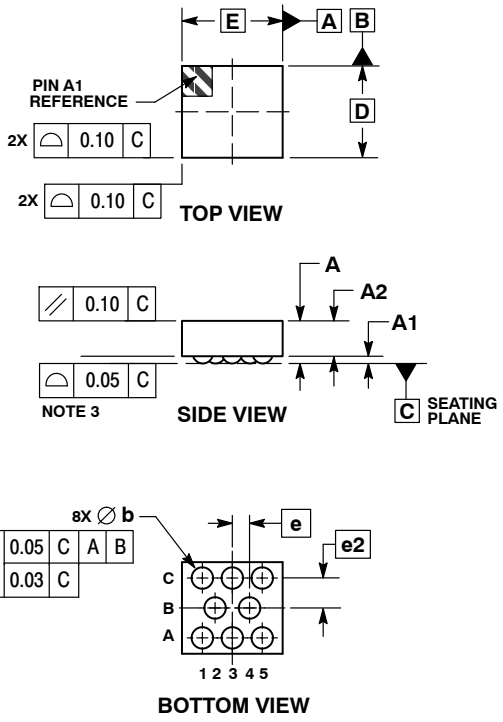
Table 2.

Items	Recommended Value	Min	Max	Unit
R1, R2	100	–	500	Ω
R3	30	20	–	kΩ
R4	2	–	4	kΩ
R5	200	–	500	kΩ
C1, C2	0.1	–	1	μF

*The characteristics of this IC under these parameters are not covered by warranty.
*TEST pin would be better to be connected to VSS.

PACKAGE DIMENSIONS

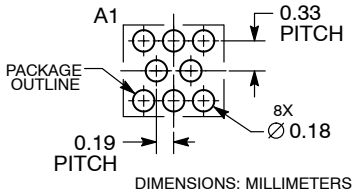
WLCSP8, 1.01x1.11
CASE 567GR
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.55
A1	0.03	0.13
A2	0.39 REF	
b	0.15	0.25
D	1.01 BSC	
E	1.11 BSC	
e	0.19 BSC	
e2	0.33 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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