LC706206CA

Product Preview

Digital MEMS Microphone Controller including Pre-amplifier and Sigma Delta Modulator and Charge Pump

ON Semiconductor®

www.onsemi.com

Description

The LC706206CA is a MOS LSI which integrates digital MEMS microphone controller function. It supplies bias voltage to external MEMS sensor and accepts analog sound signal, outputs PDM (Pulse Density Modulation) data stream.

The LC706206CA includes LDO, pre−amplifier, ADC (Analog−to Digital Converter) and charge−pump. The charge−pump generates bias voltage which is needed by the MEMS sensor. The pre−amplifier amplifies analog sound signal from the MEMS sensor and drives ADC to obtain PDM data stream.

The LC706206CA features an integrated LDO and is powered from the system supply rails up to 3.6 V, with low current consumption of 550 μA(typ) at normal operation mode (Fclk = 2.4 MHz). It also has the low power mode (Fclk = 750 kHz).

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC706206CA	Wafer (Pb−Free)	1 / Wafer Carrier

Features

- Optimized to be combined with a MEMS Sensor with 11 V Bias Voltage and −39 dBV @ 94 dBSPL Sensitivity
- Pulse Density Modulation (PDM) Output
- Standard 5−Wire Digital Interface
- 11.0 V Charge−pump Output for MEMS Sensor Bias
- +13 dB Gain (Transfer Function)
- Low Noise −90 dBFS Output makes total SNR up to 63 dB
- Low Current Consumption 550 μA(typ) at Fclk = 2.4 MHz
- Low Power Mode at Fclk = 750 kHz in which the Current Consumption 300 μA(typ)
- This is a Pb−Free Device

Applications

- Digital MEMS Microphone
- Personal Computer
- Tablet Computer
- Mobile Handset
- Headset Accessories

Block Diagram

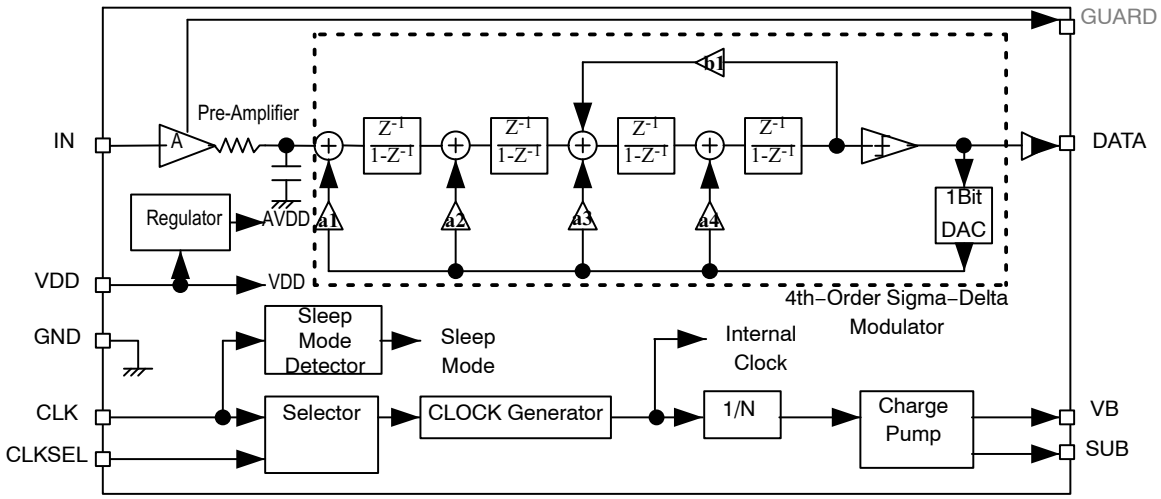


Figure 1. Block Diagram

Pad Coordinate

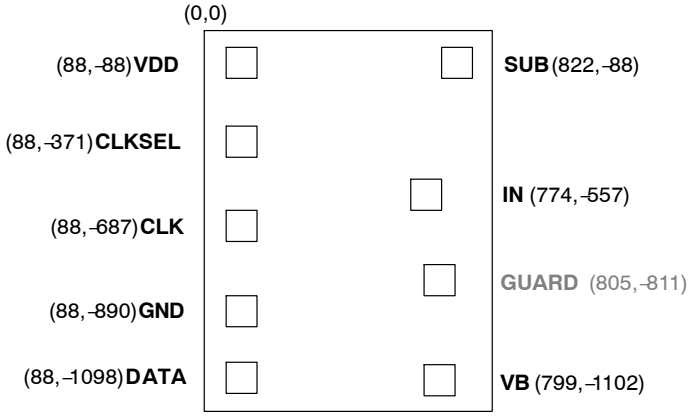


Figure 2. Pad Coordinate

Pad Size

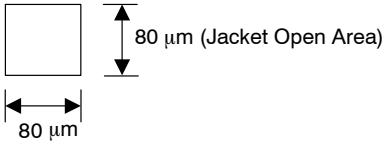


Figure 3. Pad Size

Wafer Outline

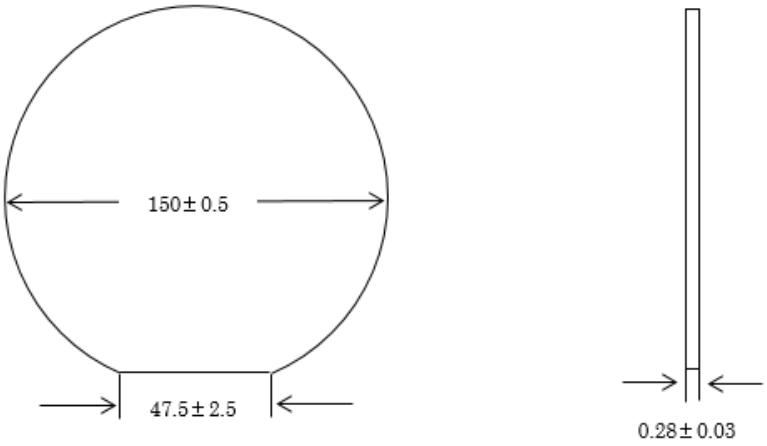


Figure 4. Wafer Outline

Table 1. ABSOLUTE MAXIMUM RATINGS at T_a = 25°C, GND = 0 V

Parameter	Symbol	Pin Name	Min	Max	Unit
Maximum power supply voltage	V_{DD} max	VDD	–0.3	+4.0	V
Maximum input voltage	V_{CLK} max	CLOCK, LR, ADJ	–0.3	V_{DD} + 0.3	V
	V_{IN} max	IN	–0.3	V_{DD} + 0.3	V
Maximum output voltage	V_O max	DATA	–0.3	V_{DD} + 0.3	V
Operating temperature range	Ta		–30	70	°C
Storage temperature range	Tstg		–40	85	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 2. CIRCUIT PARAMETERS (Note 1)

Parameter	Symbol	Pin Name	Test Condition	Min	Typ	Max	Unit
Input capacitance of die	C_{IN}	IN			0.4		pF

1. IN–Pin has a limited protection against ESD. Value of IN–Pin is proven by design.

Table 3. DC ELECTRICAL CHARACTERISTICS RATING at T_a = 25°C, V_{DD} = 1.8 V, GND = 0 V, Fclk = 2.4 MHz, Fduty = 50%

Parameter	Symbol	Pin Name	Condition	Min	Typ	Max	Unit
Power supply voltage	V_{DD}	VDD		1.64	1.8	3.6	V
Current consumption 1	IDD1	VDD	V_{DD} = 1.8 V Fclk = 3.0 MHz		550		μA
Current consumption 2	IDD2	VDD	V_{DD} = 1.8 V Fclk = 750 kHz		300		μA
Standby Current	ISTBY	VDD	V_{DD} = 3.3 V Fclk < 1 kHz			1	μA
Input/Output LOW level	Viol	CLK, DATA, CLKSEL	DATA : Iol = 0.5 mA			0.35 × V_{DD}	V
Input/Output HIGH level	Vioh	CLK, DATA, CLKSEL	DATA : Ioh = –0.5 mA	0.65 × V_{DD}			V
Charge pump voltage	Vbias	VB/SUB	V_{DD} = 3.3 V	9.66	10.5	11.34	V
Load Capacitance	Cload	DATA	V_{DD} = 1.64 V			200	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 4. AC ELECTRICAL CHARACTERISTICS DESIGN

at T_a = 25°C, V_{DD} = 1.8 V, GND = 0 V, Signal Frequency = 1 kHz, Measurement frequency = 100 Hz to 20 kHz, Fclk = 2.4 MHz, Fduty = 50%, Input capacitor = 2.5 pF, Bypass capacitor = 0.1 μF (V_{DD} − GND)

Parameter	Symbol	Pin Name	Condition	Min	Typ	Max	Unit
Clock Frequency (Normal Operation)	Fclk	CLK		0.6	2.4	3.3	MHz
Clock Frequency (Sleep Mode)	Fclk_SL	CLK				1	kHz
Clock Duty (Note 2)	Fduty	CLK		40		60	%
Over Sampling Ratio	OSR				50		
Maximum Input Voltage	Vin (Note 2)	IN	0 dBFS (= 122 dBSPL)		223.8		mVrms
THD / THD+N	THD+N_0	DATA	Vout = −2 dBFS (= 120 dBSPL) 1 kHz Sin−Wave			5	% (THD)
	THD+N_1	DATA	Vout = −5 dBFS (= 117 dBSPL) 1 kHz Sin−Wave			3	% (THD+N)
	THD+N_2	DATA	Vout = −12 dBFS (= 110 dBSPL) 1 kHz Sin−Wave			1	% (THD+N)
	THD+N_3	DATA	Vout = −28 dBFS (= 94 dBSPL) 1 kHz Sin−Wave			0.5	% (THD+N)
Digital Noise Floor	DNF_1	DATA	Fclk = 2.4 MHz A−weighted		−90.0		dBFS
	DNF_2	DATA	Fclk = 750 kHz A−weighted		−89.0		dBFS
Transfer Function (Note 3)	TF1	DATA			13.0		dB
Transfer Function vs Fclk	TF_Fclk (Note 2)	DATA		−0.1		+0.1	dB
Power Supply Rejection	PSR (Note 2)	DATA	20 Hz to 20 kHz, 100 mVp−p sine wave			−80	dBFS
Wake Up Time (Note 2)	WUT_1	DATA	−0.5 dBFS to final value			20	ms
	WUT_2	DATA	−0.2 dBFS to final value			50	ms
Fall Asleep Time (Note 2)	FAT	DATA	Fclk = 1 kHz			10	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Reference data : No measurement.
3. Each product has been designed with performance of ±0.5 dB tolerance for transfer function however it's not measured in outgoing inspection.

Table 5. PIN DESCRIPTIONS

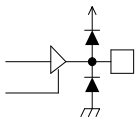
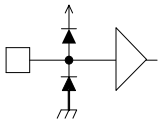
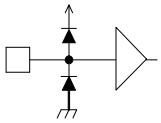
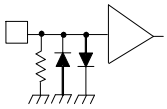
No.	Pin Name	Function	I/O	Pin Conditions
–	GND	Ground	–	–
–	VDD	Power Supply	–	–
–	GUARD	Connect to GUARD of MEMS	–	–
–	SUB	Connect to SUB of MEMS	–	–
–	DATA	PDM Data Output	Output	
–	CLKSEL	CLK Select signal input Case 1 : When CLKSEL is LOW, PDM data is outputted in sync with negative edge of CLK. Case 2 : When CLKSEL is HIGH, PDM data is outputted in sync with positive edge of CLK.	Input	
–	CLK	Clock input	Input	
–	VB	Charge Pump Voltage Output	Output	–
–	IN	Audio signal input	Input	

Table 6. SWITCHING CHARACTERISTICS

at T_a = 25°C, V_{DD} = 1.8 V, GND = 0 V, Fclk = 2.4 MHz, Fduty = 50%

Case 1: CLKSEL = LOW

Parameter	Symbol	Pin Name	Condition	Min	Typ	Max	Unit
Clock Rise Time	Tcr	CLK				10	ns
Clock Fall Time	Tcf	CLK				10	ns
Output Data Delay	Tpd_I	DATA	CL = 13 pF, RL = 1 MΩ	18		60	ns
Output Hi−Z Delay	Tpzd_I	DATA	CL = 13 pF, RL = 1 MΩ	0		16	ns

NOTE: Tpd_I > Tpzd_I

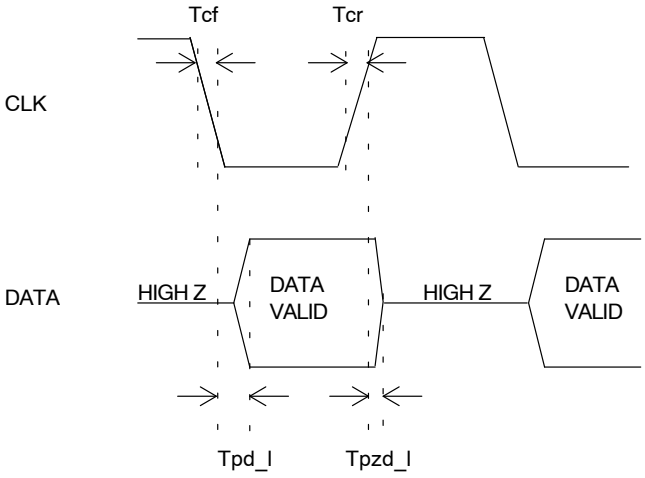


Figure 5.

Table 7. SWITCHING CHARACTERISTICS (Reference data: No measurement)
at T_a = 25°C, V_{DD} = 1.8 V, GND = 0 V, Fclk = 2.4 MHz, Fduty = 50%
Case 2: CLKSEL = HIGH

Parameter	Symbol	Pin Name	Condition	Min	Typ	Max	Unit
Clock Rise Time	Tcr	CLK				10	ns
Clock Fall Time	Tcf	CLK				10	ns
Output Data Delay	Tpd_h	DATA	CL = 13 pF, RL = 1 MΩ	18		60	ns
Output Hi−Z Delay	Tpzd_h	DATA	CL = 13 pF, RL = 1 MΩ	0		16	ns

NOTE: Tpd_h > Tpzd_h

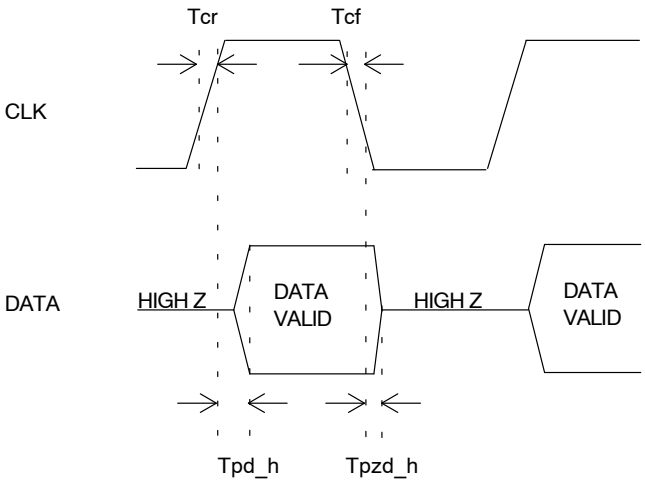


Figure 6.

PUBLICATION ORDERING INFORMATION

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