LC706210CA

Product Preview

Digital MEMS Microphone Controller including Pre-amplifier and Sigma Delta Modulator and Charge Pump

ON Semiconductor®

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Description

The LC706210CA is a MOS LSI which integrates digital MEMS microphone controller function. It supplies bias voltage to external MEMS sensor and accepts analog sound signal, outputs PDM (Pulse Density Modulation) data stream.

The LC706210CA includes LDO, pre−amplifier, ADC (Analog−to Digital Converter) and charge−pump. The charge−pump generates bias voltage which is needed by the MEMS sensor. The pre−amplifier amplifies analog sound signal from the MEMS sensor and drives ADC to obtain PDM data stream.

The LC706210CA features Gain Adjustment pad which enables sensitivity error reduction by the gain adjustment according to the deviation of MEMS sensor sensitivity. It also make the common MEMS sensor used in bottom−port structure available with top−port by the gain adjustment.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC706210CA	Wafer (Pb−Free)	1 / Wafer Carrier

Features

- Optimized to be combined with a MEMS Sensor with 13.5 V Bias and −37.5 dBV @ 94 dBSPL Sensitivity
- Pulse Density Modulation (PDM) Output
- Standard 5−Wire Digital Interface
- 13.5 V Charge−pump Output for MEMS Sensor Bias
- +11.5 dB Initial Gain (Transfer Function)
- Dedicated Gain Adjustment Pad which enables −1.5 dB or +3 dB Adjustment from the Initial Gain according to Wire Connection
- Low Noise −91 dBFS Output makes total SNR up to 64 dB
- Low Power Operation Mode
- This is a Pb−Free Device

Applications

- Digital MEMS Microphone
- Personal Computer
- Tablet Computer
- Mobile Handset
- Headset Accessories

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Publication Order Number:
LC706210CA/D

Block Diagram

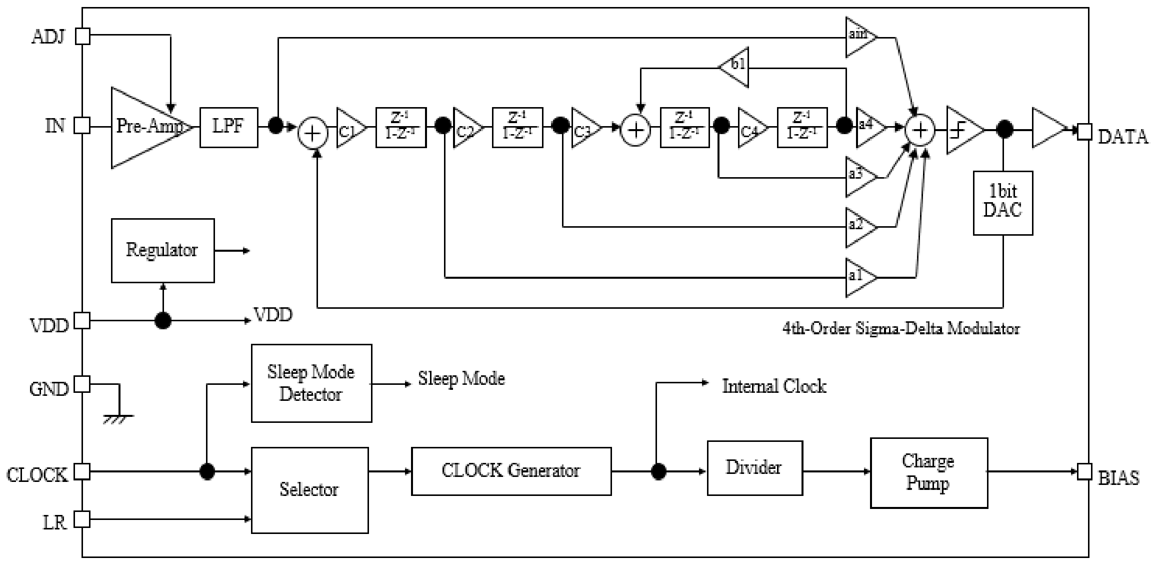
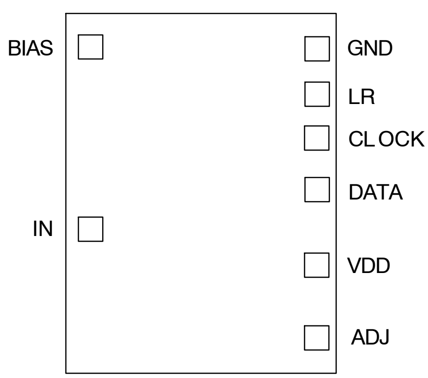


Figure 1. Block Diagram

Pad Coordinate



Die Size (distance on wafer): 1.08 x 1.48 mm

Figure 2. Pad Coordinate

Pad Size

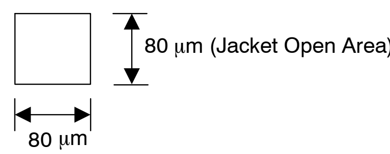


Figure 3. Pad Size

Wafer Outline

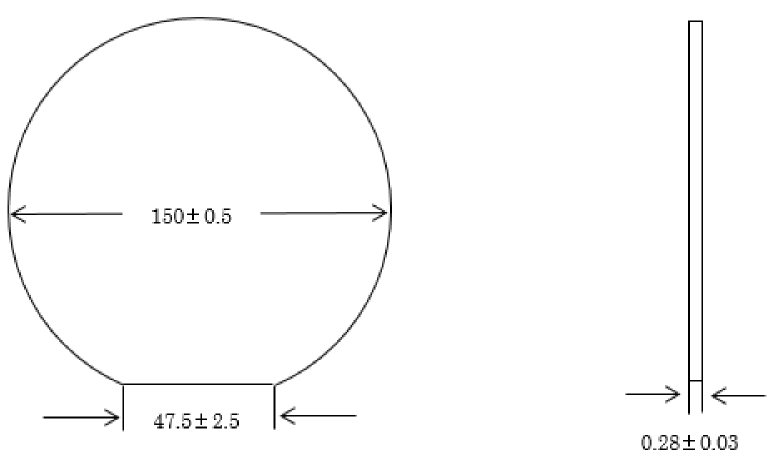


Figure 4. Wafer Outline

Table 1. ABSOLUTE MAXIMUM RATINGS at T_a = 25°C, GND = 0 V

Parameter	Symbol	Pin Name	Min	Max	Unit
Maximum power supply voltage	V_{DD} max	VDD	–0.3	+4.0	V
Maximum input voltage	V_{CLK} max	CLOCK, LR, ADJ	–0.3	V_{DD} + 0.3	V
	V_{IN} max	IN	–0.3	V_{DD} + 0.3	V
Maximum output voltage	V_O max	DATA	–0.3	V_{DD} + 0.3	V
Operating temperature range	Ta		–40	85	°C
Storage temperature range	Tstg		–40	85	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 2. CIRCUIT PARAMETERS (Note 1)

Parameter	Symbol	Pin Name	Test Condition	Min	Typ	Max	Unit
Input capacitance of die	C_{IN}	IN			0.4		pF

1. IN−Pin has a limited protection against ESD. Value of IN−Pin is proven by design.

Table 3. DC ELECTRICAL CHARACTERISTICS RATING at T_a = 25°C, V_{DD} = 1.8 V, GND = 0 V, Fduty = 50%

Parameter	Symbol	Pin Name	Condition	Min	Typ	Max	Unit
Power supply voltage	V_{DD}	VDD		1.64	1.8	3.6	V
Power consumption (Normal mode)	IDD(n)	VDD	V_{DD} = 1.8 V Fclk = 2.4 MHz		860		μA
Power consumption (Low power mode)	IDD(l)	VDD	V_{DD} = 1.8 V Fclk = 768 kHz		450		μA
Standby Current	ISTBY	VDD	V_{DD} = 3.3 V			50	μA
Input/Output LOW level	Viol	CLOCK, DATA, LR, ADJ	DATA : Iol = 0.5 mA			0.35 × V_{DD}	V
Input/Output HIGH level	Vioh	CLOCK, DATA, LR, ADJ	DATA : Ioh = –0.5 mA	0.65 × V_{DD}			V
Charge pump voltage	Vbias	BIAS	V_{DD} = 1.8 V		13.5		V
Charge Pump voltage tolerance	Tolerance	BIAS		–8		+8	%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 4. AC ELECTRICAL CHARACTERISTICS DESIGN
at T_a = 25°C, V_{DD} = 1.8 V, GND = 0 V, Signal Frequency = 1 kHz, Measurement frequency = 100 Hz to 20 kHz, Fduty = 50%, Input capacitor = 1.5 pF, Bypass capacitor = 0.1 μF (V_{DD} – GND)

Parameter	Symbol	Pin Name	Condition	Min	Typ	Max	Unit
Clock Frequency (Note 2) (Normal Operation)	Fclk	CLOCK		1	2.4	4.8	MHz
Clock Frequency (Note 2) (Low power Operation)	Fclk	CLOCK		351	768	800	kHz
Clock Frequency (Sleep Mode)	Fclk_SL	CLOCK				1	kHz
Clock Duty (Note 2)	Fduty	CLOCK		40		60	%
Over Sampling Ratio	OSR				50		
Maximum Input Voltage (Input Full Scale Voltage)	Vin	IN	0 dBFS (= 120 dBSPL)		266		mVrms
THD / THD+N	THD+N_0 (Note 2)	DATA	Vout = 0 dBFS (= 120 dBSPL) (= 167.8 mVrms) 1 kHz Sin–Wave			10	% (THD)
	THD+N_–5	DATA	Vout = –5 dBFS (= 115 dBSPL) (= 94.4 mVrms) 1 kHz Sin–Wave			1	% (THD+N)
	THD+N_–20 (Note 2)	DATA	Vout = –20 dBFS (= 100 dBSPL) (= 16.8 mVrms) 1 kHz Sin–Wave			1	% (THD+N)
Digital Noise Floor(n)	DNF_n	DATA	Bandwidth 20 kHz A–weighted, Fclk = 2.4 MHz		–91.0		dBFS
Digital Noise Floor(l)	DNF_l	DATA	Bandwidth 8 kHz A–weighted, Fclk = 768 kHz		–90.0		dBFS
Transfer function 1 (Note 3)	TF1	DATA	ADJ = open		11.5		dB
Transfer function 2 (Note 3)	TF2	DATA	ADJ = GND		10.0		dB
Transfer function 3 (Note 3)	TF3	DATA	ADJ = V_{DD}		14.5		dB
Wake Up Time (Note 2)	WUT	CLOCK	Fclk = 2.4 MHz			10	ms
Fall Asleep Time (Note 2)	FAT		Fclk = 1 kHz			10	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Reference data : No measurement.
3. Each product has been designed with performance of ±0.5 dB tolerance for transfer function however it's not measured in outgoing inspection.

Table 5. PIN DESCRIPTIONS

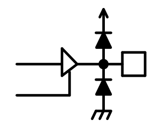
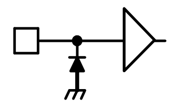
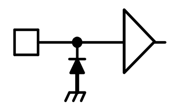
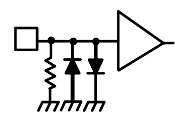
No.	Pin Name	Function	I/O	Pin Conditions
–	GND	Ground	–	–
–	VDD	Power Supply	–	–
–	DATA	PDM Data Output	Output	
–	LR	LR signal input Case 1 : When LR is LOW, PDM data is valid in sync with negative edge of CLOCK. Case 2 : When LR is HIGH, PDM data is valid in sync with positive edge of CLOCK.	Input	
–	CLOCK	Clock input	Input	
–	BIAS	Charge Pump Voltage Output	Output	–
–	IN	Audio signal input	Input	

Table 6. SWITCHING CHARACTERISTICS (Reference data: No measurement)
at T_a = 25°C, V_{DD} = 1.8 V, GND = 0 V, Fclk = 2.4 MHz, Fduty = 50%
Case 1: LR = LOW

Parameter	Symbol	Pin Name	Condition	Min	Typ	Max	Unit
Clock Rise Time	Tcr	CLOCK				10	ns
Clock Fall Time	Tcf	CLOCK				10	ns
Output Data Delay	Tpd_l	DATA	CL = 13 pF, RL = 1 MΩ	18		60	ns
Output Hi–Z Delay	Tpzd_l	DATA	CL = 13 pF, RL = 1 MΩ	0		16	ns
Delay for Data Assertion	Tdd_l	DATA		18		36	ns
Delay for Hi–Z	Tdz_l	DATA		0		4	ns

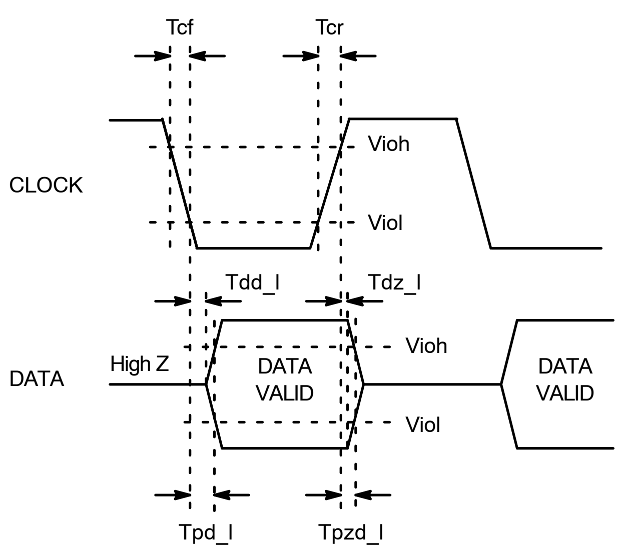


Figure 5.

Table 7. SWITCHING CHARACTERISTICS (Reference data: No measurement)
at T_a = 25°C, V_{DD} = 1.8 V, GND = 0 V, Fclk = 2.4 MHz, Fduty = 50%
Case 2: LR = HIGH

Parameter	Symbol	Pin Name	Condition	Min	Typ	Max	Unit
Clock Rise Time	Tcr	CLOCK				10	ns
Clock Fall Time	Tcf	CLOCK				10	ns
Output Data Delay	Tpd_h	DATA	CL = 13 pF, RL = 1 MΩ	18		60	ns
Output Hi−Z Delay	Tpzd_h	DATA	CL = 13 pF, RL = 1 MΩ	0		16	ns
Delay for Data Assertion	Tdd_h	DATA		18		36	ns
Delay for Hi−Z	Tdz_h	DATA		0		4	ns

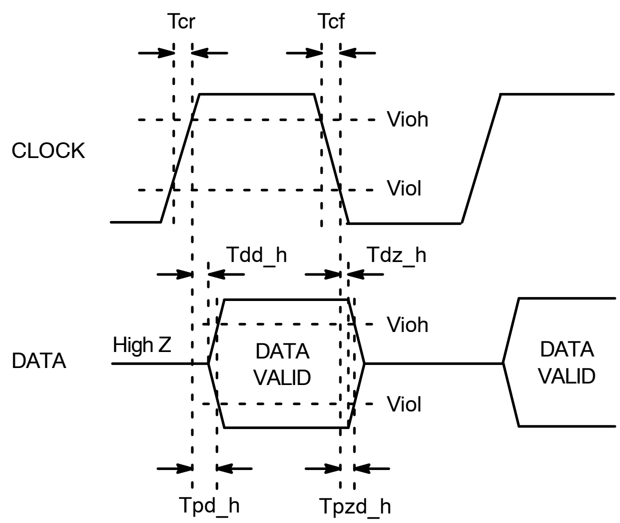


Figure 6.

NOTE: Electrical information may be based on testing done on packaged devices. The packaging or device mounting may affect the electrical performance of the device; customers are responsible for verifying device performance and reliability after assembly, and the customer is responsible for the yield of the assembly process.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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