LC709250F

16-Bit 1-Chip Microcontroller

CMOS LSI
ROM 12K byte, RAM 256 byte on−chip

ON Semiconductor®

www.onsemi.com

WLCSP9
XE SUFFIX
CASE 567JH

MARKING DIAGRAM

25001 = Specific Device Code
Y = Year
M = Month Code
XXX = Lot Number

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Overview

The LC709250F is a 16−bit microcontroller that, centered around an Xstormy16 CPU, integrates on a single chip a number of hardware features such as 12K−byte flash ROM (onboard programmable), 256−byte RAM, two 16−bit timers, a base timer, a slave IIC/synchronous SIO interface, a 2−channel 12−bit resolution AD converter, a watchdog timer, a system clock frequency divider, a 13−source (8 modules) 7−vector interrupt feature. LC709250F is available in a small package realizing the industries smallest PCB footprint for the complete solution.

Features

- X stormy16 CPU
  - 4G−byte address space
  - General−purpose registers: 16 bits x 16 registers
- Flash ROM
  - Capable of onboard programming with a wide range of voltage levels
  - Block−erasable in 128 byte units
  - Data written in 2−byte units
  - LC709250F: 12288 x 8 bits
  - (LC709250D with on−chip debugger: 32768 x 8 bits)
- RAM
  - LC709250F: 256 x 8 bits
    (LC709250D with on−chip debugger: 1024 x 8 bits)
- Minimum instruction cycle time (tCYC)
  - 31.0 us (32 kHz)
  - 1.0 us (1.0 MHz)
  - 160 ns (6 MHz)
- Ports
  - General purpose I/O ports:
    5 (P00, P01, P02, P10, P11)
  - TEST pin: 1 (TEST)
  - Power pins: 2 (VSS, VDD)
- Timers
  - Timer 0: 16−bit timer that supports PWM/toggle outputs
    1. 5−bit pre−scaler
    2. 8−bit PWM, 8−bit timer + 8−bit PWM mode selectable
    3. Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator
- Timer 1: 16−bit timer with capture registers
  - 5−bit pre−scaler
  - May be divided into 2 channels of 8−bit timer
  - Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator
- Base Timer
  1. Clock may be selected from frequency−divided output of system clock, OSC0.
  2. Interrupt can be generated in 7 timing schemes
- Serial interfaces
  - SLIIC0: Slave IIC/8−bit synchronous SIO
    Mode 0: IIC slave mode communication
    Mode 1: Synchronous 8−bit serial I/O (MSB first)
- AD Converter
  - 12/8 bits resolution selectable
  - Analog input: 2 channels
  - Comparator mode
- Watchdog timer
  - Driven by the base timer + internal watchdog timer dedicated counter
  - Interrupt or reset mode selectable
- Internal Reset Function
  - Power−on reset (POR) function

April, 2018 − Rev. 0
Publication Order Number:
LC709250F/D

1. POR reset is generated only at power−on time.

- Interrupts (peripheral function)
  - 13 sources (8 modules), 7 vector addresses
    1. Provides three levels (low(L), high(H), and highest(X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
    2. When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Interrupt Source
1	08000H	Watchdog timer (1)
2	08004H	Base timer (2)
3	08008H	Timer 0 (2)
4	08018H	Timer 1 (2)
5	0801CH	SLIIC0 (1) / Port 1 (2)
6	08030H	ADC (1)
7	0803CH	Port 0 (2)

  - 3 priority levels selectable
  - Of interrupts of the same level, the one with the smallest vector address takes precedence
  - A number enclosed in parentheses denotes the number of sources
- Interrupts (exception processing)
  - 5 sources, 1 vector address
    1. Interrupts of this type are enabled or disabled through the exception interrupt control register (EXCPL and EXCPH) and not affected by the global enable flag.
    2. Exception processing interrupts take precedence over interrupts that are generated by any of the peripheral functions. Consequently, no interrupt request is accepted while an exception processing interrupt is being processed.

No.	Vector Address	Interrupt (Exception Processing)
1	08080H	Exception processing (5)

  - The number enclosed in parentheses indicates the number of interrupt sources.
- Subroutine Stack: 256 byte RAM area
  - Subroutine calls that automatically save PSW, interrupt vector calls: 6 bytes
  - Subroutine calls that do not automatically save PSW: 4 bytes
- Multiplication / division instructions
  - 16 bits x 16 bits (4 tCYC execution time)
  - 16 bits / 16 bits (18 to 19 tCYC execution time)
  - 32 bits / 16 bits (18 to 19 tCYC execution time)
- Oscillator circuits
  - RC oscillator circuit (internal): for system clock (1.0 MHz)
  - RC oscillator circuit (for OSC1): for system clock (6.0 MHz)
  - RC oscillator circuit (for OSC0): for system clock (32 kHz)
  - SLRC oscillator circuit (internal): for system clock (in the case of exception processing)
- System clock divider function
  - Can run on low current
  - 1/1 to 1/128 of the system clock frequency can be set
- Standby function
  - HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation
    1. Oscillation is not halted automatically
    2. Released by a system reset or occurrence of an interrupt
  - HOLD mode: Suspends instruction execution and the operation of the peripheral circuits
    1. RC and OSC0 oscillators automatically stop
    2. There are way of releasing the HOLD mode
       (1) Having an interrupt source established at port 0
  - HOLDX mode: Suspends instruction execution and the operation of the peripheral circuits except those which run on OSC0
    1. OSC1 and RC oscillations automatically stop
    2. OSC0 maintains the state that is established when the HOLDX mode is entered
    3. There are way of releasing the HOLDX mode
       (1) Having an interrupt source established at Port 0 and Port 1.
       (2) Base timer interrupt
- Package form
  - WLCSP9, 1.60 × 1.76: Pb−Free and Halogen Free type
- Development tools
  - On−chip debugger: EOCUIF2 + LC709250D Package form

ORDERING INFORMATION

Device	Package	Shipping†
LC709250FXE−01MH	WLCSP9, 1.60x1.76 (Pb−Free / Halogen Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

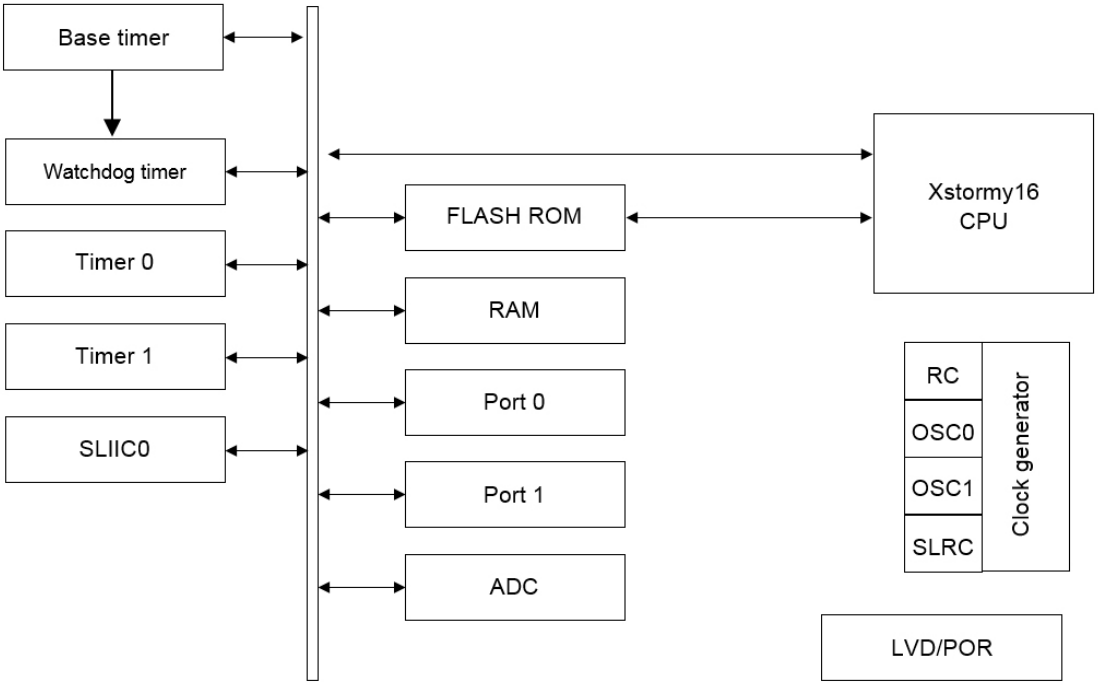


Figure 1. System Block Diagram

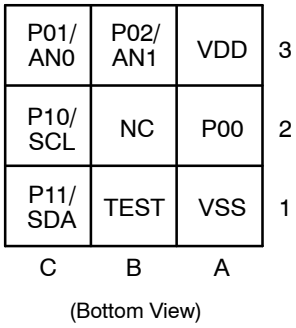


Figure 2. Pin Assignment

Table 1. PIN FUNCTION

WLCSP9	Pin Name	I/O	Port type	Description
1B	TEST	I	–	Connect this pin to V_{SS}.
1A	V_{SS}	–	–	GND pin.
3A	V_{DD}	–	–	Power supply pin.
2A	P00	I/O	Type−1	GPIO. HOLD release input. Port 0 interrupt input.
3B	P02/AN1	I/O	Type−2	GPIO. AD converter input port. Pull−up resistor.
3C	P01/AN0	I/O	Type−2	GPIO. AD converter input port. Pull−up resistor. HOLD release input. Port 0 interrupt input.
1C	P11/SDA	I/O	Type−1	GPIO. I^2C Data pin. Pull−up must be done externally as SDA. HOLD release input. Port 1 interrupt input.
2C	P10/SCL	I/O	Type−1	GPIO. I^2C Clock pin. Pull−up must be done externally as SCL. HOLD release input. Port 1 interrupt input.
2B	NC	–	–	Connect this pin to V_{SS}.

Port Block diagram

Type−1 (Open drain)

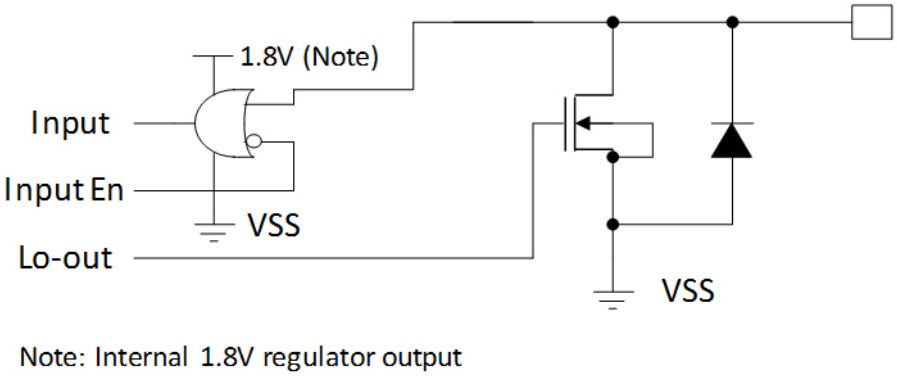


Figure 3. Type 1 Port Block Diagram

Type−2

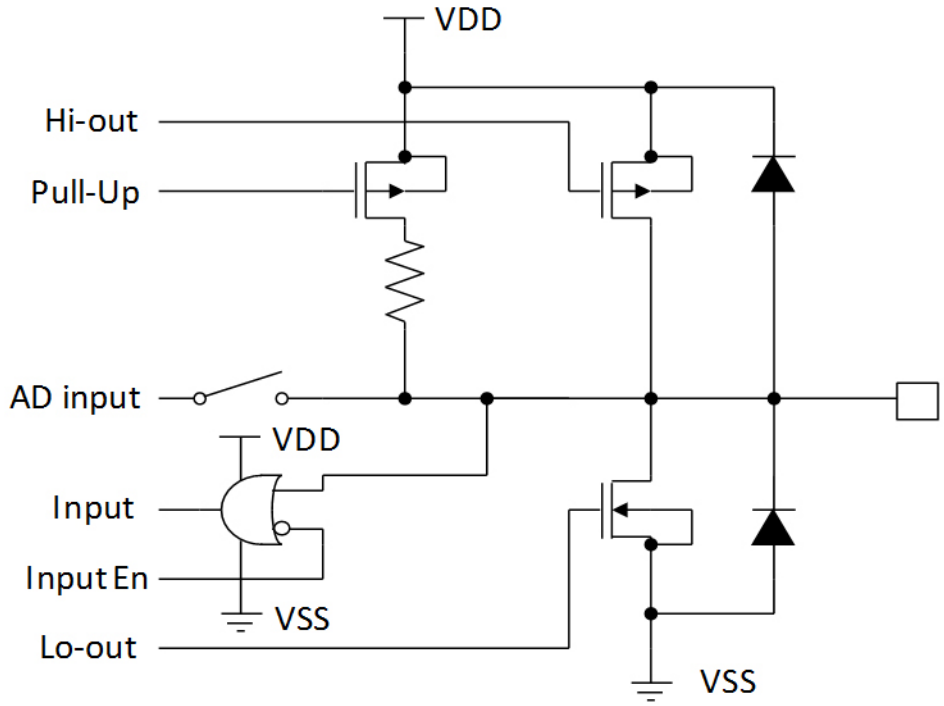


Figure 4. Type 2 Port Block Diagram

Table 2. ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Pin/Remarks	Conditions		Specification			Unit
				V_{DD} [V]	Min	Typ	Max	
Maximum supply voltage	V_{DD} max	V_{DD}			−0.3		+6.5	V
Input voltage	V_I max (1)	P01/AN0, P02/AN1			−0.3		V_{DD} +0.3	
Input/output voltage	V_I max (2)	P00, P10/SCL, P11/SDA			−0.3		+6.5	
Allowable power dissipation	Pd max		Ta = −40 to +85°C				60	mW
Operating ambient temperature	Topr				−40		+85	°C
Storage ambient temperature	Tstg				−55		+125	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. ALLOWABLE OPERATING CONDITIONS (T_A = −40°C to 85°C, V_{SS} = 0 V)

Parameter	Symbol	Pin/Remarks	Conditions		Specification			Unit
				V_{DD} [V]	Min	Typ	Max	
Operating supply voltage	V_{DD}	V_{DD}			2.5		4.5	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS (T_A = −40 to +85°C, V_{SS} = 0 V, Typ: 3.5 V)

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD} [V]	Specification			Unit
					Min	Typ	Max	
INPUT / OUTPUT								
High level input voltage	V_{IH} (1)	P01/AN0, P02/AN1		2.5 to 4.5	0.7V_{DD}		V_{DD}	V
	V_{IH} (2)	P00, P10/SCL, P11/SDA			1.4			
Low level input voltage	V_{IL} (1)	P01/AN0, P02/AN1			V_{SS}		0.25V_{DD}	
	V_{IL} (2)	P00, P10/SCL, P11/SDA					0.5	
High level input current	I_{IH} (1)	P00 to P02, P10 to P11	V_{IN} = V_{DD} (including output transistor off leakage current)				1	μA
Low level input current	I_{IL} (1)	P00 to P02, P10 to P11	V_{IN} = V_{SS} (including output transistor off leakage current)		−1			
High level output voltage	V_{OH} (1)	P01/AN0, P02/AN1	I_{OH} = −0.4 mA	3.0 to 4.5	V_{DD}−0.4			V
	V_{OH} (2)		I_{OH} = −0.2 mA	2.5 to 4.5	V_{DD}−0.4			
Low level output voltage	V_{OL} (1)	P00 to P02, P10 to P11	I_{OL} = 3.0 mA	3.0 to 4.5			0.4	
	V_{OL} (2)		I_{OL} = 1.3 mA	2.5 to 4.5			0.4	
Pull−up resistor	Rpu	P01/AN0, P02/AN1	V_{OH} = 0.9 V_{DD}	2.5 to 4.5		35		kΩ

Table 4. ELECTRICAL CHARACTERISTICS (T_A = −40 to +85°C, V_{SS} = 0 V, Typ: 3.5 V)

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD} [V]	Specification			Unit
					Min	Typ	Max	
CONSUMPTION CURRENT								
Normal mode	IDDOP(1)	V_{DD}	Internal 6MHz RC oscillator 1/1 frequency division mode	2.5 to 4.5		2.7		mA
	IDDOP(2)		Internal 1MHz RC oscillator 1/1 frequency division mode			1.0		
	IDDOP(3)		Internal 32kHz RC oscillator 1/1 frequency division mode			20		μA
HALT mode	IDDHALT(1)		Internal 6MHz RC oscillator 1/1 frequency division mode			0.65		mA
	IDDHALT(2)		Internal 1MHz RC oscillator 1/1 frequency division mode			0.25		
	IDDHALT(3)		Internal 32kHz RC oscillator 1/1 frequency division mode			4.5		μA
HOLD mode	IDDHOLD(1)					1		
HOLDX mode	IDDHOLD(2)		Internal 32kHz RC oscillator			2		
POWER ON RESET								
Reset release voltage	V_{RR}	V_{DD}					2.4	V
INTERNAL OSCILLATOR								
6 MHz RC frequency	F_{HRC}			2.5 to 4.5	4	6	10	MHz
1 MHz RC frequency	F_{MRC}				0.5	1	2.2	
32 KHz RC frequency	F_{LRC}		T_A = −20 to 70°C		30.4	32	33.6	kHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. I^2C SLAVE CHARACTERISTICS (T_A = −40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD} [V]	Specification		Unit
					Min	Max	
Clock frequency	TSCL	P10/SCL		2.5 to 4.5		400	kHz
Bus free time between STOP condition and START condition	TBUF	P10/SCL, P11/SDA	See Figure 5		1.3		μs
Hold time (repeated) START condition First clock pulse is generated after this interval	THD:STA	P10/SCL, P11/SDA	See Figure 5		0.6		μs
Repeated START condition set-up time	TSU:STA	P10/SCL, P11/SDA	See Figure 5		0.6		μs
STOP condition setup time	TSU:STO	P10/SCL, P11/SDA	See Figure 5		0.6		μs
Data hold time	THD:DAT	P10/SCL, P11/SDA	See Figure 5		0	0.9	μs
Data setup time	TSU:DAT	P10/SCL, P11/SDA	See Figure 5		100		ns
Clock low period	TLOW	P10/SCL	See Figure 5		1.3		μs
Clock high period	THIGH	P10/SCL	See Figure 5		0.6		μs
Clock/data fall time	TF	P10/SCL, P11/SDA			20 + 0.1C_B	300	ns
Clock/data rise time	TR	P10/SCL, P11/SDA			20 + 0.1C_B	300	ns

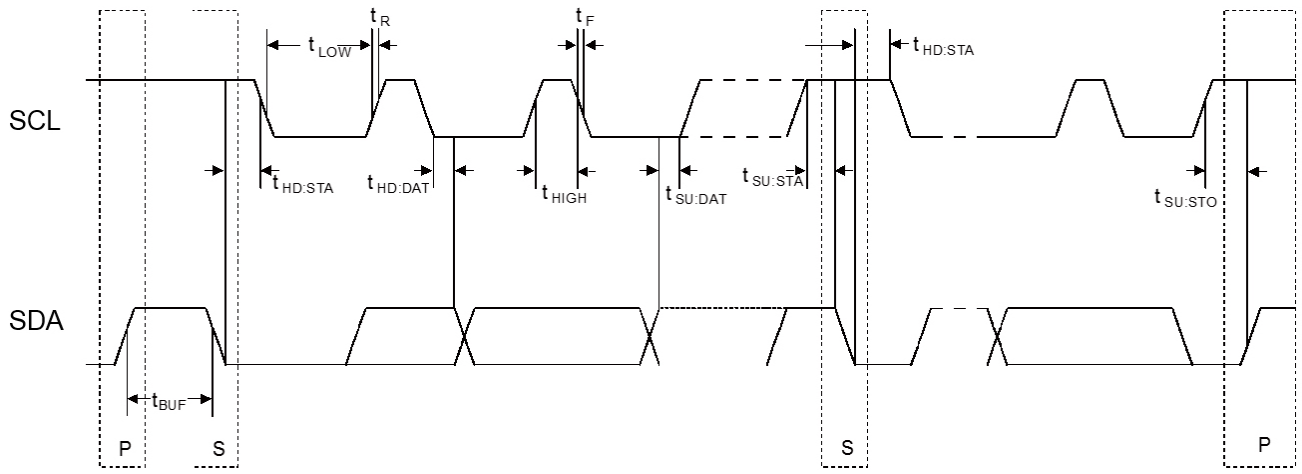


Figure 5. I²C Timing Diagram

Table 6. AD CONVERTER CHARACTERISTICS (T_A = −40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Applicable Pin /Remarks	Conditions	VDD[V]	Specification			
					Min	Typ	Max	Unit
12−BIT AD CONVERSION MODE								
Resolution	NAD	P01/AN0, P02/AN1		2.5 to 4.5		12		bit
Absolute accuracy	ETAD		(Note 1)				±16	LSB
Conversion time	TCAD12		Conversion time calculated (Note 2)			555		μs
Analog input voltage range	VAIN				VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD				1	μA
	IAINL		VAIN=VSS		-1			
$TCAD12 = \left(\frac{52}{\text{AD division ratio}} + 2\right) \times tCYC$								
8−BIT AD CONVERSION MODE								
Resolution	NAD	P01/AN0, P02/AN1		2.5 to 4.5		8		bit
Absolute accuracy	ETAD		(Note 1)				±1.5	LSB
Conversion time	TCAD8		Conversion time calculated (Note 2)			342		μs
Analog input voltage range	VAIN				VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD				1	μA
	IAINL		VAIN=VSS		−1			
$TCAD8 = \left(\frac{32}{\text{AD division ratio}} + 2\right) \times tCYC$								

1. The quantization error (±1/2LSB) is excluded from the absolute accuracy.
2. 1/64 division ratio of AD converter is recommended when OSC1 (6.0 MHz) is selected as the system clock and the System clock frequency division is 1/1.

Table 7. F−ROM PROGRAMMING CHARACTERISTICS (T_A = +10 to +55°C, V_{SS} = 0 V)

Parameter	Symbol	Applicable Pin/Remarks	Conditions		Specification			
				V_{DD} [V]	Min	Typ	Max	Unit
Onboard programming current	IDDFW (1)	V_{DD}	Total current: IDDOP + IDDFW	2.7 to 4.5			10	mA
Onboard programming time	tFW (1)		2K−byte erase operation	2.7 to 4.5			25	ms
	tFW (2)		2−byte programming operation	2.7 to 4.5			45	μs

Power Pin Treatment Condition

Connect capacitor that meets the following condition between the VDD and VSS pins. The capacitor is placed with the shortest possible lead wires.

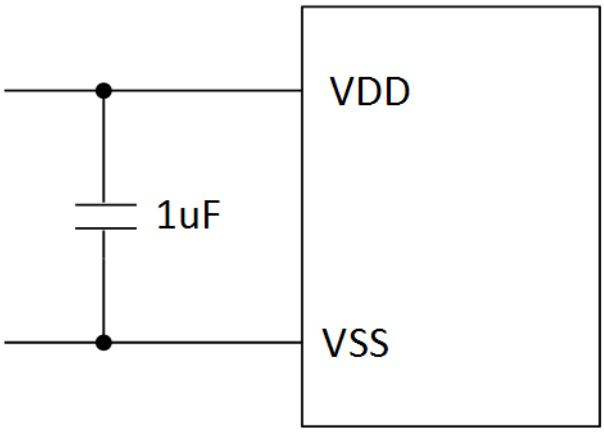
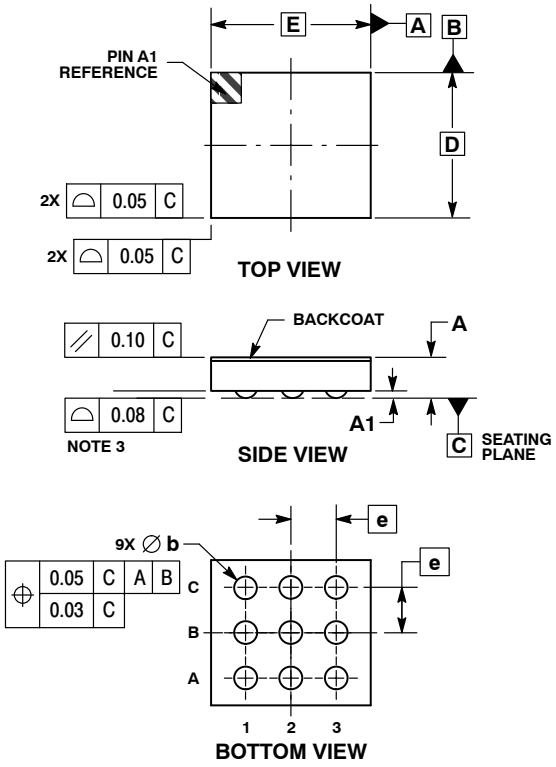


Figure 6. Power Pin Treatment

PACKAGE DIMENSIONS

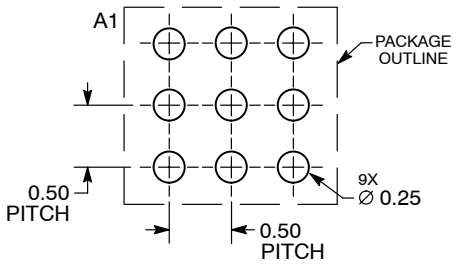
WLCSP9, 1.60x1.76
CASE 567JH
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.51
A1	0.09	0.19
b	0.20	0.30
D	1.60 BSC	
E	1.76 BSC	
e	0.50 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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