LC79401KNC

Dot-Matrix LCD Drivers

CMOS LSI

ON Semiconductor®

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The LC79401KNC is a 80-outputs segment driver LSI for graphic dot-matrix liquid crystal display systems. The LC79401KNC latches 80 bits of display data sent from a controller using a 4-bit parallel transfer technique and generates LCD drive signals. When combined as a kit with common driver, either the LC79430KNC, the LC79401KNC can drive large screen LCD panels.

Features

- Incorporates LCD Drive Circuits for 80 bits of Display
- Supports Display Duties from 1/64 to 1/256
- The Provision of a Chip Disable Pin Supports Power Reduction in Large-scale Panels
- Allows External Provision of the Bias Power Supply
- Data Transfer Clock: 6.0 MHz (max), Bidirectional Shifting Supported
- Operating Supply Voltage/Operating Temperature
  V_{DD} (Logic Block): 2.7 to 5.5 V/−20 to +85°C
  $V_{DD}-V_{EE}$ (LCD Block): 12 to 32 V/−20 to +85°C
- Data Input: 4-bit Parallel Input
- CMOS Process
- Package: Bare Chip

The electrical characteristics values shown below are for devices packaged in the plastic package.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C ±2°C, V_{SS} = 0 V)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD} max	Maximum Supply Voltage (Logic)		−0.3 to +7.0	V
$V_{DD}-V_{EE}$ max	Maximum Supply Voltage (LCD)	(Note 1)	0 to 35	V
V_I max	Maximum Input Voltage		−0.3 to V_{DD} + 0.3	V
T_{stg}	Storage Temperature		−40 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. $V_{DD} \geq V1 > V3 > V4 > V_{EE}$, $V_{DD}-V3 \leq 7$ V, $V4-V_{EE} \leq 7$ V.

ALLOWABLE OPERATING RANGES (T_A = −20 to +85°C, V_{SS} = 0 V)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	Supply Voltage (Logic)			2.7	–	5.5	V
$V_{DD}-V_{EE}$	Supply Voltage (LCD)	(Notes 2, 3)		12	–	32	V
V_{IH}	Input High Level Voltage	DI1 to 4, CP, LOAD, CDI, R/L, M, $\overline{DISPOFF}$		0.8 V_{DD}	–	–	V
V_{IL}	Input Low Level Voltage	DI1 to 4, CP, LOAD, CDI, R/L, M, $\overline{DISPOFF}$		–	–	0.2 V_{DD}	V
f_{CP}	CP Shift Clock	CP		–	–	6.0	MHz
t_{WC}	CP Pulse Width	CP		50	–	–	ns
t_{WL}	LOAD Pulse Width	LOAD		50	–	–	ns
t_{SETUP}	Setup Time	DI1 to 4 → CP		30	–	–	ns
t_{HOLD}	Hold Time	DI1 to 4 → CP	V_{DD} = 2.7 to 4.5 V	40	–	–	ns
			V_{DD} = 4.5 to 5.5 V	30	–	–	ns
t_{CL}	CP → LOAD	CP → LOAD		80	–	–	ns

ALLOWABLE OPERATING RANGES (T_A = −20 to +85°C, V_{SS} = 0 V) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{LC1}	LOAD → CP	LOAD → CP		110	–	–	ns
t_{LC2}		LOAD → CP	V_{DD} = 2.7 to 4.5 V	30	–	–	ns
			V_{DD} = 4.5 to 5.5 V	15	–	–	ns
t_R	CP and LOAD Rise Time	CP, LOAD		–	–	(Note 4)	ns
t_F	CP and LOAD Fall Time	CP, LOAD		–	–	(Note 4)	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. $V_{DD} \geq V1 > V3 > V4 > V_{EE}$, $V_{DD}-V3 \leq 7$ V, $V4-V_{EE} \leq 7$ V.
3. When the power is turned on, either the logic system power must be turned on before the LCD drive system power or else they must both be turned on at the same time. When the power is turned off, either the LCD drive system power must be turned off before the logic system power, or else both must be turned off at the same time.
4. The CP and LOAD rise time(t_R) and the CP and LOAD fall time(t_F) must satisfy equations (1) and (2) below at the same time.

$$t_{R,}t_F < \frac{1}{2\,f_{CP}} - t_{WC} \quad \text{(eq. 1)}$$

$$t_{R,}t_F < 50\ \text{ns} \quad \text{(eq. 2)}$$

ELECTRICAL CHARACTERISTICS (T_A = +25°C ±2°C, V_{DD} = 2.7 to 5.5 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IH}	Input High Level Current	$V_{IN} = V_{DD}$; LOAD, CP, CDI, R/L, DI1 to 4, M, $\overline{\text{DISPOFF}}$	–	–	1	μA
I_{IL}	Input Low Level Current	$V_{IN} = V_{SS}$; LOAD, CP, CDI, R/L, DI1 to 4, M, $\overline{\text{DISPOFF}}$	−1	–	–	μA
V_{OH}	Output High Level Voltage	I_{OH} = −400 μA; CDO	V_{DD}−0.4	–	–	V
V_{OL}	Output Low Level Voltage	I_{OL} = 400 μA; CDO	–	–	0.4	V
R_{ON}(1)	Driver on Resistance	$V_{DD}-V_{EE}$ = 30 V, $\lvert V_{DE}-V_O \rvert$ = 0.5 V O1 to O80 (Note 5)	–	0.6	1.5	kΩ
R_{ON}(2)		$V_{DD}-V_{EE}$ = 20 V, $\lvert V_{DE}-V_O \rvert$ = 0.5 V O1 to O80 (Note 5)	–	0.7	2.0	kΩ
I_{ST}	Standby Current Drain	CDI = V_{DD}, $V_{DD}-V_{EE}$ = 30 V, CP = 6.0 MHz, Output unloaded; V_{SS}	–	–	200	μA
I_{SS} (Note 6)	Operating Current Drain	$V_{DD}-V_{EE}$ = 30 V, CP = 6.0 MHz, LOAD = 14 kHz, M = 35 Hz; V_{SS}	–	–	4.0	mA
I_{EE} (Note 7)		$V_{DD}-V_{EE}$ = 30 V, CP = 6.0 MHz, LOAD = 14 kHz, M = 35 Hz; V_{EE}	–	–	0.5	mA
C_I	Input Capacitance	f = 6 MHz; CP	–	8	–	pF

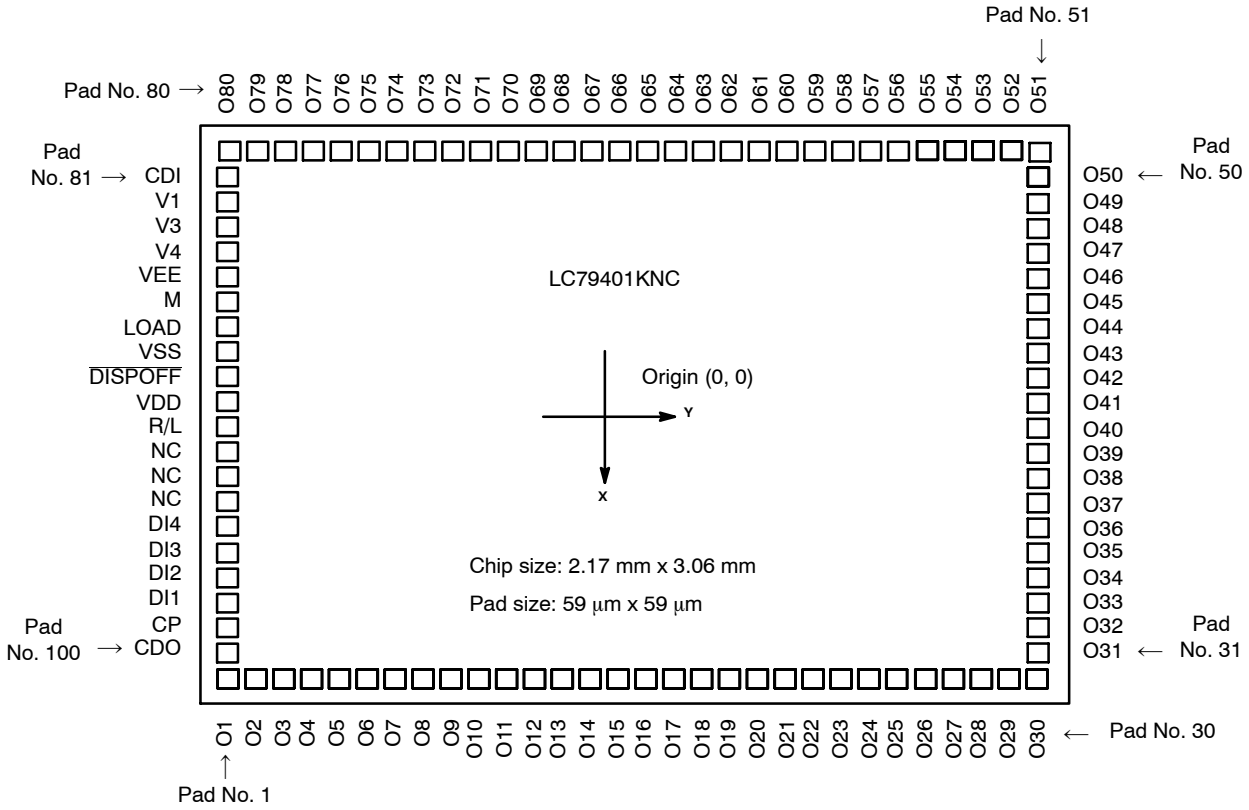
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. V_{DE} = one of V1, V3, V4 or V_{EE}. V1 = V_{DD}, V3 = 15/17 ($V_{DD}-V_{EE}$), V4 = 2/17 ($V_{DD}-V_{EE}$).
6. I_{SS} is the current flowing from V_{DD} to V_{SS}.
7. I_{EE} is the current flowing from V_{DD} to V_{EE}.

SWITCHING CHARACTERISTICS (T_A = +25°C ±2°C, V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{D1}	Output Delay Time1	Load = 15 pF: CDO	V_{DD} = 2.7 to 4.5 V	–	–	100	ns
			V_{DD} = 4.5 to 5.5 V	–	–	80	ns
t_{D2}	Output Delay Time2	Load = 15 pF: CDO	V_{DD} = 2.7 to 4.5 V	–	–	100	ns
			V_{DD} = 4.5 to 5.5 V	–	–	80	ns

PAD ASSIGNMENT



* Please connects the substrate to VEE or Floating.

Figure 1. Pad Assignment

BLOCK DIAGRAM

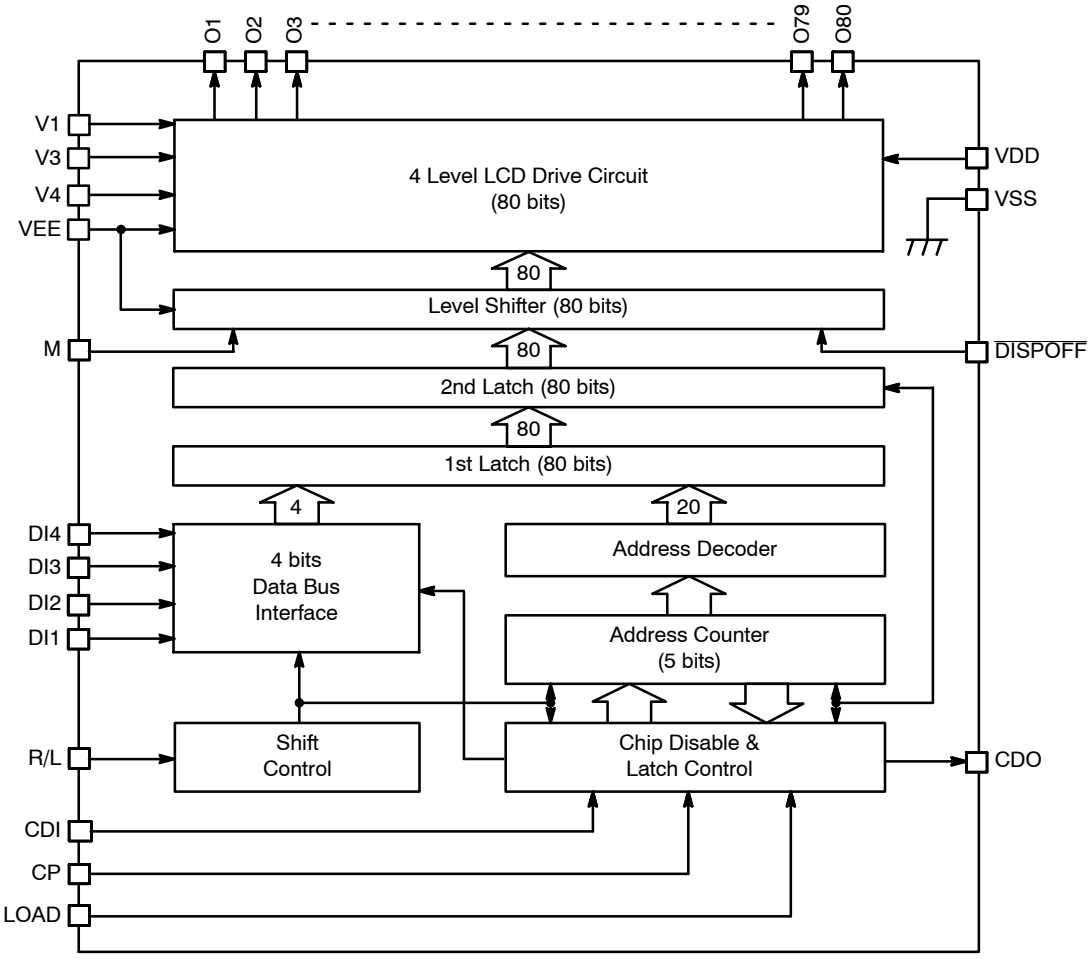


Figure 2. Block Diagram

PAD COORDINATES

Table 1. PAD COORDINATES

Pad No.	Signal	X Coordinates	Y Coordinates	Pad No.	Signal	X Coordinates	Y Coordinates
1	O1	979.5	−1268.0	51	O51	−945.0	1411.0
2	O2	979.5	−1162.0	52	O52	−979.5	1268.0
3	O3	979.5	−1072.0	53	O53	−979.5	1178.0
4	O4	979.5	−982.0	54	O54	−979.5	1088.0
5	O5	979.5	−892.0	55	O55	−979.5	998.0
6	O6	979.5	−802.0	56	O56	−979.5	908.0
7	O7	979.5	−712.0	57	O57	−979.5	818.0
8	O8	979.5	−622.0	58	O58	−979.5	728.0
9	O9	979.5	−532.0	59	O59	−979.5	638.0
10	O10	979.5	−442.0	60	O60	−979.5	548.0
11	O11	979.5	−352.0	61	O61	−979.5	458.0
12	O12	979.5	−262.0	62	O62	−979.5	368.0
13	O13	979.5	−172.0	63	O63	−979.5	278.0
14	O14	979.5	−82.0	64	O64	−979.5	188.0
15	O15	979.5	8.0	65	O65	−979.5	98.0
16	O16	979.5	98.0	66	O66	−979.5	8.0
17	O17	979.5	188.0	67	O67	−979.5	−82.0
18	O18	979.5	278.0	68	O68	−979.5	−172.0
19	O19	979.5	368.0	69	O69	−979.5	−262.0
20	O20	979.5	458.0	70	O70	−979.5	−352.0
21	O21	979.5	548.0	71	O71	−979.5	−442.0
22	O22	979.5	638.0	72	O72	−979.5	−532.0
23	O23	979.5	728.0	73	O73	−979.5	−622.0
24	O24	979.5	818.0	74	O74	−979.5	−712.0
25	O25	979.5	908.0	75	O75	−979.5	−802.0
26	O26	979.5	998.0	76	O76	−979.5	−892.0
27	O27	979.5	1088.0	77	O77	−979.5	−982.0
28	O28	979.5	1178.0	78	O78	−979.5	−1072.0
29	O29	979.5	1268.0	79	O79	−979.5	−1162.0
30	O30	945.0	1411.0	80	O80	−945.0	−1289.0
31	O31	855.0	1411.0	81	CDI	−855.0	−1289.0
32	O32	765.0	1411.0	82	V1	−765.0	−1289.0
33	O33	675.0	1411.0	83	V3	−675.0	−1289.0
34	O34	585.0	1411.0	84	V4	−585.0	−1289.0
35	O35	495.0	1411.0	85	VEE	−495.0	−1289.0
36	O36	405.0	1411.0	86	M	−405.0	−1289.0
37	O37	315.0	1411.0	87	LOAD	−315.0	−1289.0
38	O38	225.0	1411.0	88	VSS	−225.0	−1289.0
39	O39	135.0	1411.0	89	$\overline{\text{DISPOFF}}$	−135.0	−1289.0
40	O40	45.0	1411.0	90	VDD	−45.0	−1289.0

Table 1. PAD COORDINATES (continued)

Pad No.	Signal	X Coordinates	Y Coordinates	Pad No.	Signal	X Coordinates	Y Coordinates
41	O41	−45.0	1411.0	91	RL	45.0	−1289.0
42	O42	−135.0	1411.0	92	NC	135.0	−1289.0
43	O43	−225.0	1411.0	93	NC	225.0	−1289.0
44	O44	−315.0	1411.0	94	NC	315.0	−1289.0
45	O45	−405.0	1411.0	95	DI4	405.0	−1289.0
46	O46	−495.0	1411.0	96	DI3	495.0	−1289.0
47	O47	−585.0	1411.0	97	DI2	585.0	−1289.0
48	O48	−675.0	1411.0	98	DI1	675.0	−1289.0
49	O49	−765.0	1411.0	99	CP	765.0	−1289.0
50	O50	−855.0	1411.0	100	CDO	855.0	−1289.0

PIN FUNCTION

Table 2. PIN FUNCTION

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>90</td><td>V_{DD}</td><td rowspan="3">Supply</td><td rowspan="3">V_{DD}–V_{SS}: Logic power supply
V_{DD}–V_{EE}: LCD drive circuit power supply</td></tr>
<tr><td>88</td><td>V_{SS}</td></tr>
<tr><td>85</td><td>V_{EE}</td></tr>
<tr><td>82</td><td>V1</td><td rowspan="3">Supply</td><td rowspan="3">LCD drive level power supply
V1, V_{EE}: Selected level
V3, V4: Unselected level</td></tr>
<tr><td>83</td><td>V3</td></tr>
<tr><td>84</td><td>V4</td></tr>
<tr><td>99</td><td>CP</td><td>I</td><td>Display data acquisition clock (falling edge trigger)</td></tr>
<tr><td>87</td><td>LOAD</td><td>I</td><td>Display data latch clock (falling edge trigger)
The display data LCD drive signal is output on the falling edge</td></tr>
<tr><td>95
96
97
98</td><td>DI4
DI3
DI2
DI1</td><td>I</td><td>
<table>
<tr><th>Display Data</th><th>LCD Drive Output</th><th>LCD Display</th></tr>
<tr><td>H</td><td>Selected Level</td><td>On</td></tr>
<tr><td>L</td><td>Unselected Level</td><td>Off</td></tr>
</table>
</td></tr>
<tr><td>91</td><td>R/L</td><td>I</td><td>Control pin that inverts the data output destination:
<table>
<tr><th rowspan="2">R/L</th><th rowspan="2">Data Input</th><th colspan="7">Number of Clock</th></tr>
<tr><th>1</th><th>2</th><th>3</th><th>…</th><th>18</th><th>19</th><th>20</th></tr>
<tr><td rowspan="4">L</td><td>DI1</td><td>O77</td><td>O73</td><td>O69</td><td>…</td><td>O9</td><td>O5</td><td>O1</td></tr>
<tr><td>DI2</td><td>O78</td><td>O74</td><td>O70</td><td>…</td><td>O10</td><td>O6</td><td>O2</td></tr>
<tr><td>DI3</td><td>O79</td><td>O75</td><td>O71</td><td>…</td><td>O11</td><td>O7</td><td>O3</td></tr>
<tr><td>DI4</td><td>O80</td><td>O76</td><td>O72</td><td>…</td><td>O12</td><td>O8</td><td>O4</td></tr>
<tr><td rowspan="4">H</td><td>DI1</td><td>O4</td><td>O8</td><td>O12</td><td>…</td><td>O72</td><td>O76</td><td>O80</td></tr>
<tr><td>DI2</td><td>O3</td><td>O7</td><td>O11</td><td>…</td><td>O71</td><td>O75</td><td>O79</td></tr>
<tr><td>DI3</td><td>O2</td><td>O6</td><td>O10</td><td>…</td><td>O70</td><td>O74</td><td>O78</td></tr>
<tr><td>DI4</td><td>O1</td><td>O5</td><td>O9</td><td>…</td><td>O69</td><td>O73</td><td>O77</td></tr>
</table>
</td></tr>
<tr><td>86</td><td>M</td><td>I</td><td>LCD drive output alternation signal</td></tr>
<tr><td>81</td><td>CDI</td><td>I</td><td>Chip disable pin
High level: Data is not acquired
Low level: Data is acquired</td></tr>
<tr><td>100</td><td>CDO</td><td>O</td><td>Connect to the CDI pin on the next chip when cascade connection is used</td></tr>
<tr><td>89</td><td>$\overline{\text{DISPOFF}}$</td><td>I</td><td>Input that controls the O1 to O80 output pins. During periods when this pin Is low, the O1 to O80 output pins output the V1 level. See the truth table</td></tr>
<tr><td>1 to 80</td><td>O1 to O80</td><td>O</td><td>LCD drive outputs
The output level are determined by the combination of the output the data, The M signal, and The $\overline{\text{DISPOFF}}$ pin as shown in the table.
<table>
<tr><th>M</th><th>Q</th><th>$\overline{\text{DISPOFF}}$</th><th>Output</th></tr>
<tr><td>L</td><td>L</td><td>H</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>V1</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>V4</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>VEE</td></tr>
<tr><td>*</td><td>*</td><td>L</td><td>V1</td></tr>
</table>
* Don’t care (fixed at high or low)</td></tr>
<tr><td>92</td><td>NC</td><td rowspan="3">-</td><td rowspan="3">Must be left open</td></tr>
<tr><td>93</td><td>NC</td></tr>
<tr><td>94</td><td>NC</td></tr>
</table>

APPLICATION EXAMPLE (LC79401KNC/LC79430KNC)

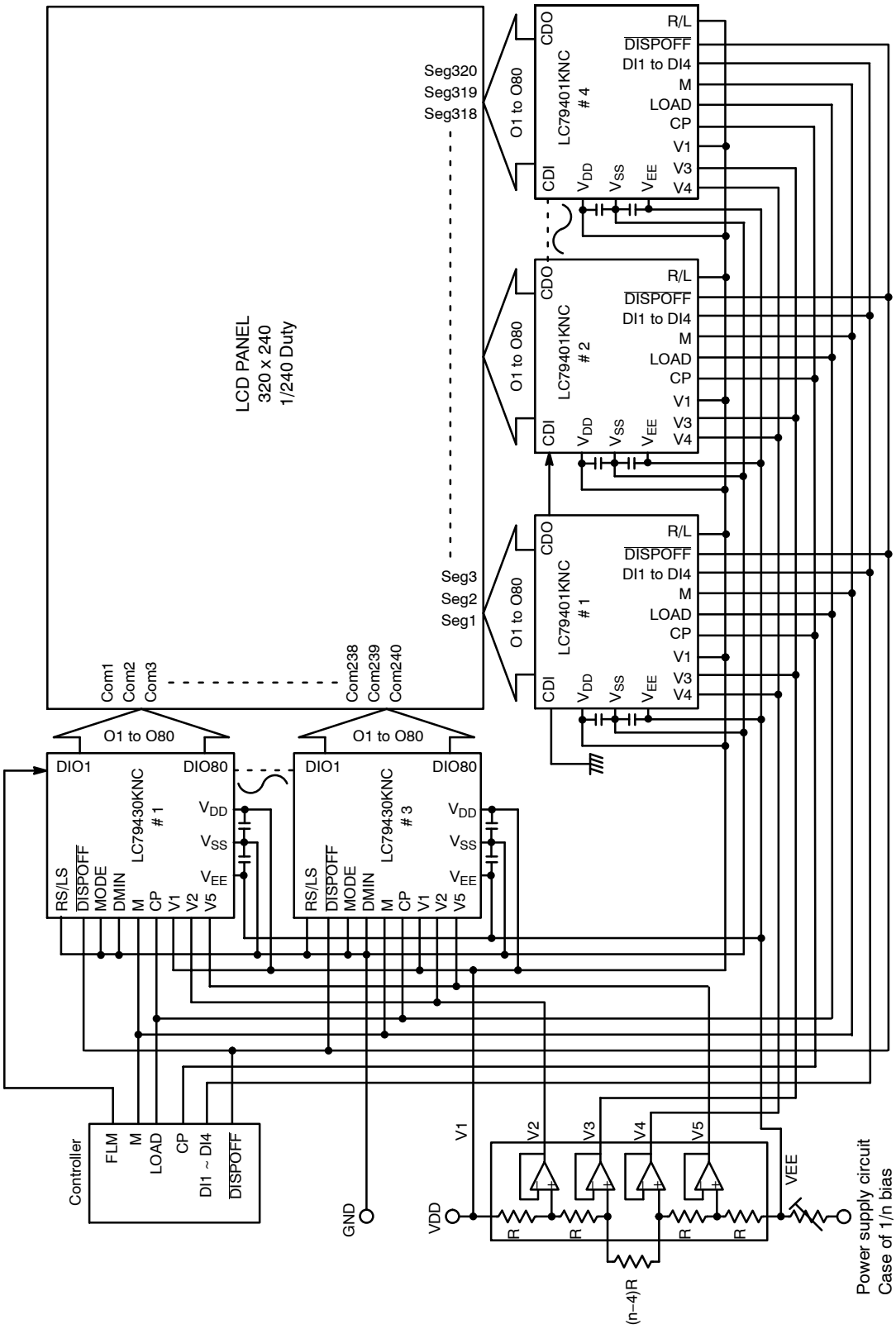


Figure 3. Application Example

SWITCHING CHARACTERISTICS DIAGRAM

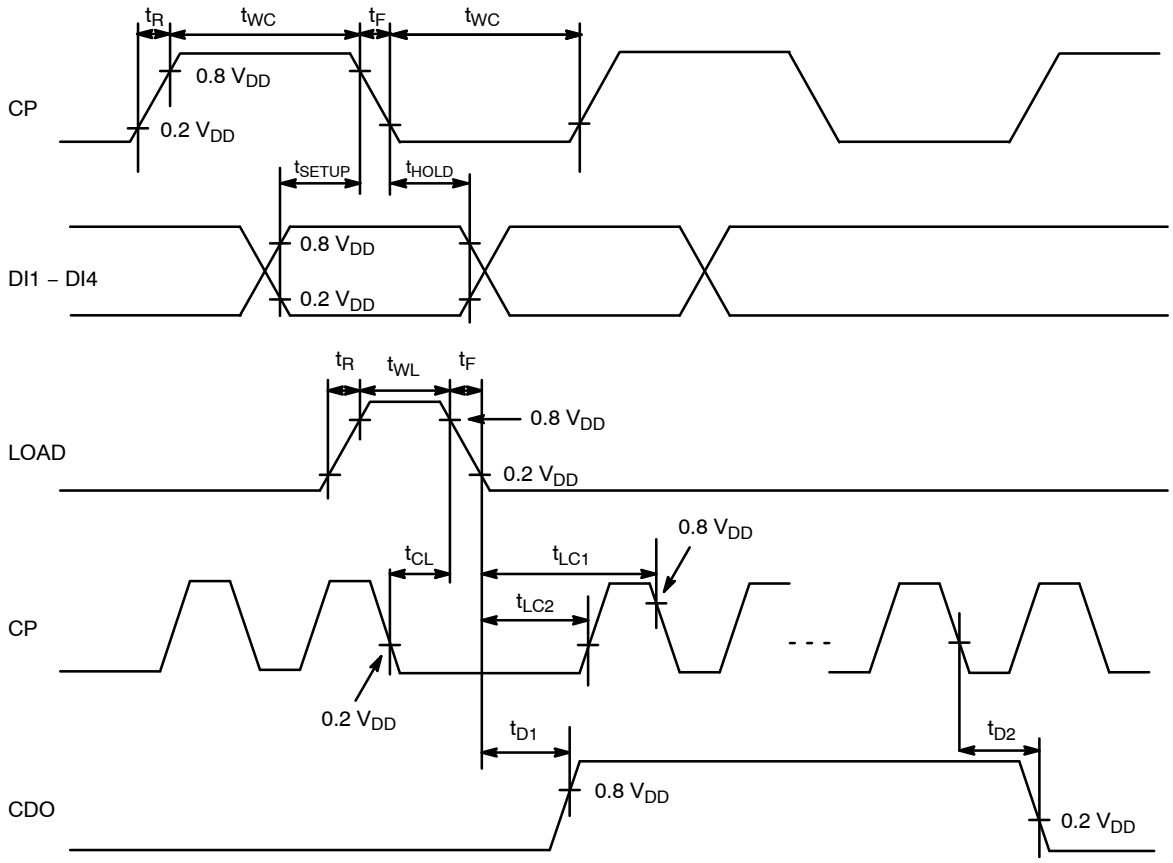


Figure 4. Switching Characteristics Diagram

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