LC79430KNC

Dot-Matrix LCD Drivers

CMOS LSI

ON Semiconductor®

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The LC79430KNC is a large-scale dot matrix LCD common driver LSI. The LC79430KNC contains an 80-bit bidirectional shift register and is equipped with a 4-level LCD driver. The input/output pins for cascade connection can be used to further increase the IC's number of bits. The LC79430KNC can be used in conjunction with segment driver LC79401KNC to drive a wide-screen LCD panel.

Features

- On-chip LCD Drive Circuit (80 bits)
- Display Duty Selection Ranging from 1/64 to 1/256
- On-chip Input/Output Pins Support further Increases in Bit Number
- Supports Externally Supplied Bias Voltage
- On-chip 80-bit Bidirectional Shift Register (Supports 40-bit × 2 Division)
- Supports Single Mode (80-bit Shift Register) and Dual Mode (40-bit × 2 Shift Register) Applications
  - ♦ Single Mode:
    (1) O1 → O80
    (2) O80 → O1
  - ♦ Dual Mode:
    (3) O1 → O40, O41 → O80
    (4) O80 → O41, O40 → O1

  All Four of the Shift Direction Selection Listed above All Supported
- Operating Power Supply Voltage/Operating Temperature
  V_{DD} (Logic Block): 2.7 to 5.5 V/−20 to +85°C
  $V_{DD} - V_{EE}$ (LCD block): 12 to 32 V/−20 to +85°C
- CMOS Process
- Package: Bare Chip

The electrical characteristics values shown below are for devices packaged in the plastic package.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C ±2°C, V_{SS} = 0 V)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD} max	Maximum Supply Voltage (Logic)		−0.3 to +7.0	V
V_{DD}−V_{EE} max	Maximum Supply Voltage (LCD)	(Note 1)	0 to 35	V
V_I max	Maximum Input Voltage		−0.3 to V_{DD} + 0.3	V
T_{stg}	Storage Temperature		−40 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. The following relations between elements should be maintained: $V_{DD} \geq V1 > V2 > V5 > V_{EE}$, $V_{DD}-V2 \leq 7$ V, $V5-V_{EE} \leq 7$ V.

ALLOWABLE OPERATING RANGES (T_A = −20 to +85°C, V_{SS} = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply Voltage (Logic)		2.7	–	5.5	V
V_{DD}−V_{EE}	Supply Voltage (LCD)	(Notes 2, 3)	12	–	32	V
V_{IH}	Input High Level Voltage	DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, $\overline{\text{DISPOFF}}$	0.8 V_{DD}	–	–	V
V_{IL}	Input Low Level Voltage	DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, $\overline{\text{DISPOFF}}$	–	–	0.2 V_{DD}	V
f_{CP}	CP Shift Clock	CP	–	–	1.0	MHz
t_{WC}	CP Pulse Width	CP	63	–	–	ns

ALLOWABLE OPERATING RANGES (T_A = −20 to +85°C, V_{SS} = 0 V) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SETUP}	Setup Time	DIO1 → CP, DIO80 → CP, DMIN → CP	100	–	–	ns
t_{HOLD}	Hold Time	DIO1 → CP, DIO80 → CP, DMIN → CP	100	–	–	ns
t_R	CP Rise Time	CP	–	–	50	ns
t_F	CP Fall Time	CP	–	–	50	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. The following relations between elements should be maintained: $V_{DD} \geq V1 > V2 > V5 > V_{EE}$, $V_{DD}-V2 \leq 7$ V, $V5-V_{EE} \leq 7$ V.
3. When the power supply is turned on, power to the LCD driver is turned on after or simultaneously with the turning on of the logic section's power supply. When the power supply is turned off, the logic power supply is turned off after or at the same time the LCD driver power supply is turned off.

ELECTRICAL CHARACTERISTICS (T_A = +25°C ±2°C, V_{DD} = 2.7 to 5.5 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IH}	Input High Level Current	$V_{IN} = V_{DD}$; V_{DD} = 5.5 V, DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, $\overline{DISPOFF}$	–	–	1	μA
I_{IL}	Input Low Level Current	$V_{IN} = V_{SS}$; V_{DD} = 5.5 V, DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, $\overline{DISPOFF}$	−1	–	–	μA
V_{OH}	Output High Level Voltage	I_{OH} = −0.4 mA, DIO1, DIO80	V_{DD}−0.4	–		V
V_{OL}	Output Low Level Voltage	I_{OL} = 0.4 mA, DIO1, DIO80	–	–	0.4	V
R_{ON}(1)	Driver on Resistance	$V_{DD}-V_{EE}$ = 30 V, $\lvert V_{DE}-V_O \rvert$ = 0.5 V V_{DD} = 4.5 V; O1 to O80 (Note 4)	–	–	1.0	kΩ
R_{ON}(2)		$V_{DD}-V_{EE}$ = 20 V, $\lvert V_{DE}-VO \rvert$ = 0.5 V V_{DD} = 4.5 V; O1 to O80 (Note 4)	–	–	1.0	kΩ
I_{SS} (Note 5)	Consumable Current Drain(1)	$V_{DD}-V_{EE}$ = 30 V, CP = 14 kHz Output unloaded, V_{DD} = 5.5 V; V_{SS}	–	–	100	μA
I_{EE} (Note 6)	Consumable Current Drain(2)	$V_{DD}-V_{EE}$ = 30 V, CP = 14 kHz Output unloaded, V_{DD} = 5.5 V; V_{EE}	–	–	100	μA
C_I	Input Capacitance	f = 1 MHz; CP	–	8	–	pF

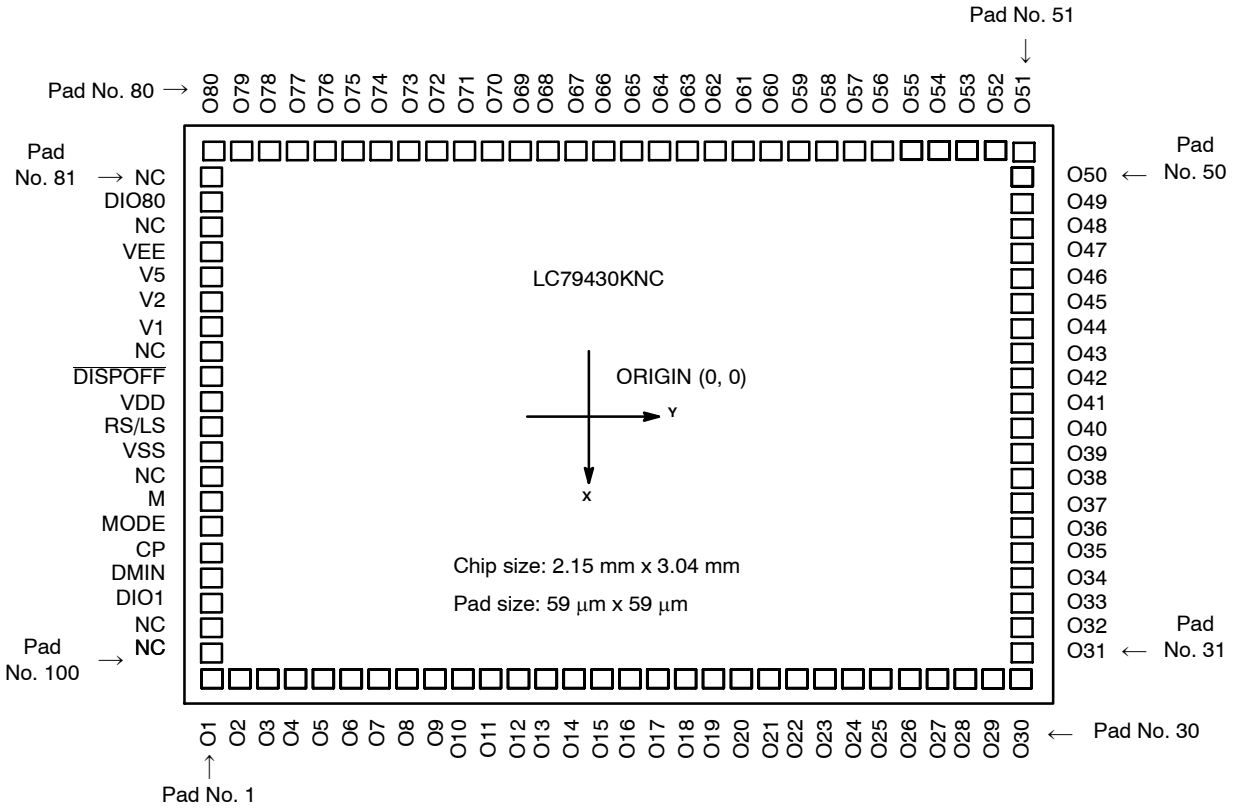
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. V_{DE} = V1 or V2 or V5 or V_{EE}, V1 = V_{DD}, V2 = 16/17($V_{DD}-V_{EE}$), V5 = 1/17($V_{DD}-V_{EE}$).
5. I_{SS} is the current flowing from V_{DD} to V_{SS}.
6. I_{EE} is the current flowing from V_{DD} to V_{EE}.

SWITCHING CHARACTERISTICS (T_A = +25°C ±2°C, V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tPLH	Output Delay Time	CL = 15 pF; CP → DIO1, CP → DIO80	–	–	250	ns
tPHL		CL = 15 pF; CP → DIO1, CP → DIO80	–	–	250	ns

PAD ASSIGNMENT



* Please connects the substrate to VEE or Floating.

Figure 1. Pad Assignment

BLOCK DIAGRAM

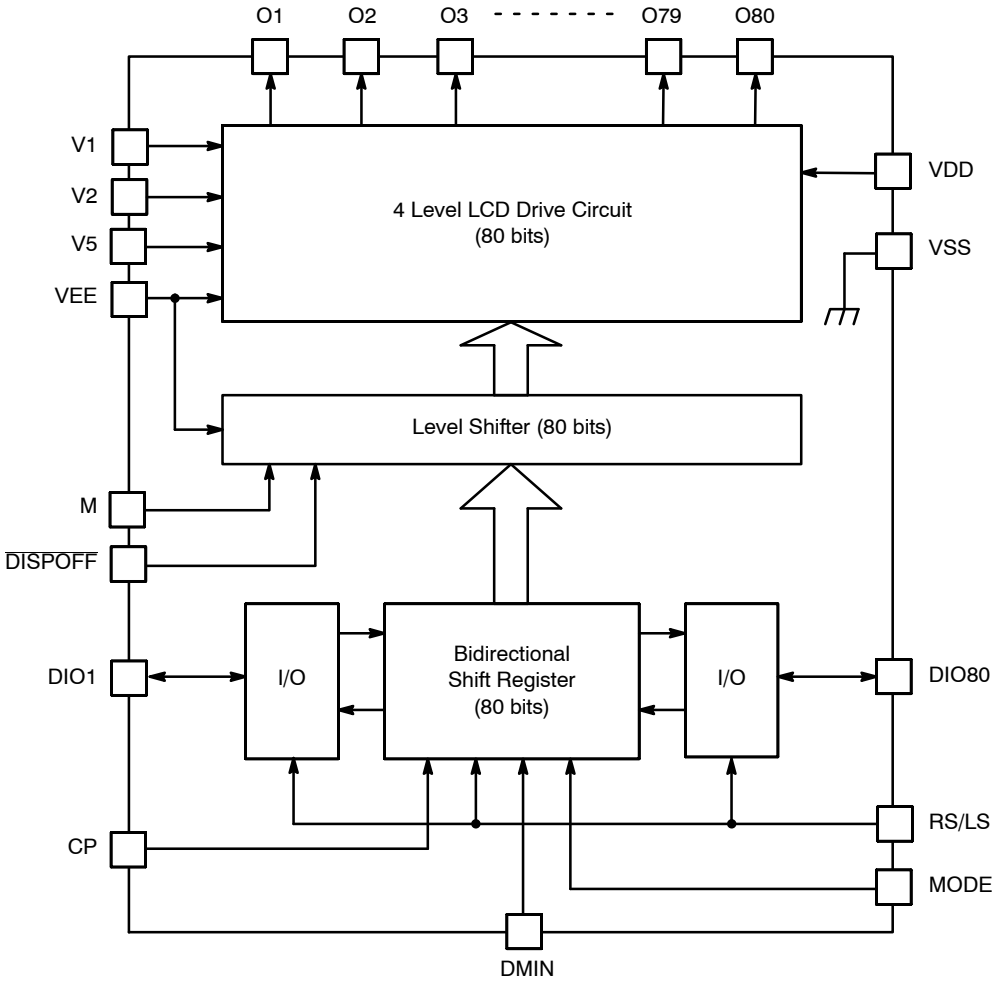


Figure 2. Block Diagram

PAD COORDINATES

Table 1. PAD COORDINATES

Pad No.	Signal	X Coordinates	Y Coordinates	Pad No.	Signal	X Coordinates	Y Coordinates
1	O1	969.5	−1263.0	51	O51	−945.0	1416.0
2	O2	969.5	−1157.0	52	O52	−969.5	1273.0
3	O3	969.5	−1067.0	53	O53	−969.5	1183.0
4	O4	969.5	−977.0	54	O54	−969.5	1093.0
5	O5	969.5	−887.0	55	O55	−969.5	1003.0
6	O6	969.5	−797.0	56	O56	−969.5	913.0
7	O7	969.5	−707.0	57	O57	−969.5	823.0
8	O8	969.5	−617.0	58	O58	−969.5	733.0
9	O9	969.5	−527.0	59	O59	−969.5	643.0
10	O10	969.5	−437.0	60	O60	−969.5	553.0
11	O11	969.5	−347.0	61	O61	−969.5	463.0
12	O12	969.5	−257.0	62	O62	−969.5	373.0
13	O13	969.5	−167.0	63	O63	−969.5	283.0
14	O14	969.5	−77.0	64	O64	−969.5	193.0
15	O15	969.5	13.0	65	O65	−969.5	103.0
16	O16	969.5	103.0	66	O66	−969.5	13.0
17	O17	969.5	193.0	67	O67	−969.5	−77.0
18	O18	969.5	283.0	68	O68	−969.5	−167.0
19	O19	969.5	373.0	69	O69	−969.5	−257.0
20	O20	969.5	463.0	70	O70	−969.5	−347.0
21	O21	969.5	553.0	71	O71	−969.5	−437.0
22	O22	969.5	643.0	72	O72	−969.5	−527.0
23	O23	969.5	733.0	73	O73	−969.5	−617.0
24	O24	969.5	823.0	74	O74	−969.5	−707.0
25	O25	969.5	913.0	75	O75	−969.5	−797.0
26	O26	969.5	1003.0	76	O76	−969.5	−887.0
27	O27	969.5	1093.0	77	O77	−969.5	−977.0
28	O28	969.5	1183.0	78	O78	−969.5	−1067.0
29	O29	969.5	1273.0	79	O79	−969.5	−1157.0
30	O30	945.0	1416.0	80	O80	−945.0	−1284.0
31	O31	855.0	1416.0	81	NC	−855.0	−1284.0
32	O32	765.0	1416.0	82	DIO80	−765.0	−1284.0
33	O33	675.0	1416.0	83	NC	−675.0	−1284.0
34	O34	585.0	1416.0	84	VEE	−585.0	−1284.0
35	O35	495.0	1416.0	85	V5	−495.0	−1284.0
36	O36	405.0	1416.0	86	V2	−405.0	−1284.0
37	O37	315.0	1416.0	87	V1	−315.0	−1284.0
38	O38	225.0	1416.0	88	NC	−225.0	−1284.0
39	O39	135.0	1416.0	89	$\overline{\text{DISPOFF}}$	−135.0	−1284.0
40	O40	45.0	1416.0	90	VDD	−45.0	−1284.0

Table 1. PAD COORDINATES (continued)

Pad No.	Signal	X Coordinates	Y Coordinates	Pad No.	Signal	X Coordinates	Y Coordinates
41	O41	−45.0	1416.0	91	RS/LS	45.0	−1284.0
42	O42	−135.0	1416.0	92	VSS	135.0	−1284.0
43	O43	−225.0	1416.0	93	NC	225.0	−1284.0
44	O44	−315.0	1416.0	94	M	315.0	−1284.0
45	O45	−405.0	1416.0	95	MODE	405.0	−1284.0
46	O46	−495.0	1416.0	96	CP	495.0	−1284.0
47	O47	−585.0	1416.0	97	DMIN	585.0	−1284.0
48	O48	−675.0	1416.0	98	DIO1	675.0	−1284.0
49	O49	−765.0	1416.0	99	NC	765.0	−1284.0
50	O50	−855.0	1416.0	100	NC	855.0	−1284.0

PIN FUNCTION

Table 2. PIN FUNCTION

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>90
92
84</td><td>V_{DD}
V_{SS}
V_{EE}</td><td>Supply</td><td>V_{DD}–V_{SS}: Logic power supply
V_{DD}–V_{EE}: LCD drive circuit power supply</td></tr>
<tr><td>87
86
85</td><td>V1
V2
V5</td><td>Supply</td><td>LCD drive level power supply
V1, V_{EE}: Selected level
V2, V5: Unselected level</td></tr>
<tr><td>96</td><td>CP</td><td>I</td><td>Bidirectional shift register shift clock (falling edge trigger)</td></tr>
<tr><td>98
82

91
95
97</td><td>DIO1
DIO80

RS/LS
MODE
DMIN</td><td>I/O
I/O

I
I
I</td><td>
<table>
<tr><th>MODE</th><th>RS/LS</th><th>Data Transfer Direction</th><th>DIO1</th><th>DIO80</th><th>DMIN</th></tr>
<tr><td rowspan="2">L (Single)</td><td>L (Shift right)</td><td>O1 → O80</td><td>IN</td><td>OUT</td><td>*</td></tr>
<tr><td>H (Shift left)</td><td>O80 → O1</td><td>OUT</td><td>IN</td><td>*</td></tr>
<tr><td rowspan="4">H (Dual)</td><td rowspan="2">L (Shift right)</td><td>O1 → O40</td><td rowspan="2">IN</td><td rowspan="2">OUT</td><td rowspan="2">IN</td></tr>
<tr><td>O41 → O80</td></tr>
<tr><td rowspan="2">H (Shift left)</td><td>O80 → O41</td><td rowspan="2">OUT</td><td rowspan="2">IN</td><td rowspan="2">IN</td></tr>
<tr><td>O40 → O1</td></tr>
</table>
* Don’t care (fixed at high or low)
</td></tr>
<tr><td>94</td><td>M</td><td>I</td><td>LCD drive output alternation signal</td></tr>
<tr><td>89</td><td>$\overline{\text{DISPOFF}}$</td><td>I</td><td>O1 to O80 output controlling input pins</td></tr>
<tr><td>1
.
.
.
.
.
.
.
80</td><td>O1
.
.
.
.
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.
.
O80</td><td>O</td><td>LCD drive outputs
The output levels are determined by the combination of the output the data,
The M signal, and the $\overline{\text{DISPOFF}}$ pin as shown in the table.
<table>
<tr><th>M</th><th>Data</th><th>$\overline{\text{DISPOFF}}$</th><th>Output</th></tr>
<tr><td>L</td><td>L</td><td>H</td><td>V2</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>VEE</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>V5</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>V1</td></tr>
<tr><td>*</td><td>*</td><td>L</td><td>V1</td></tr>
</table>
* Don’t care (fixed at high or low)
</td></tr>
<tr><td>81
83
88
93
99
100</td><td>NC</td><td>–</td><td>Must be left open</td></tr>
</table>

APPLICATION EXAMPLE (LC79401KNC/LC79430KNC)

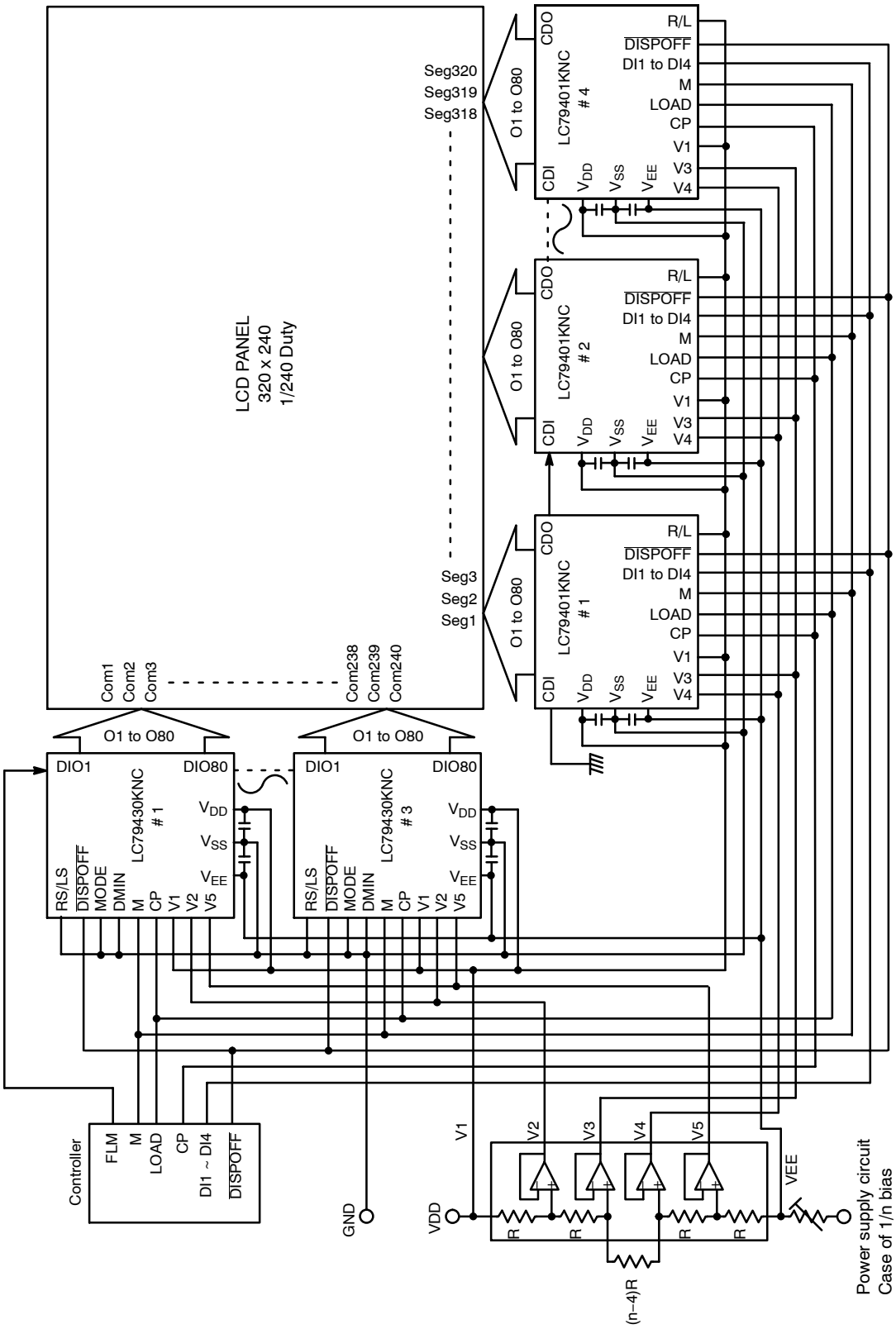

Figure 3. Application Example

SWITCHING CHARACTERISTICS DIAGRAM

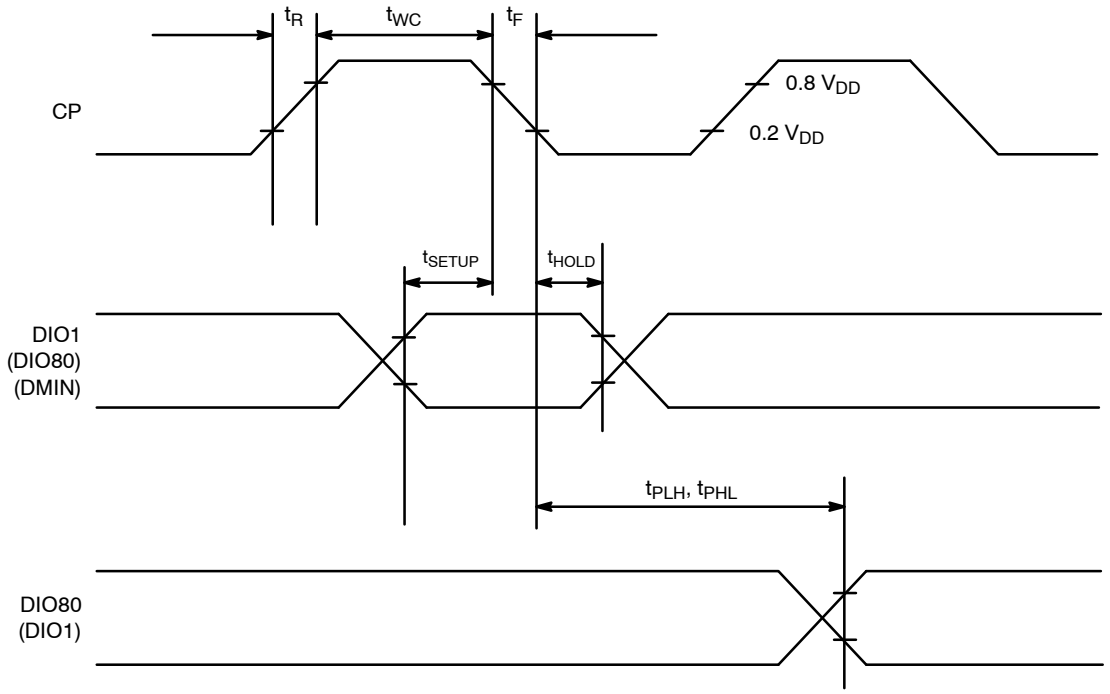

Figure 4. Switching Characteristics Diagram

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