LC87F9W48A

8-bit 1-chip Microcontroller with Full-Speed USB

Tablet Signal Processing Circuit Integrated

ON Semiconductor®

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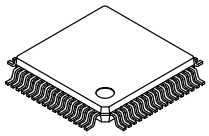
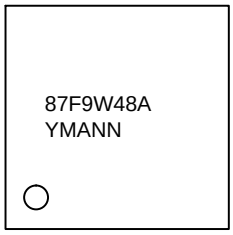


TQFP64 7x7
CASE 932 BC

MARKING DIAGRAM



87F9W48A	= Specific Device Code
Y	= Year of Production
M	= Assembly Operation Month
A	= Assembly Site
NN	= Serialization

PIN CONNECTION

See detailed Pin Connection information on page 5 of this data sheet.

ORDERING INFORMATION

Device	Package	Shipping
LC87F9W48A−F5CE1−H	TQFP64 (Pb−Free)	1250 / JTRAY

Overview

The LC87F9W48A is an 8−bit microcontroller that, centered around a CPU running at a minimum bus cycle time of 83.3 ns, integrates on a single chip a number of hardware features such as 50K−byte flash ROM (on−board programmable), 3072−byte RAM, an on−chip debugger, a sophisticated 16−bit timer/counter (may be divided into 8−bit timers), a 16−bit timer (may be divided into 8−bit timers or 8−bit PWMs), two 8−bit timers with a prescaler, a base timer, two channels of synchronous SIO interface with automatic transfer function, an asynchronous/synchronous SIO interface, a single−master I^2C/synchronous SIO interface, a UART interface (full duplex), a full−speed USB interface (with device control function), a 10−bit 5−channel AD converter, two channels of 12−bit PWM, a system clock frequency divider, an internal reset circuit, a tablet signal processing circuit, and a 31−source 10−vector interrupt function.

Features

Flash ROM:

- Capable of On−board Programming with a Wide Supply Voltage Range of 2.7 V to 5.5 V
- Block Erasable in 128-byte Units
- Writes Data in 2-byte Units
- 51200 × 8 bits

RAM:

- 3072 × 9 bits

Bus Cycle Time:

- 83.3 ns (at CF = 12 MHz), V_{DD} = 2.7 V to 5.5 V

NOTE: The bus cycle time here refers to the ROM read speed.

Tablet Signal Processing Circuit:

- PGA (Programmable Gain Amplifier): 1.0 dB to 42.5 dB Gain Low noise of 0.66 μV/√Hz or less (when PGA gain is 34.5 dB)
- Multiplier (full−wave rectifier circuit): Made up of Multiplier + Comparator + Differential/Single−ended Converter Circuit 1× Multiplier Gain, Built−in 2nd Order Low Pass Filter
- Built−in Integrator Amplifier
- Built−in Reference Voltage Generator
- Consumption Current: 4.3 mA (Typ) (Tablet Signal Processing Circuit Block Only)

Minimum Instruction Cycle Time (tCYC):

- 250 ns (at CF = 12 MHz), V_{DD} = 2.7 V to 5.5 V

Ports:

- I/O Ports
  Ports whose input/output can be specified in 1−bit units: 35 (P00 to P07, P10 to P17, P20 to P27, P30 to P34, P70 to P73, PWM0, PWM1)
- USB−dedicated Pins: 4 (D+, D−, DPUP, VBUS)
- Dedicated Tablet Signal Processing Pins: 12 (MCLK, MUTE, TCLK, REFIN, VIN+, VIN−, VREF, VOUT, MIN, MOUT, SIN, SOUT)
- Oscillation−dedicated Pins: 2 (CF1, CF2)
- PLL Filter Pin: 1 (UFILT)
- Reset Pin: 1 ($\overline{RES}$)
- Debugger−dedicated Pin: 1 (OWP0)
- Power Pins: 8 ($V_{SS}1$ to $V_{SS}3$, AV_{SS}, $V_{DD}1$ to $V_{DD}3$, AV_{DD})

Timers:

- Timer 0: 16−bit timer/counter with a capture register
  - Mode 0: 8−bit timer with an 8−bit programmable prescaler (with an 8−bit capture register) × 2 channels
  - Mode 1: 8−bit timer with an 8−bit programmable prescaler (with an 8−bit capture register) + 8−bit counter (with an 8−bit capture register)
  - Mode 2: 16−bit timer with an 8−bit programmable prescaler (with a 16−bit capture register)
  - Mode 3: 16−bit counter (with a 16−bit capture register)
- Timer 1: 16−bit timer/counter with PWM/toggle output
  - Mode 0: 8−bit timer with an 8−bit prescaler (with toggle output) + 8−bit timer/counter with an 8−bit prescaler (with toggle output)
  - Mode 1: 8−bit PWM with an 8−bit prescaler × 2 channels
  - Mode 2: 16−bit timer/counter with an 8−bit prescaler (with toggle output) (Toggle output also possible from the low−order 8 bits)
  - Mode 3: 16−bit timer with an 8−bit prescaler (with toggle output) (Low−order 8 bits can be used as a PWM.)
- Timer 6: 8−bit timer with a 6−bit prescaler (with toggle output)
- Timer 7: 8−bit timer with a 6−bit prescaler (with toggle output)
- Base Timer
  1. The clock can be selected from the system clock and timer 0 prescaler output.
  2. Interrupts can be generated at five specified time intervals.

Serial Interfaces:

- SIO0: Synchronous serial interface
  1. LSB first/MSB first selectable
  2. Transfer clock cycle: 4/3 to 512/3 tCYC
  3. Automatic continuous data communication (1 to 256 bits can be specified in 1−bit units.) (Suspension and resumption of data transfer possible in 1−byte units.)
- SIO1: 8−bit asynchronous/synchronous serial interface
  - Mode 0: Synchronous 8−bit serial I/O (2− or 3−wire configuration, 2 to 512 tCYC transfer clock)
  - Mode 1: Asynchronous serial I/O (half−duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrate)
  - Mode 2: Bus mode 1 (1 start bit, 8 data bits, 2 to 512 tCYC transfer clock)
  - Mode 3: Bus mode 2 (start detection, 8 data bits, stop detection)
- SIO4: Synchronous serial interface
  1. LSB first/MSB first selectable
  2. Transfer clock cycle: 4/3 to 1020/3 tCYC
  3. Automatic continuous data communication (1 to 2048 bytes can be specified in 1−byte units) (Suspension and resumption of data transfer possible on a byte or word basis.)
  4. Clock polarity selectable
  5. Internal CRC16 calculation circuit
- SMIIC2: Single master I^2C/8−bit synchronous SIO
  - Mode 0: Communication in master mode with a single−master
  - Mode 1: Synchronous 8−bit serial I/O (Data MSB first)

Full Duplex UART:

1. Data length: 7/8/9 bits selectable
2. Stop bits: 1 bit (2 bits in continuous transmission mode)
3. Parity bits: None/even/odd parity (8−bit data length only)
4. Baudrate: 16/3 to 8192/3 tCYC

AD Converter: 10 bits × 5 channels:

- 10−/8−bit AD converter resolution selectable
- Automatic start function (AD conversion start trigger is generated at the end of the receive period of the tablet signal processing circuit)
- Capable of AD converting of the integrator output (SOUT) from the tablet signal processing circuit

PWM: Multifrequency 12−bit PWM × 2 channels

USB Interface (with device control function):

1. Conforms to USB 2.0 (full−speed) specifications.
2. Supports a maximum of six user−defined endpoints.
3. Endpoint buffers are mapped into RAM (see Table 1).
4. Vbus connection detection function

Table 1. ENDPOINT BUFFERS

Endpoint		EP0	EP1	EP2	EP3	EP4	EP5	EP6
Transfer Type	Control	○	−	−	−	−	−	−
	Bulk	−	○	○	○	○	○	○
	Interrupt	−	○	○	○	○	○	○
	Isochronous	−	○	○	○	○	○	○
Max. Payload		64	64	64	64	64	64	64

Watchdog Timer:

- External RC watchdog timer
- Interrupt/system reset can be selected.

Clock Output Function:

- Capable of generating a clock with a frequency of 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, or 1/64 of the source oscillator clock selected as the system clock.

Interrupts:

- 31 sources, 10 vector addresses

1. Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt request of the level equal to or lower than the current interrupt is not accepted.
2. When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the lowest vector address takes precedence.

Table 2. INTERRUPTS

No.	Vector	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1/(tablet reception end)
3	00013H	H or L	INT2/T0L/INT4/USB bus active
4	0001BH	H or L	INT3/INT5/base timer/USB−Vbus detection
5	00023H	H or L	T0H/(tablet reception end)
6	0002BH	H or L	T1L/T1H/SMIIC2
7	00033H	H or L	SIO0/USB bus reset/USB suspend/UART1 reception end
8	0003BH	H or L	SIO1/USB endpoint/USB−SOF/SIO4/UART1 buffer empty/UART1 transmission end
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/PWM0/PWM1

- Priority level: X > H > L
- If interrupts of the same level occur at the same time, the interrupt with the lowest vector address is processed first.
- Vector address 0000BH or 00023H can be selected for the tablet reception end interrupt.

Subroutine Stack Level: Up to 1536 levels
(The stack is allocated in RAM.)

High−speed Multiplication/Division Instructions:

- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits × 8 bits (8 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)

Oscillator Circuits and PLL:

- RC oscillator circuit (internal): For system clock
- CF oscillator circuit: For system clock
- PLL circuit (internal): For USB interface
  (See Figure 8)

Internal Reset Function:

- Power−on reset (POR) function
  1. POR is generated only at a power−on time.
  2. The POR release level can be selected from 8 levels (1.67 V, 1.97 V, 2.07 V, 2.37 V, 2.57 V, 2.87 V, 3.86 V, and 4.35 V) by setting options.
- Low−voltage detection reset (LVD) function
  1. LVD and POR functions are combined to generate a reset when power is turned on and when the power voltage falls below a certain level.

2. The use/disuse of the LVD function and the low−voltage detection level (from 7 levels: 1.91 V, 2.01 V, 2.31 V, 2.51 V, 2.81 V, 3.79 V, and 4.28 V) can be selected by setting options.

Standby Function:

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  - Oscillators do not stop automatically.
  - There are three ways of releasing HALT mode.
    1. Setting the reset pin to a low level
    2. Generating a reset by the watchdog timer or low−voltage detection
    3. Generating an interrupt
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  - The PLL, CF, and RC oscillators automatically stop operation.
  - There are six ways of releasing HOLD mode.
    1. Setting the reset pin to a low level
    2. Generating a reset by the watchdog timer or low−voltage detection
    3. Establishing an interrupt source at either INT0, INT1, INT2, INT4, or INT5 pin
       *INT0 and INT1 HOLD mode release is available only when level detection is set.
    4. Establishing an interrupt source at port 0
    5. Establishing a bus active interrupt source in the USB interface control circuit
    6. Establishing a Vbus detection interrupt source

Package Form:

- TQFP64 (7 × 7) (Lead−free and halogen−free type)

Development Tools:

- On−chip debugger: TCB87−Type C (1−wire communication cable) + LC87F9W48A

Flash ROM Programming Board:

Package	Programming Board
TQFP64 (7 × 7)	W87F9WTQ

Flash ROM Writer: See Table 3.

Table 3. FLASH ROM WRITER

Vendor		Model	Version	Device
Flash Support Group (FSG)	Single	AF9709/AF9709B/AF9709C (including ANDO Electric products)	Rev. 03.28 or later	87F064SU
ON Semiconductor	Single/Gang	SKK/SKK Type B/SKK Type C (SANYO FWS)	Application version 1.08 or later Chip data version 2.44 or later	LC87F9W48
	On-board Single/Gang	SKK−DBG Type C (SANYO FWS)		

(Further information on the AF series)
Flash Support Group, Inc.
Phone: +81−53−459−1050
E−mail: sales@j−fsg.co.jp

PIN ASSIGNMENT

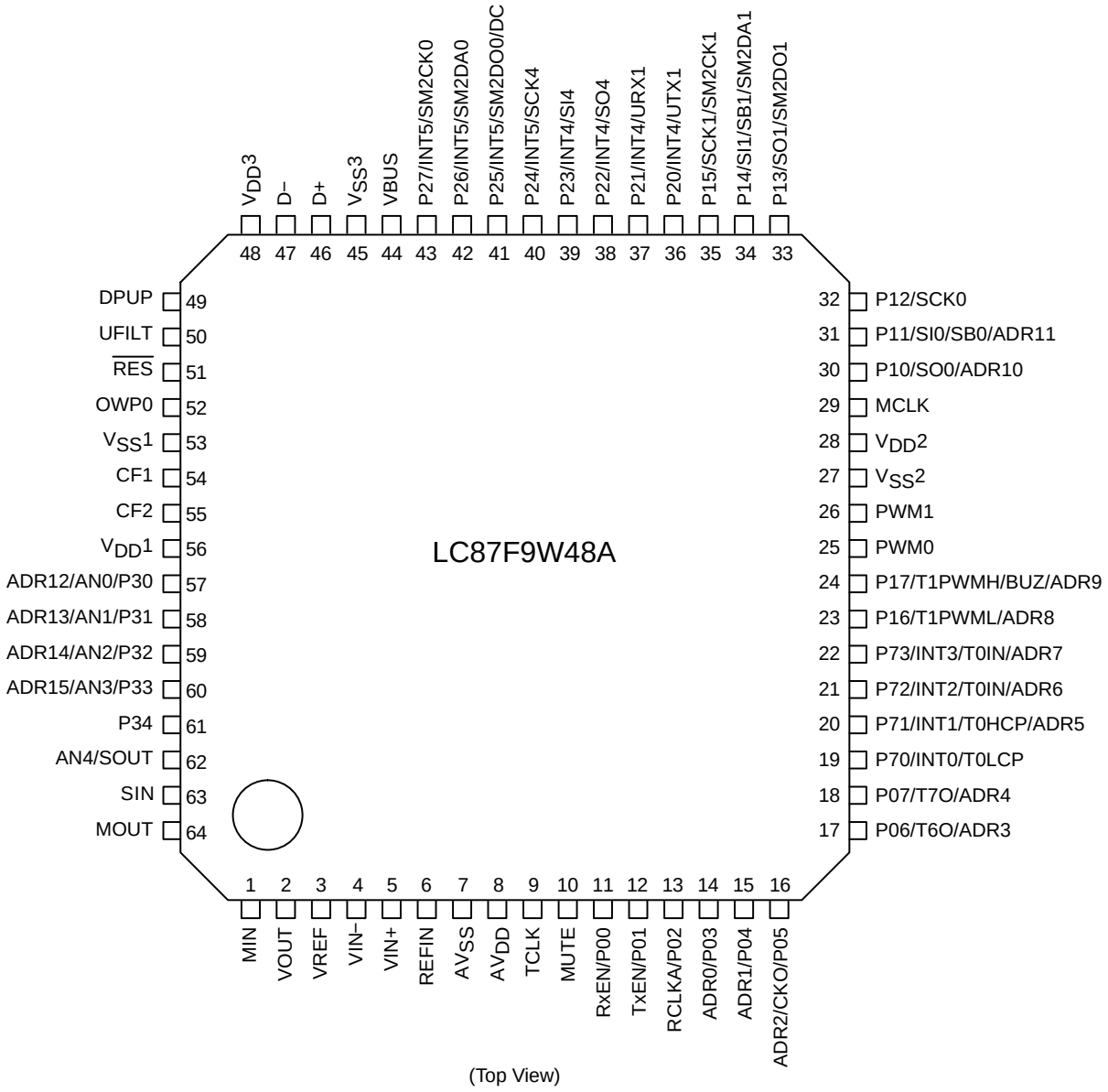


Figure 1. TQFP64 (7 × 7)

Table 4. PINOUT

Pin Number	Pin Name
1	MIN
2	VOUT
3	VREF
4	VIN−
5	VIN+
6	REFIN
7	AV_{SS}
8	AV_{DD}
9	TCLK
10	MUTE
11	P00/RxEN
12	P01/TxEN
13	P02/RCLKA
14	P03/ADR0
15	P04/ADR1
16	P05/CKO/ADR2
17	P06/T6O/ADR3
18	T07/T7O/ADR4
19	P70/INT0/T0LCP
20	P71/INT1/T0HCP/ADR5
21	P72/INT2/T0IN/ADR6
22	P73/INT3/T0IN/ADR7
23	P16/T1PWML/ADR8
24	P17/T1PWMH/BUZ/ADR9
25	PWM0
26	PWM1
27	$V_{SS}2$
28	$V_{DD}2$
29	MCLK
30	P10/SO0/ADR10
31	P11/SI0/SB0/ADR11
32	P12/SCK0

Pin Number	Pin Name
33	P13/SO1/SM2DO1
34	P14/SI1/SB1/SM2DA1
35	P15/SCK1/SM2CK1
36	P20/INT4/UTX1
37	P21/INT4/URX1
38	P22/INT4/SO4
39	P23/INT4/SI4
40	P24/INT5/SCK4
41	P25/INT5/SM2DO0/DC
42	P26/INT5/SM2DA0
43	P27/INT5/SM2CK0
44	VBUS
45	$V_{SS}3$
46	D+
47	D−
48	$V_{DD}3$
49	DPUP
50	UFILT
51	$\overline{RES}$
52	OWP0
53	$V_{SS}1$
54	CF1
55	CF2
56	$V_{DD}1$
57	P30/AN0/ADR12
58	P31/AN1/ADR13
59	P32/AN2/ADR14
60	P33/AN3/ADR15
61	P34
62	SOUT/AN4
63	SIN
64	MOUT

SYSTEM BLOCK DIAGRAM

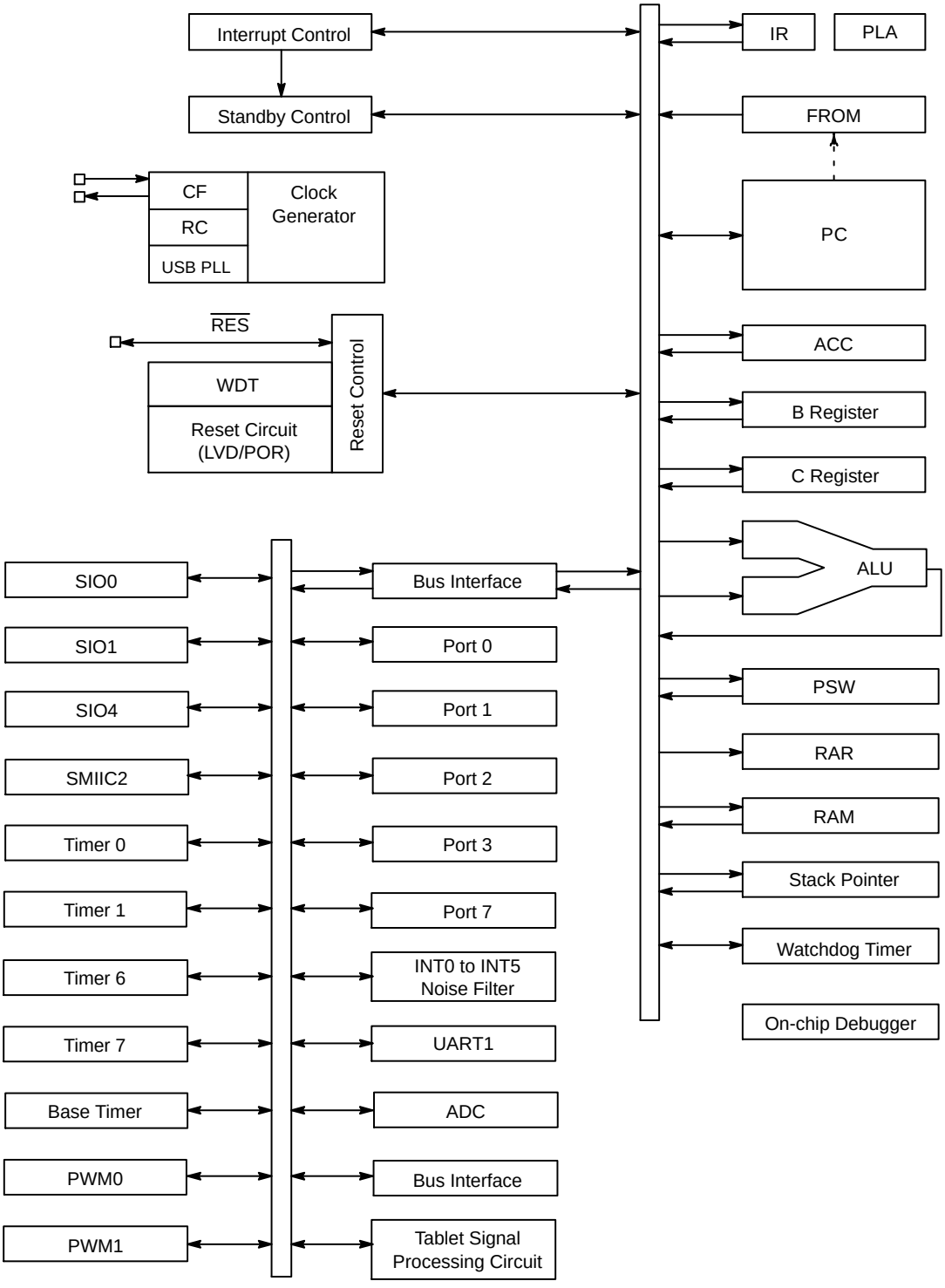


Figure 2. System Block Diagram

PIN DESCRIPTION

Table 5. PIN DESCRIPTION

Pin Name	I/O	Description	Option
$V_{SS}1$, $V_{SS}2$, $V_{SS}3$	–	Power supply pin (–)	No
$V_{DD}1$, $V_{DD}2$,	–	Power supply pin (+)	No
$V_{DD}3$	–	USB reference power supply pin	Yes
Port 0 P00 to P07	I/O	– 8−bit I/O port – I/O can be specified in 1−bit units. – Pull−up resistors can be turned on and off in 1−bit units. – HOLD release input – Port 0 interrupt input – Pin functions: P05: System clock output P06: Timer 6 toggle output P07: Timer 7 toggle output	Yes
Port 1 P10 to P17	I/O	– 8−bit I/O port – I/O can be specified in 1−bit units. – Pull−up resistors can be turned on and off in 1−bit units. – Pin functions: P10: SIO0 data output P11: SIO0 data input / bus I/O P12: SIO0 clock I/O P13: SIO1 data output / SMIIC2 data output (used in 3−wire SIO mode) P14: SIO1 data input / bus I/O / SMIIC2 bus I/O / data input P15: SIO1 clock I/O / SMIIC2 clock I/O P16: Timer 1 PWML output P17: Timer 1 PWMH output / buzzer output	Yes
Port 2 P20 to P27	I/O	– 8−bit I/O port – I/O can be specified in 1−bit units. – Pull−up resistors can be turned on and off in 1−bit units. – Pin functions: P20 to P23: INT4 input / HOLD release input / timer 1 event input / timer 0L capture input / timer 0H capture input P24 to P27: INT5 input / HOLD release input / timer 1 event input / timer 0L capture input / timer 0H capture input P20: UART1 transmit P21: UART1 receive P22: SIO4 data I/O P23: SIO4 data I/O P24: SIO4 clock I/O P25: SMIIC2 data output (used in 3−wire SIO mode) P26: SMIIC2 bus I/O / data input P27: SMIIC2 clock I/O Interrupt acknowledge type: **Rising / Falling / Rising & Falling / H level / L level** INT4 ○ ○ ○ × × INT5 ○ ○ ○ × ×	Yes
Port 3 P30 to P34	I/O	– 5−bit I/O port – I/O can be specified in 1−bit units. – Pull−up resistors can be turned on and off in 1−bit units. – Pin functions AD converter input: AN0 to AN3 (P30 to P33)	Yes

Table 5. PIN DESCRIPTION (continued)

Pin Name	I/O	Description	Option
Port 7 P70 to P73	I/O	− 4−bit I/O port − I/O can be specified in 1−bit units. − Pull−up resistor only for P70 can be turned on and off. − Pin functions: P70: INT0 input / HOLD release input / timer 0L capture input / watchdog timer output P71: INT1 input / HOLD release input / timer 0H capture input P72: INT2 input / HOLD release input / timer 0 event input / timer 0L capture input / high−speed clock counter input P73: INT3 input (input with noise filter) / timer 0 event input / timer 0H capture input Interrupt acknowledge type: **Rising / Falling / Rising & Falling / H level / L level** INT0 ○ ○ × ○ ○ INT1 ○ ○ × ○ ○ INT2 ○ ○ ○ × × INT3 ○ ○ ○ × ×	No
PWM0 PWM1	I/O	PWM0, PWM1 output ports General−purpose input ports	No
D+ D−	I/O	USB data I/O pins / general−purpose I/O ports	No
DPUP	O	1.5 kΩ pull−up resistor connection pin for D+	No
VBUS	I	USB Vbus detection pin	No
UFILT	I/O	PLL filter circuit connection pin	No
$\overline{\text{RES}}$	I/O	External reset input / internal reset output pin	No
CF1	I	Ceramic resonator input pin	No
CF2	O	Ceramic resonator output pin	No
OWP0	I/O	Debugger−dedicated pin	No
MCLK	O	Negative power supply generating clock output pin	No
MUTE	O	Used to pull down amplifier input in transmit mode	No
TCLK	O	Transmit clock output pin	No

ON−CHIP DEBUGGER PIN TREATMENT

For the treatment of the on−chip debugger pins, refer to the separately available document entitled “RD87 On−chip Debugger Installation Manual”.

RECOMMENDED UNUSED PIN TREATMENT

Table 6. RECOMMENDED UNUSED PIN TREATMENT

Pin Name	Recommended Unused Pin Treatment	
	Board	Software
P00 to P07	OPEN	Set Output Low
P10 to P17	OPEN	Set Output Low
P20 to P27	OPEN	Set Output Low
P30 to P34	OPEN	Set Output Low
P70 to P73	OPEN	Set Output Low
PWM0, PWM1	OPEN	Set Output Low
D+, D−	OPEN	Set Output Low
VBUS	Pull Down with a 100 kΩ Resistor	–
OWP0	Pull Down with a 100 kΩ Resistor	–

PORT OUTPUT TYPES

The table below lists the types of port outputs and the presence/absence of a pull−up resistor.

Data can be read into any input port even if it is in the output mode.

Table 7. PORT OUTPUT TYPES

Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07 P10 to P17 P20 to P27 P30 to P34	1 bit	1	CMOS	Programmable
		2	N−channel Open Drain	Programmable
P70	–	No	N−channel Open Drain	Programmable
P71 to P73	–	No	CMOS	No
PWM0, PWM1	–	No	CMOS	No
D+, D−	–	No	CMOS	No

USER OPTION TABLE

Table 8. USER OPTION TABLE

Option Name	Option Type	Flash-ROM Version	Option Selected in Units of	Option Setting
Port Output Type	P00 to P07	○	1 bit	CMOS
				N-channel Open Drain
	P10 to P17	○	1 bit	CMOS
				N-channel Open Drain
	P20 to P27	○	1 bit	CMOS
				N-channel Open Drain
	P30 to P34	○	1 bit	CMOS
				N-channel Open Drain
Program Start Address	–	○	–	00000h
				0FE00h
USB Regulator	USB Regulator	○	–	Use
				Nonuse
	USB Regulator (in HOLD mode)	○	–	Use
				Nonuse
	USB Regulator (in HALT mode)	○	–	Use
				Nonuse
Low-voltage Detection Reset Function	Detection Function	○	–	Enable: Use
				Disable: Nonuse
	Detection Level	○	–	7−level
Power-on Reset Function	Power-on Reset Level	○	–	8−level

USB REFERENCE POWER SUPPLY OPTION

The reference voltage for USB port output is generated by applying 4.0 V to 5.5 V to $V_{DD}1$ and activating the internal USB reference voltage circuit. The active/inactive state of the reference voltage circuit can be switched by selecting an option. The procedure for making the option selection is described below.

Table 9. USB REFERENCE POWER SUPPLY OPTION

		(1)	(2)	(3)	(4)
Option Setting	USB Regulator	Use	Use	Use	Nonuse
	USB Regulator in HOLD Mode	Use	Nonuse	Nonuse	Nonuse
	USB Regulator in HALT Mode	Use	Nonuse	Use	Nonuse
Reference Voltage Circuit Operation	Normal Operating Mode	Active	Active	Active	Inactive
	HOLD Mode	Active	Inactive	Inactive	Inactive
	HALT Mode	Active	Inactive	Active	Inactive

1. When the USB reference voltage circuit is made inactive, the level of the reference voltage for USB port output is equal to $V_{DD}1$.
2. Selection (2) and (3) are used to stop the reference voltage circuit in HALT and HOLD mode.
3. When the reference voltage circuit is activated, the current drain increases by approximately 100 μA compared with the current drain when the reference voltage circuit is inactive.

Application Circuit Example 1: $V_{DD}1 = V_{DD}2 = AV_{DD} = 3.3$ V

- Inactivate the reference voltage circuit (setting in (4)).
- Connect $V_{DD}3$ to $V_{DD}1$, $V_{DD}2$, and AV_{DD}.

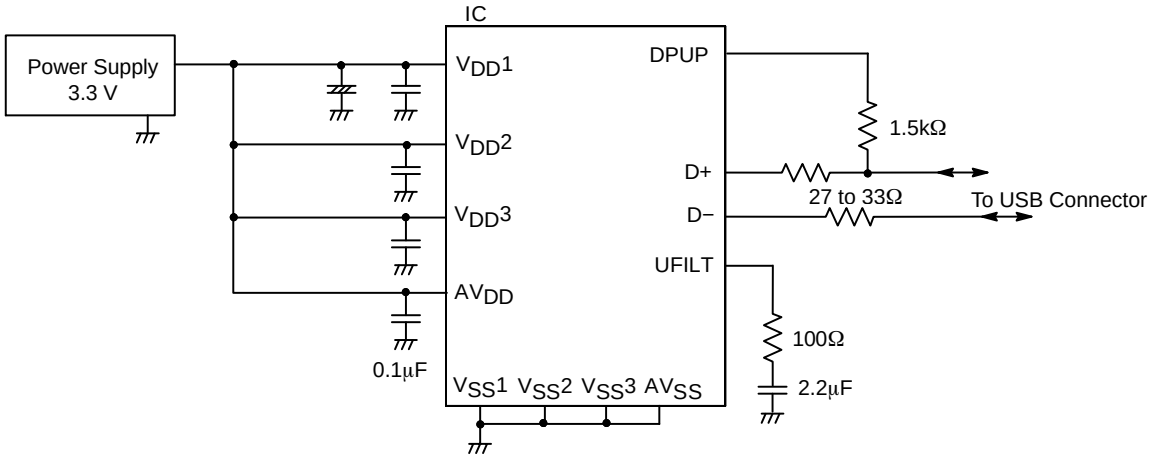


Figure 3. Application Circuit Example 1

Application Circuit Example 2: $V_{DD}1 = V_{DD}2 = AV_{DD} = 5.0$ V

- Activate the reference voltage circuit (setting in (1)).
- Disconnect $V_{DD}3$ to $V_{DD}1$, $V_{DD}2$, and AV_{DD} and insert a capacitor between $V_{DD}3$ and V_{SS}.

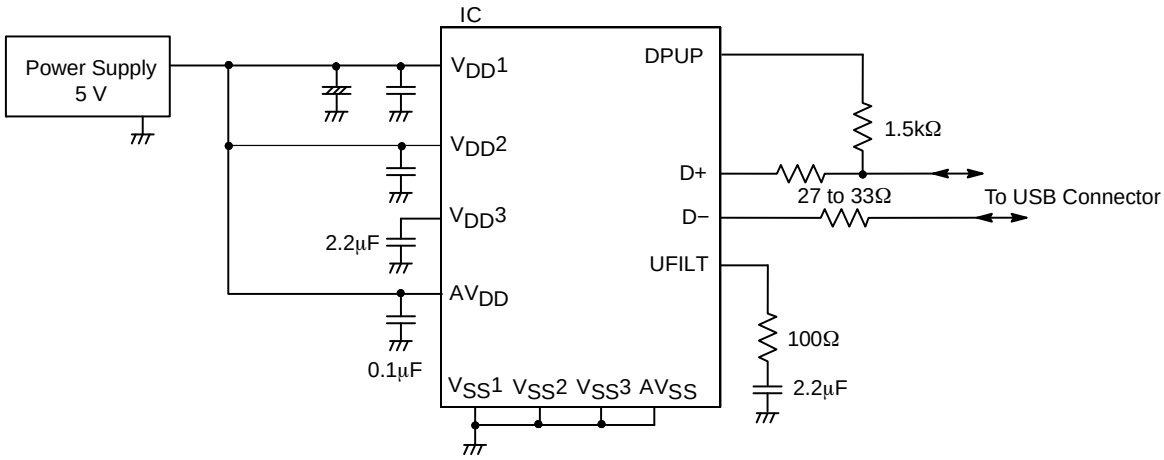


Figure 4. Application Circuit Example 2

Table 10. ABSOLUTE MAXIMUM RATINGS
(at T_A = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = AV_{SS}$ = 0 V)

Parameter		Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification			
						Min	Typ	Max	Unit
Maximum Supply Voltage		V_{DD} max	$V_{DD}1$, $V_{DD}2$, $V_{DD}3$, AV_{DD}	$V_{DD}1 = V_{DD}2 = V_{DD}3 = AV_{DD}$		−0.3		+6.5	V
Input Voltage		V_I(1)	CF1			−0.3		V_{DD}+0.3	
		V_I(2)	VBUS			−0.3		+6.5	
Input/Output Voltage		V_{IO}(1)	Ports 0,1,2,3,7 PWM0, PWM1, CF2, TCLK, MUTE, MCLK, D+, D−, DPUP, UFILT, OWP0, $\overline{RES}$, REFIN, VREF, VIN−, VIN+, VOUT, MIN, MOUT, SIN, SOUT			−0.3		V_{DD}+0.3	
High Level Output Current	Peak Output Current	IOPH(1)	Ports 0,1,2 P71 to P73	− When CMOS output type is selected. − Current at each pin		−10			mA
		IOPH(2)	Port 3	− When CMOS output type is selected. − Current at each pin		−5			
		IOPH(3)	PWM0, PWM1	Current at each pin		−20			
		IOPH(4)	TCLK, MUTE, MCLK	Current at each pin		−35			
	Average Output Current (Note 4)	IOMH(1)	Ports 0,1,2 P71 to P73	− When CMOS output type is selected. − Current at each pin		−7.5			
		IOMH(2)	Port 3	− When CMOS output type is selected. − Current at each pin		−3			
		IOMH(3)	PWM0, PWM1	Current at each pin		−15			
		IOMH(4)	TCLK, MUTE, MCLK	Current at each pin		−20			
	Total Output Current	ΣIOAH(1)	Port 0 P16, P17, P71 to P73 PWM0, PWM1	Total of all pins		−25			
		ΣIOAH(2)	P10 to P15 Port 2 MCLK	Total of all pins		−50			
		ΣIOAH(3)	Ports 0,1,2 P71 to P73 PWM0, PWM1 MCLK	Total of all pins		−75			
		ΣIOAH(4)	Port 3	Total of all pins		−10			
		ΣIOAH(5)	D+, D−	Total of all pins		−25			
		ΣIOAH(6)	TCLK, MUTE	Total of all pins		−30			
Low Level Output Current	Peak Output Current	IOPL(1)	Ports 0,1,2,7 PWM0, PWM1	Current at each pin				20	mA
		IOPL(2)	Port 3	Current at each pin				10	
		IOPL(3)	TCLK, MUTE, MCLK	Current at each pin				35	
	Average Output Current (Note 4)	IOML(1)	Ports 0,1,2,7 PWM0, PWM1	Current at each pin				15	
		IOML(2)	Port 3	Current at each pin				7.5	
		IOML(3)	TCLK, MUTE, MCLK	Current at each pin				20	
	Total Output Current	ΣIOAL(1)	Ports 0,7 P16, P17 PWM0, PWM1	Total of all pins				45	
		ΣIOAL(2)	P10 to P15 Port 2 MCLK	Total of all pins				60	
		ΣIOAL(3)	Ports 0,1,2,7 PWM0, PWM1 MCLK	Total of all pins				105	
		ΣIOAL(4)	Port 3	Total of all pins				15	
		ΣIOAL(5)	D+, D−	Total of all pins				25	
		ΣIOAL(6)	TCLK, MUTE	Total of all pins				30	

Table 10. ABSOLUTE MAXIMUM RATINGS (continued)
(at T_A = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = AV_{SS}$ = 0 V)

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification			
					Min	Typ	Max	Unit
Allowable Power Dissipation	Pd max	TQFP64 (7×7)	T_A = −40 to +85°C Mounted on the thermal resistance test board (Note 5)				340	mW
Operating Ambient Temperature	Topr				−40		+85	°C
Storage Ambient Temperature	Tstg				−55		+125	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
4. The average output current is an average value measured over 100 ms intervals.
5. 50 × 50 × 1.6t mm, glass epoxy board.

Table 11. ALLOWABLE OPERATING CONDITIONS
(at T_A = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = AV_{SS}$ = 0 V)

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification			
					Min	Typ	Max	Unit
Operating Supply Voltage (Note 6)	V_{DD}(1)	$V_{DD}1 = V_{DD}2 = V_{DD}3 = AV_{DD}$	0.245 μs ≤ tCYC ≤ 200 μs Except on-board programming		2.7		5.5	V
			0.245 μs ≤ tCYC ≤ 0.383 μs When USB circuit is running.		3.0		5.5	
Memory Retention Supply Voltage	VHD	$V_{DD}1 = V_{DD}2 = V_{DD}3 = AV_{DD}$	When in HOLD mode RAM, registor retained		2.0		5.5	
High Level Input Voltage	V_{IH}(1)	− Ports 0,1,2,3 − P71 to P73 − P70 port input/interrupt side − PWM0, PWM1		2.7 to 5.5	0.3 V_{DD} + 0.7		V_{DD}	
	V_{IH}(2)	P70 watchdog timer side		2.7 to 5.5	0.9 V_{DD}		V_{DD}	
	V_{IH}(3)	CF1, $\overline{RES}$		2.7 to 5.5	0.75 V_{DD}		V_{DD}	
	V_{IH}(4)	VBUS		2.7 to 5.5	0.75 V_{DD}		5.5	
Low Level Input Voltage	V_{IL}(1)	− Ports 0,1,2,3 − P71 to P73 − P70 port input/interrupt side		4.0 to 5.5	V_{SS}		0.1 V_{DD} + 0.4	
	V_{IL}(2)			2.7 to 4.0	V_{SS}		0.2 V_{DD}	
	V_{IL}(3)	PWM0, PWM1		4.0 to 5.5	V_{SS}		0.15 V_{DD} + 0.4	
	V_{IL}(4)			2.7 to 4.0	V_{SS}		0.2 V_{DD}	
	V_{IL}(5)	P70 watchdog timer side		2.7 to 5.5	V_{SS}		0.8 V_{DD} − 1.0	
	V_{IL}(6)	CF1, $\overline{RES}$, VBUS		2.7 to 5.5	V_{SS}		0.25 V_{DD}	
Instruction Cycle Time (Note 7)	tCYC		Except on-board programming	2.7 to 5.5	0.245		200	μs
			When USB circuit is running	3.0 to 5.5	0.245		0.383	
External System Clock Frequency	FEXCF(1)	CF1	− CF2 pin open − System clock frequency division ratio 1/1 − External system clock duty = 50 ±5%	3.0 to 5.5	0.1		12	MHz
Oscillation Frequency Range	FmCF(1)	CF1, CF2	12 MHz ceramic oscillation mode (See Figure 5).	2.7 to 5.5		12		MHz
	FmRC		Internal RC oscillation	2.7 to 5.5	0.5	1.0	2.0	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
6. V_{DD} must be held greater than or equal to 3.0 V in the flash ROM on-board programming mode.
7. Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Table 12. ELECTRICAL CHARACTERISTICS

(at T_A = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = AV_{SS}$ = 0 V)

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification			
					Min	Typ	Max	Unit
High Level Input Current	I_{IH}(1)	Ports 0,1,2,3,7 $\overline{RES}$, PWM0, PWM1, D+, D−, VBUS	Output disabled Pull−up resistor off $V_{IN} = V_{DD}$ (Including output Tr's off leakage current)	2.7 to 5.5			1	μA
	I_{IH}(2)	CF1	$V_{IN} = V_{DD}$	2.7 to 5.5			15	
Low Level Input Current	I_{IL}(1)	Ports 0,1,2,3,7 $\overline{RES}$, PWM0, PWM1, D+, D−, VBUS	Output disabled Pull−up resistor off $V_{IN} = V_{SS}$ (Including output Tr's off leakage current)	2.7 to 5.5	−1			
	I_{IL}(2)	CF1	$V_{IN} = V_{SS}$	2.7 to 5.5	−15			
High Level Output Voltage	V_{OH}(1)	Ports 0,1,2,3 P71 to P73	I_{OH} = −1 mA	4.5 to 5.5	V_{DD} − 1			V
	V_{OH}(2)		I_{OH} = −0.4 mA	3.0 to 5.5	V_{DD} − 0.4			
	V_{OH}(3)		I_{OH} = −0.2 mA	2.7 to 5.5	V_{DD} − 0.4			
	V_{OH}(4)	PWM0, PWM1 P05 (when CKO system clock output function is used)	I_{OH} = −10 mA	4.5 to 5.5	V_{DD} − 1.5			
	V_{OH}(5)		I_{OH} = −1.6 mA	3.0 to 5.5	V_{DD} − 0.4			
	V_{OH}(6)		I_{OH} = −1 mA	2.7 to 5.5	V_{DD} − 0.4			
	V_{OH}(7)	TCLK, MUTE, MCLK	25% setting I_{OH} = −1 mA	3.0 to 5.5	V_{DD} − 0.4			
	V_{OH}(8)		50% setting I_{OH} = −2 mA	3.0 to 5.5	V_{DD} − 0.4			
	V_{OH}(9)		75% setting I_{OH} = −3 mA	3.0 to 5.5	V_{DD} − 0.4			
	V_{OH}(10)		100% setting I_{OH} = −4 mA	3.0 to 5.5	V_{DD} − 0.4			
	V_{OH}(11)	DPUP	I_{OH} = −4 mA	3.0 to 5.5	V_{DD} − 0.2			
Low Level Output Voltage	V_{OL}(1)	Ports 0,1,2,7 PWM0, PWM1	I_{OL} = 10 mA	4.5 to 5.5			1.5	
	V_{OL}(2)		I_{OL} = 1.6 mA	3.0 to 5.5			0.4	
	V_{OL}(3)		I_{OL} = 1 mA	2.7 to 5.5			0.4	
	V_{OL}(4)	Port 3	I_{OL} = 1.6 mA	3.0 to 5.5			0.4	
	V_{OL}(5)		I_{OL} = 1 mA	2.7 to 5.5			0.4	
	V_{OL}(6)	TCLK, MUTE, MCLK	25% setting I_{OL} = 1 mA	3.0 to 5.5			0.4	
	V_{OL}(7)		50% setting I_{OL} = 2 mA	3.0 to 5.5			0.4	
	V_{OL}(8)		75% setting I_{OL} = 3 mA	3.0 to 5.5			0.4	
	V_{OL}(9)		100% setting I_{OL} = 4 mA	3.0 to 5.5			0.4	
Pull-up Resistance	Rpu(1)	Ports 0,1,2,3 Port 7	$V_{OH} = 0.9\ V_{DD}$	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)			2.7 to 4.5	18	50	150	
Hysteresis Voltage	VHYS	$\overline{RES}$ Ports 0,1,2,3,7 VBUS		2.7 to 5.5		$0.1V_{DD}$		V
Pin Capacitance	CP	All pins	Pins other than those under test $V_{IN} = V_{SS}$ f = 1 MHz T_A = 25°C	2.7 to 5.5		10		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 13. SERIAL I/O CHARACTERISTICS

(at T_A = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = AV_{SS}$ = 0 V)

Parameter			Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification			
							Min	Typ	Max	Unit
SIO0 SERIAL CHARACTERISTICS (Note 8)										
Serial Clock	Input Clock	Frequency	tSCK(1)	SCK0(P12)	See Figure 11	2.7 to 5.5	2			tCYC
		Low Level Pulse Width	tSCKL(1)				1			
		High Level Pulse Width	tSCKH(1)				1			
			tSCKHA(1a)		− Continuous data transmission/ reception mode − USB and SIO4 not used at the same time − See Figure 11 − (Note 9)		4			
			tSCKHA(1b)		− Continuous data transmission/ reception mode − USB used at the same time − SIO4 not used at the same time − See Figure 11 − (Note 9)		7			
			tSCKHA(1c)		− Continuous data transmission/ reception mode − USB and SIO4 used at the same time − See Figure 11 − (Note 9)		9			
	Output Clock	Frequency	tSCK(2)	SCK0(P12)	− When CMOS output type is selected − See Figure 11	2.7 to 5.5	4/3			
		Low Level Pulse Width	tSCKL(2)				1/2			tSCK
		High Level Pulse Width	tSCKH(2)				1/2			
			tSCKHA(2a)		− Continuous data transmission/ reception mode − USB and SIO4 not used at the same time − When CMOS output type is selected − See Figure 11		tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	tCYC
			tSCKHA(2b)		− Continuous data transmission/ reception mode − USB used at the same time − SIO4 not used at the same time − When CMOS output type is selected − See Figure 11		tSCKH(2) +2tCYC		tSCKH(2) +(19/3) tCYC	
			tSCKHA(2c)		− Continuous data transmission/ reception mode − USB and SIO4 used at the same time − When CMOS output type is selected − See Figure 11		tSCKH(2) +2tCYC		tSCKH(2) +(25/3) tCYC	
Serial Input	Data Setup Time		tsDI(1)	SB0(P11), SI0(P11)	− Must be specified with respect to the rising edge of SIOCLK. − See Figure 11	2.7 to 5.5	0.03			µs
	Data Hold Time		thDI(1)				0.03			
Serial Output	Input Clock	Output Delay Time	tdDO(1)	SO0(P10), SB0(P11)	− Continuous data transmission/ reception mode − (Note 10)	2.7 to 5.5			(1/3)tCYC +0.05	
			tdDO(2)		− Synchronous 8−bit mode − (Note 10)				1tCYC +0.05	
	Output Clock		tdDO(3)		− (Note 10)				(1/3)tCYC +0.05	

Table 13. SERIAL I/O CHARACTERISTICS (continued)
(at T_A = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = AV_{SS}$ = 0 V)

Parameter			Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification			
							Min	Typ	Max	Unit
SIO1 SERIAL CHARACTERISTICS (Note 8)										
Serial Clock	Input Clock	Frequency	tSCK(3)	SCK1(P15)	See Figure 11	2.7 to 5.5	2			tCYC
		Low Level Pulse Width	tSCKL(3)				1			
		High Level Pulse Width	tSCKH(3)				1			
	Output Clock	Frequency	tSCK(4)	SCK1(P15)	− When CMOS output type is selected − See Figure 11	2.7 to 5.5	2			
		Low Level Pulse Width	tSCKL(4)				1/2			tSCK
		High Level Pulse Width	tSCKH(4)				1/2			
Serial Input	Data Setup Time		tsDI(2)	SB1(P14), SI1(P14)	− Must be specified with respect to the rising edge of SIOCLK − See Figure 11	2.7 to 5.5	0.03			µs
	Data Hold Time		thDI(2)				0.03			
Serial Output	Output Delay Time		tdDO(4)	SO1(P13), SB1(P14)	− Must be specified with respect to the falling edge of SIOCLK. − Must be specified as the time up to the beginning of output state change in open drain output mode. − See Figure 11	2.7 to 5.5			(1/2)tCYC +0.05	
SIO4 SERIAL CHARACTERISTICS (Note 8)										
Serial Clock	Input Clock	Frequency	tSCK(5)	SCK4(P24)	See Figure 11	2.7 to 5.5	2			tCYC
		Low Level Pulse Width	tSCKL(5)				1			
		High Level Pulse Width	tSCKH(5)				1			
			tSCKHA(5a)		− USB and SIO0 continuous transfer mode not used at the same time − See Figure 11 − (Note 9)		4			
			tSCKHA(5b)		− USB used at the same time − SIO0 continuous transfer mode not used at the same time − See Figure 11 − (Note 9)		7			
			tSCKHA(5c)		− USB and SIO0 continuous transfer mode used at the same time − See Figure 11 − (Note 9)		10			
	Output Clock	Frequency	tSCK(6)	SCK4(P24)	− When CMOS output type is selected. − See Figure 11	2.7 to 5.5	4/3			
		Low Level Pulse Width	tSCKL(6)				1/2			tSCK
		High Level Pulse Width	tSCKH(6)				1/2			
			tSCKHA(6a)		− USB and SIO0 continuous transfer mode not used at the same time − When CMOS output type is selected − See Figure 11		tSCKH(6) +(5/3) tCYC		tSCKH(6) +(10/3) tCYC	tCYC
			tSCKHA(6b)		− USB used at the same time − SIO0 continuous transfer mode not used at the same time − When CMOS output type is selected − See Figure 11		tSCKH(6) +(5/3) tCYC		tSCKH(6) +(19/3) tCYC	
			tSCKHA(6c)		− USB and SIO0 continuous transfer mode used at the same time − When CMOS output type is selected − See Figure 11		tSCKH(6) +(5/3) tCYC		tSCKH(6) +(28/3) tCYC	

Table 13. SERIAL I/O CHARACTERISTICS (continued)
(at T_A = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = AV_{SS}$ = 0 V)

Parameter			Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification			
							Min	Typ	Max	Unit
SIO4 SERIAL CHARACTERISTICS (Note 8)										
Serial Input		Data Setup Time	tsDI(3)	SO4(P22), SI4(P23)	− Must be specified with respect to the rising edge of SIOCLK − See Figure 11	2.7 to 5.5	0.03			µs
		Data Hold Time	thDI(3)				0.03			
Serial Output		Output Delay Time	tdDO(5)	SO4(P22), SI4(P23)	− Must be specified with respect to the falling edge of SIOCLK − Must be specified as the time up to the beginning of output state change in open drain output mode − See Figure 11	2.7 to 5.5			(1/3)tCYC +0.05	
SMIIC2 SIMPLE SIO MODE I/O CHARACTERISTICS (Note 8)										
Serial Clock	Input Clock	Frequency	tSCK(7)	SM2CK0(P27), SM2CK1(P15)	See Figure 11	2.7 to 5.5	4/3			tCYC
		Low Level Pulse Width	tSCKL(7)				2/3			
		High Level Pulse Width	tSCKH(7)				2/3			
	Output Clock	Frequency	tSCK(8)	SM2CK0(P27), SM2CK1(P15)	− When CMOS output type is selected − See Figure 11	2.7 to 5.5	4/3			
		Low Level Pulse Width	tSCKL(8)				1/2			tSCK
		High Level Pulse Width	tSCKH(8)				1/2			
Serial Input	Data Setup Time		tsDI(4)	SM2DA0(P26), SM2DA1(P14)	− Must be specified with respect to the rising edge of SIOCLK − See Figure 11	2.7 to 5.5	0.03			µs
	Data Hold Time		thDI(4)				0.03			
Serial Output	Output Delay Time		tdDO(6)	SM2DO0(P25), SM2DO1(P13), SM2DA0(P26), SM2DA1(P14)	− Must be specified with respect to the falling edge of SIOCLK − Must be specified as the time up to the beginning of output state change − See Figure 11	2.7 to 5.5			(1/3)tCYC +0.05	
SMIIC0 I²C MODE I/O CHARACTERISTICS (Note 8)										
Clock	Input Clock	Frequency	tSCL	SM2CK0(P27), SM2CK1(P15)	See Figure 13	2.7 to 5.5	5			Tfilt
		Low Level Pulse Width	tSCLL				2.5			
		High Level Pulse Width	tSCLH				2			
	Output Clock	Frequency	tSCLx	SM2CK0(P27), SM2CK1(P15)	Must be specified as the time up to the beginning of output state change	2.7 to 5.5	10			
		Low Level Pulse Width	tSCLLx				1/2			tSCL
		High Level Pulse Width	tSCLHx				1/2			
SM2CK and SM2DA Pin Input Spike Suppression Time			tsp	SM2CK0(P27), SM2CK1(P15), SM2DA0(P26), SM2DA1(P14)	See Figure 13	2.7 to 5.5			1	Tfilt
Bus Release Time between Start and Stop		Input	tBUF	SM2CK0(P27), SM2CK1(P15), SM2DA0(P26), SM2DA1(P14)	See Figure 13	2.7 to 5.5	2.5			Tfilt
		Output	tBUFx		− Standard clock mode − Must be specified as the time up to the beginning of output state change		5.5			µs
					− High-speed clock mode − Must be specified as the time up to the beginning of output state change		1.6			

Table 13. SERIAL I/O CHARACTERISTICS (continued)
(at T_A = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = AV_{SS}$ = 0 V)

Parameter		Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification			
						Min	Typ	Max	Unit
SMIIC0 I²C MODE I/O CHARACTERISTICS (Note 8)									
Start/Restart Condition Hold Time	Input	tHD;STA	SM2CK0(P27), SM2CK1(P15), SM2DA0(P26), SM2DA1(P14)	− When SMIIC register control bit, SHDS = 0 − Figure 13	2.7 to 5.5	2.0			Tfilt
				− When SMIIC register control bit, SHDS = 1 − Figure 13		2.5			
	Output	tHD;STAx		− Standard clock mode − Must be specified as the time up to the beginning of output state change		4.1			µs
				− High-speed clock mode − Must be specified as the time up to the beginning of output state change		1.0			
Restart Condition Setup Time	Input	tSU;STA	SM2CK0(P27), SM2CK1(P15), SM2DA0(P26), SM2DA1(P14)	See Figure 13	2.7 to 5.5	1.0			Tfilt
	Output	tSU;STAx		− Standard clock mode − Must be specified as the time up to the beginning of output state change		5.5			µs
				− High-speed clock mode − Must be specified as the time up to the beginning of output state change		1.6			
Stop Condition Setup Time	Input	tSU;STO	SM2CK0(P27), SM2CK1(P15), SM2DA0(P26), SM2DA1(P14)	See Figure 13	2.7 to 5.5	1.0			Tfilt
	Output	tSU;STOx		− Standard clock mode − Must be specified as the time up to the beginning of output state change		4.9			µs
				− High-speed clock mode − Must be specified as the time up to the beginning of output state change		1.1			
Data Hold Time	Input	tHD;DAT	SM2CK0(P27), SM2CK1(P15), SM2DA0(P26), SM2DA1(P14)	See Figure 13	2.7 to 5.5	0			Tfilt
	Output	tHD;DATx		− Must be specified as the time up to the beginning of output state change		1		1.5	
Data Setup Time	Input	tSU;DAT	SM2CK0(P27), SM2CK1(P15), SM2DA0(P26), SM2DA1(P14)	See Figure 13	2.7 to 5.5	1			Tfilt
	Output	tSU;DATx		− Must be specified as the time up to the beginning of output state change		1tSCL−1.5Tfilt			

8. These specifications are theoretical values. Be sure to add margin depending on its use.
9. To use serial-clock-input in continuous transmission/reception mode, a time from SI0RUN being set when serial clock is high to the falling edge of the first serial clock must be longer than tSCKHA.
10. Must be specified with respect to the falling edge of SIOCLK. Must be specified as the time up to the beginning of output state change in open drain output mode. See Figure 11.
11. The value of Tfilt is determined by the values of the register SMIC2BRG, bits 7 and 6 (BRP1, BRP0) and the system clock frequency.

BRP1	BRP0	Tfilt
0	0	(1/3)tCYC×1
0	1	(1/3)tCYC×2
1	0	(1/3)tCYC×3
1	1	(1/3)tCYC×4

Set the value of the BRP1 and BRP0 bits so that the value of Tfilt falls within the following value range: 250 ns ≥ Tfilt > 140 ns

12. For standard clock mode operation, set up the SMIC2BRG register so that the following conditions are satisfied:
250 ns ≥ Tfilt > 140 ns; BRDQ (bit5) = 1; SCL frequency value ≤ 100 kHz

For high-speed clock mode operation, set up the SMIC2BRG register so that the following conditions are satisfied:
250 ns ≥ Tfilt > 140 ns; BRDQ (bit5) = 0; SCL frequency value ≤ 400 kHz

Table 14. PULSE INPUT CONDITIONS

(at T_A = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = AV_{SS}$ = 0 V)

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	Min	Typ	Max	Unit
High/Low Level Pulse Width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72), INT4(P20 to P23), INT5(P24 to P27)	− Interrupt source flag can be set − Event input to timers 0,1 is enabled	2.7 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3 (P73) when noise filter time constant is 1/1.	− Interrupt source flag can be set − Event input to timer 0 is enabled	2.7 to 5.5	2			
	tPIH(3) tPIL(3)	INT3 (P73) when noise filter time constant is 1/32.	− Interrupt source flag can be set − Event input to timer 0 is enabled	2.7 to 5.5	64			
	tPIH(4) tPIL(4)	INT3 (P73) when noise filter time constant is 1/128.	− Interrupt source flag can be set − Event input to timer 0 is enabled	2.7 to 5.5	256			
	tPIL(5)	$\overline{RES}$	Resetting is enabled	2.7 to 5.5	200			μs

Table 15. AD CONVERTER CHARACTERISTICS (10-BIT AD CONVERSION MODE)

(at T_A = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = AV_{SS}$ = 0 V)

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	Min	Typ	Max	Unit
Resolution	N	AN0(P30) to AN3(P33) AN4(SOUT)		2.7 to 5.5		10		bit
Absolute Accuracy	ET		(Note 13)	2.7 to 5.5			±4	LSB
Conversion Time	TCAD		See conversion time calculation formula (Note 14)	2.7 to 5.5	13		41	μs
Analog Input Voltage Range	VAIN			2.7 to 5.5	V_{SS}		V_{DD}	V
Analog Port Input Current	IAINH		VAIN = V_{DD}	2.7 to 5.5			1	μA
	IAINL		VAIN = V_{SS}	2.7 to 5.5	−1			

13. The quantization error (±1/2LSB) is excluded from the absolute accuracy. The absolute accuracy is measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.
14. The conversion time refers to the period from the time an instruction for starting a conversion process is executed until the time the conversion result register is loaded with a complete digital conversion value corresponding to the analog input value.
    The conversion time is doubled in the following cases:
    - The AD conversion is performed for the first time in the 10-bit AD conversion mode after a system reset.
    - The AD conversion is performed for the first time after the AD conversion mode is switched from 8-bit to 10-bit conversion mode.

Conversion Time Calculation Formula

10−bit AD conversion mode: TCAD (conversion time) = ((40 / (AD frequency division ratio)) + 2) × (1/3) × tCYC

Table 16. RECOMMENDED OPERATING CONDITIONS

External Oscillator FMCF [MHz]	Supply Voltage Range V_{DD} [V]	System Clock Frequency Division Ratio (SYSDIV)	Cycle Time tCYC [ns]	AD Frequence Division Ratio (ADDIV)	Conversion Time (TCAD) [μs]
					10 Bit AD
12	2.7 to 5.5	1/1	250	1/4	13.5

Table 17. POWER-ON RESET (POR) CHARACTERISTICS

(at T_A = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = AV_{SS}$ = 0 V)

Parameter	Symbol	Conditions	Specification				
			Option Selection Voltage	Min	Typ	Max	Unit
POR Release Voltage	PORRL	Select from option. (Note 15)	1.67 V	1.55	1.67	1.79	V
			1.97 V	1.85	1.97	2.09	
			2.07 V	1.95	2.07	2.19	
			2.37 V	2.25	2.37	2.49	
			2.57 V	2.45	2.57	2.69	
			2.87 V	2.75	2.87	2.99	
			3.86 V	3.73	3.86	3.99	
			4.35 V	4.21	4.35	4.49	
Detection Voltage Undefined State	POUKS	See Figure 15 (Note 16)			0.7	0.95	
Power Supply Rise Time	PORIS	Power supply rise time from V_{DD} = 0 V to 1.6 V				100	ms

15. The POR reset level can be selected from 8 levels only when is “Disable” is selected in the LVD reset function option.
16. POR is in undefined state before transistors start operation.

Table 18. LOW VOLTAGE DETECTION RESET (LVD) CHARACTERISTICS

(at T_A = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = AV_{SS}$ = 0 V)

Parameter	Symbol	Conditions	Specification				
			Option Selection Voltage	Min	Typ	Max	Unit
LVD Reset Voltage (Note 18)	LVDET	Select from option. See Figure 16. (Note 17) (Note 19)	1.91 V	1.81	1.91	2.01	V
			2.01 V	1.91	2.01	2.11	
			2.31 V	2.21	2.31	2.41	
			2.51 V	2.41	2.51	2.61	
			2.81 V	2.71	2.81	2.91	
			3.79 V	3.69	3.79	3.89	
			4.28 V	4.18	4.28	4.38	
LVD Hysteresis Width	LVHYS		1.91 V		55		mV
			2.01 V		55		
			2.31 V		55		
			2.51 V		55		
			2.81 V		55		
			3.79 V		60		
			4.28 V		65		
Detection Voltage Undefined State	LVUKS	See Figure 16 (Note 20)			0.7	0.95	V
Low Voltage Detection Minimum Width (Response Sensitivity))	TLVDW	LVDET−0.5 V See Figure 17		0.2			ms

17. The LVD reset level can be selected from 7 levels only when “Enable” is selected in the LVD reset function option.
18. LVD reset voltage specification values do not include hysteresis voltage.
19. LVD reset voltage may exceed its specification values when port output state changes or when a large current flows to the port.
20. LVD is in an undefined state before transistors start operation.

Table 19. CONSUMPTION CURRENT CHARACTERISTICS

(at T_A = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = AV_{SS}$ = 0 V)

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification			
					Min	Typ	Max	Unit
Normal Mode Consumption Current (Note 21) (Note 22)	IDDOP(1)	$V_{DD}1=V_{DD}2=V_{DD}3=AV_{DD}$	− FmCF = 12 MHz ceramic oscillation mode − System clock set to 12 MHz side − nternal PLL oscillator stopped − Internal RC oscillator stopped − USB circuit stopped − 1/1 frequency division ratio	4.5 to 5.5		6.6	12	mA
				3.0 to 3.6		3.8	6.5	
Normal Mode Consumption Current (Note 21) (Note 22)	IDDOP(2)	$V_{DD}1=V_{DD}2=V_{DD}3=AV_{DD}$	− FmCF = 12 MHz ceramic oscillation mode − System clock set to 12 MHz side − Internal PLL oscillator started − Internal RC oscillator stopped − USB circuit started − 1/1 frequency division ratio	4.5 to 5.5		11	19	mA
				3.0 to 3.6		5.6	9.8	
	IDDOP(3)		− FmCF = 12 MHz ceramic oscillation mode − System clock set to 6 MHz side − Internal RC oscillator stopped − 1/2 frequency division ratio	4.5 to 5.5		3.9	6.8	
				3.0 to 3.6		2.2	3.8	
				2.7 to 3.0		1.9	3.0	
	IDDOP(4)		− FmCF = 0 Hz (oscillation stopped) − System clock set to internal RC oscillator − 1/2 frequency division ratio	4.5 to 5.5		0.28	0.89	
				3.0 to 3.6		0.17	0.52	
				2.7 to 3.0		0.15	0.43	
HALT Mode Consumption Current (Note 21) (Note 22)	IDDHALT(1)	$V_{DD}1=V_{DD}2=V_{DD}3=AV_{DD}$	− HALT mode − FmCF = 12 MHz ceramic oscillation mode − System clock set to 12 MHz side − Internal PLL oscillator stopped − Internal RC oscillator stopped − USB circuit stopped − 1/1 frequency division ratio	4.5 to 5.5		3.6	6.4	mA
				3.0 to 3.6		1.9	3.4	
	IDDHALT(2)		− HALT mode − FmCF = 12 MHz ceramic oscillation mode − System clock set to 12 MHz side − Internal PLL oscillator started − Internal RC oscillator stopped − USB circuit started − 1/1 frequency division ratio	4.5 to 5.5		7.2	14	
				3.0 to 3.6		3.7	6.6	
	IDDHALT(3)		− HALT mode − FmCF = 12 MHz ceramic oscillation mode − System clock set to 6 MHz side − Internal RC oscillator stopped − 1/2 frequency division ratio	4.5 to 5.5		2.3	4.2	
				3.0 to 3.6		1.2	2.1	
				2.7 to 3.0		0.94	1.6	
	IDDHALT(4)		− HALT mode − FmCF = 0 Hz (oscillation stopped) − System clock set to internal RC oscillator − 1/2 frequency division ratio	4.5 to 5.5		0.13	0.41	
				3.0 to 3.6		0.08	0.24	
				2.7 to 3.0		0.07	0.19	
HOLD Mode Consumption Current (Note 21) (Note 22)	IDDHOLD(1)	$V_{DD}1=V_{DD}2=V_{DD}3=AV_{DD}$	− HOLD mode − CF1=V_{DD} or open (external clock mode)	4.5 to 5.5		0.09	40	μA
				3.0 to 3.6		0.04	17	
				2.7 to 3.0		0.03	13	
	IDDHOLD(2)		− HOLD mode − When LVD option is selected − CF1 = V_{DD} or open (external clock mode)	4.5 to 5.5		2.9	44	
				3.0 to 3.6		2.3	20	
				2.7 to 3.0		2.1	16	

21. The consumption current values do not include the current that flows into the output transistors, internal pull−up resistors and tablet analog signal processing circuit.
22. Unless LVD (low voltage detection) is specified, the current consumption for LVD operation is not included.

Table 20. USB CHARACTERISTICS AND TIMING
(at T_A = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = AV_{SS}$ = 0 V)

Parameter	Symbol	Conditions	Specification			
			Min	Typ	Max	Unit
High Level Output	$V_{OH(USB)}$	15 kΩ ±5% to GND	2.8		3.6	V
Low Level Output	$V_{OL(USB)}$	1.5 kΩ ±5% to 3.6 V	0.0		0.3	V
Output Signal Crossover Voltage	V_{CRS}		1.3		2.0	V
Differential Input Sensitivity	V_{DI}	|(D+)−(D−)|	0.2			V
Differential Input Common Mode Range	V_{CM}		0.8		2.5	V
High Level Input	$V_{IH(USB)}$		2.0			V
Low Level Input	$V_{IL(USB)}$				0.8	V
USB Data Rise Time	t_R	− R_S = 27 to 33 Ω, C_L = 50 pF − $V_{DD}3$ = 3.0 to 3.6 V	4		20	ns
USB Data Fall Time	t_F	− R_S = 27 to 33 Ω, C_L = 50 pF − $V_{DD}3$ = 3.0 to 3.6 V	4		20	ns

Table 21. F−ROM PROGRAMMING CHARACTERISTICS
(at T_A = +10°C to +55°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = AV_{SS}$ = 0 V)

Parameter	Symbol	Pin	Conditions	V_{DD}[V]	Specification			
					Min	Typ	Max	Unit
On-board Programming Current	IDDFW(1)	$V_{DD}1$	Excluding power dissipation in the microcontroller block	3.0 to 5.5		5	10	mA
Programming Time	tFW(1)		Erase operation	3.0 to 5.5		20	30	ms
	tFW(2)		Write operation			40	60	μs

Main System Clock Oscillator Circuit

Use only external circuit constants with which the resonator vendor confirmed normal and stable oscillation of the oscillator circuit.

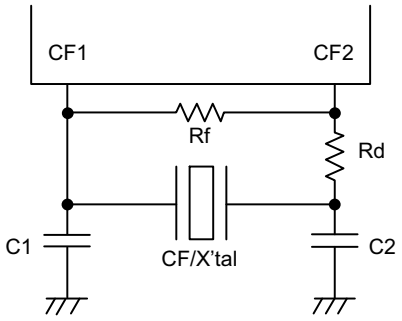


Figure 5. Main System Clock Oscillator Circuit

NOTE: The components that are involved in oscillation should be placed as close to the resonator and to one another as possible with the shortest possible trace because they are vulnerable to the influences of the circuit pattern.

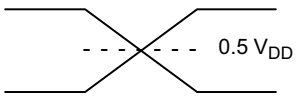
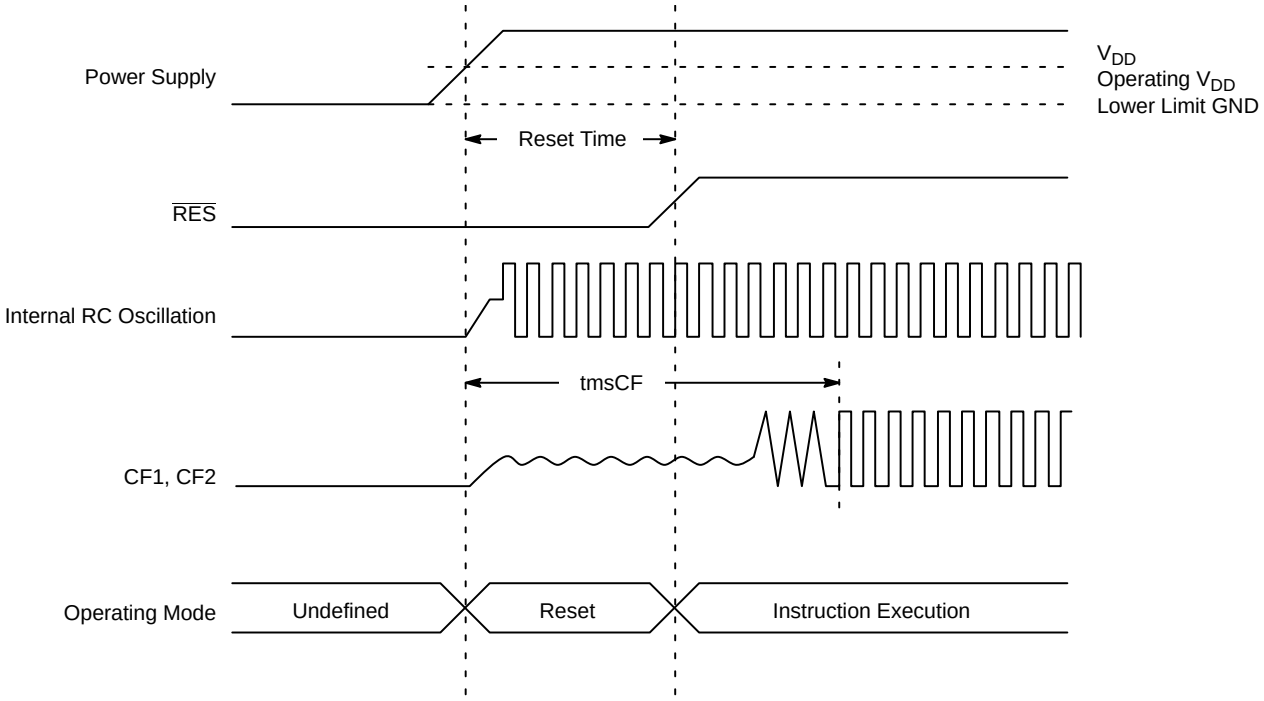
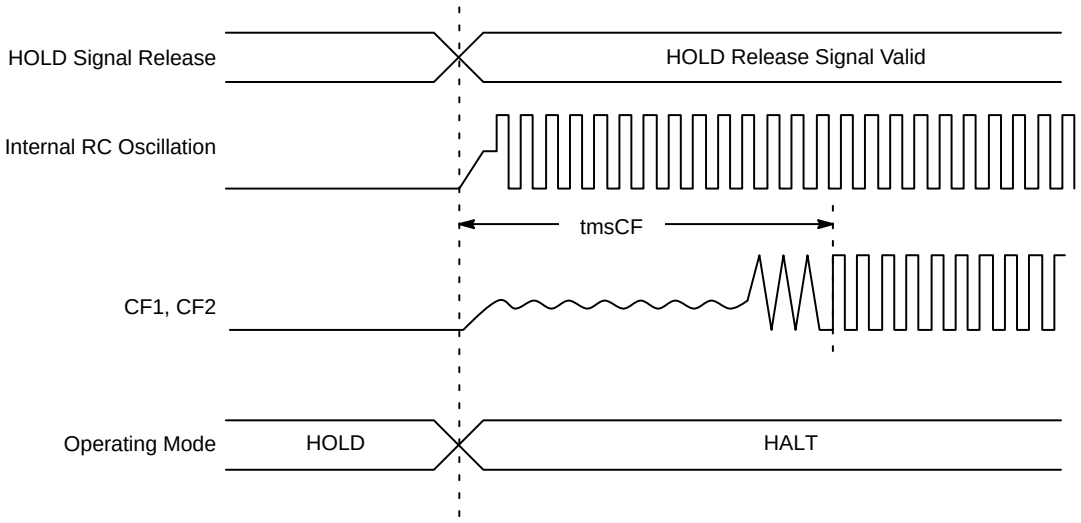


Figure 6. AC Timing Measurement Point

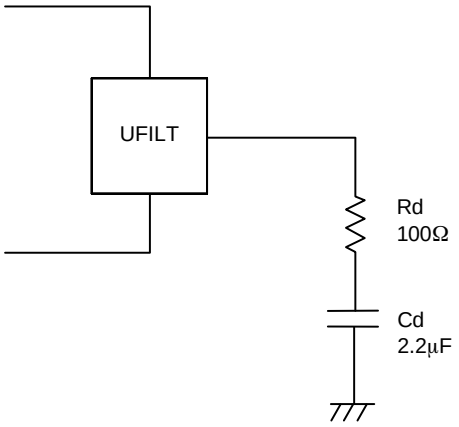


Reset Time and Oscillation Stabilization Time



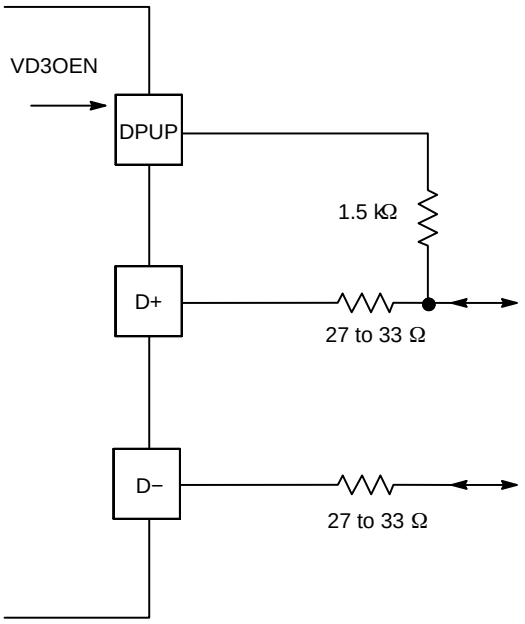
HOLD Release Signal and Oscillation Stabilization Time

Figure 7. Oscillation Stabilization Time



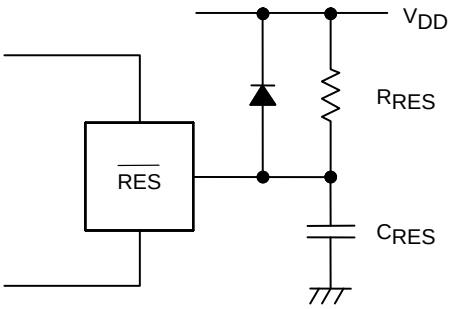
Note:
To generate the 48 MHz clock for the USB using the internal PLL circuit, it is necessary to connect the filter circuit shown in the left figure to the UFILT pin.

Figure 8. External Filter Circuit for the Internal USB−dedicated PLL Circuit



Note:
The pull-up resistor for D+ must be implemented so that it can be turned on or off according to the presence or absence of Vbus.

Figure 9. USB Port Peripheral Circuit



Note:
Determine the value of C_{RES} and R_{RES} so that a reset is triggered for 200 μs after the supply voltage goes above the lower limit of the operating voltage.

Figure 10. Sample Reset Circuit

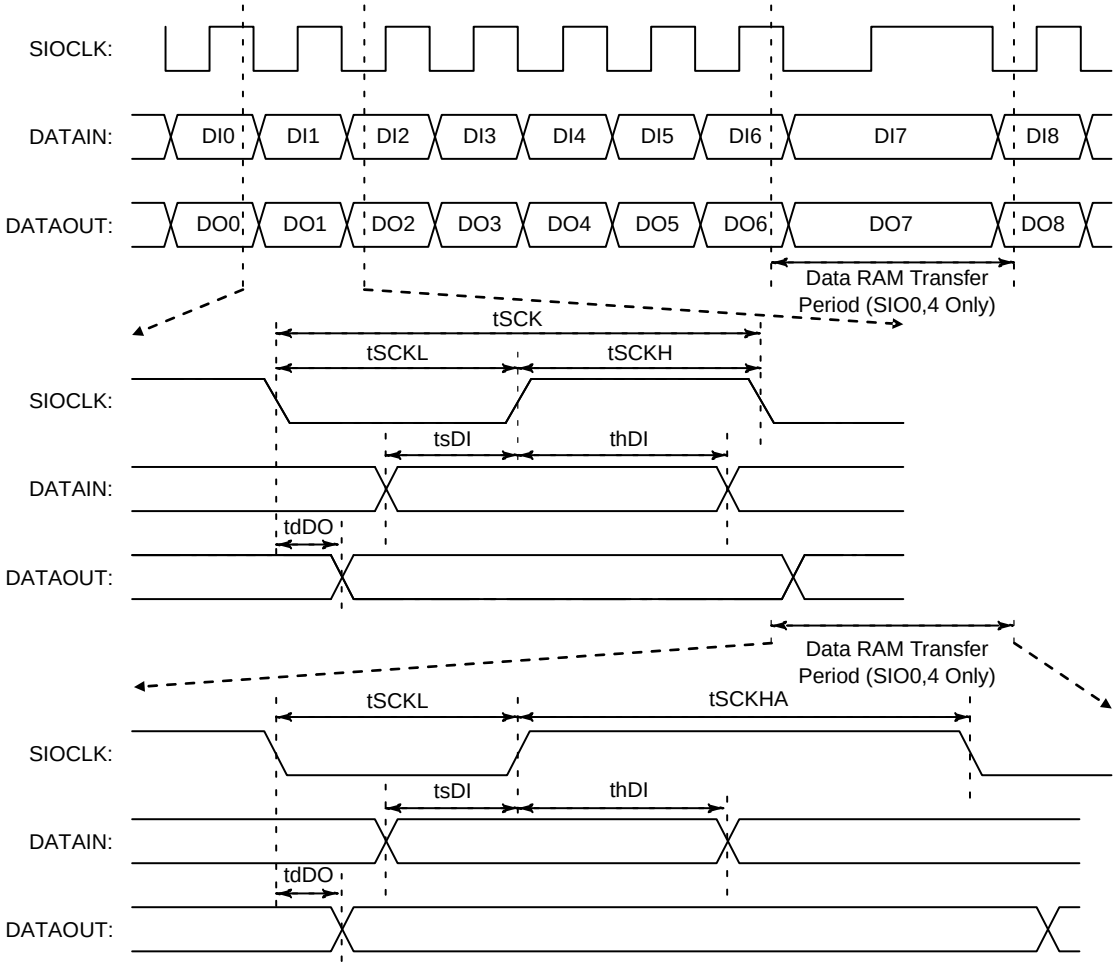


Figure 11. Serial Input/Output Waveform

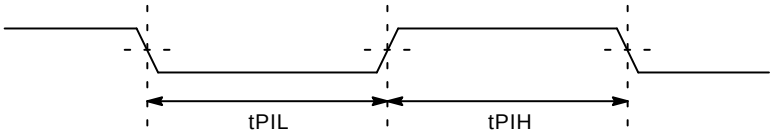
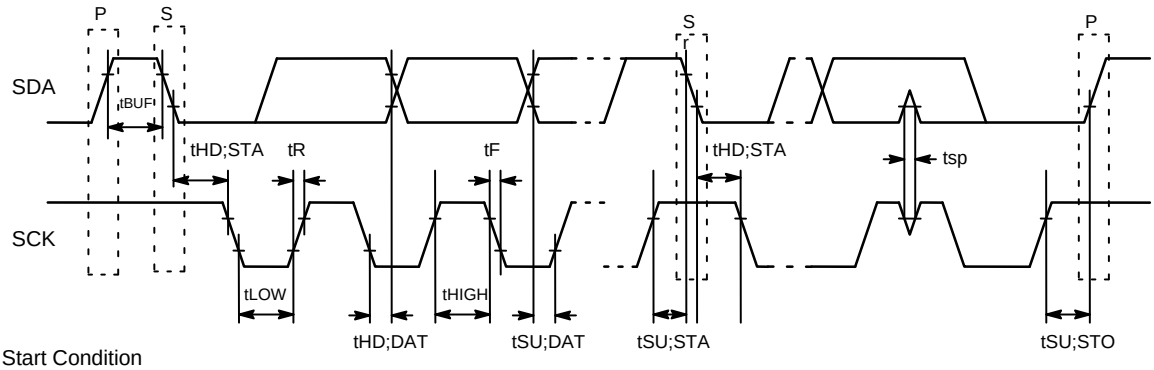


Figure 12. Pulse Input Timing Waveform



S: Start Condition
P: Stop Condition
Sr: Restart Condition

Figure 13. I^2C Timing

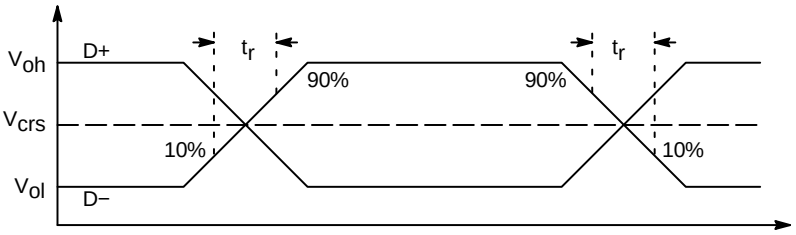


Figure 14. USB Data Signal Timing and Voltage Level

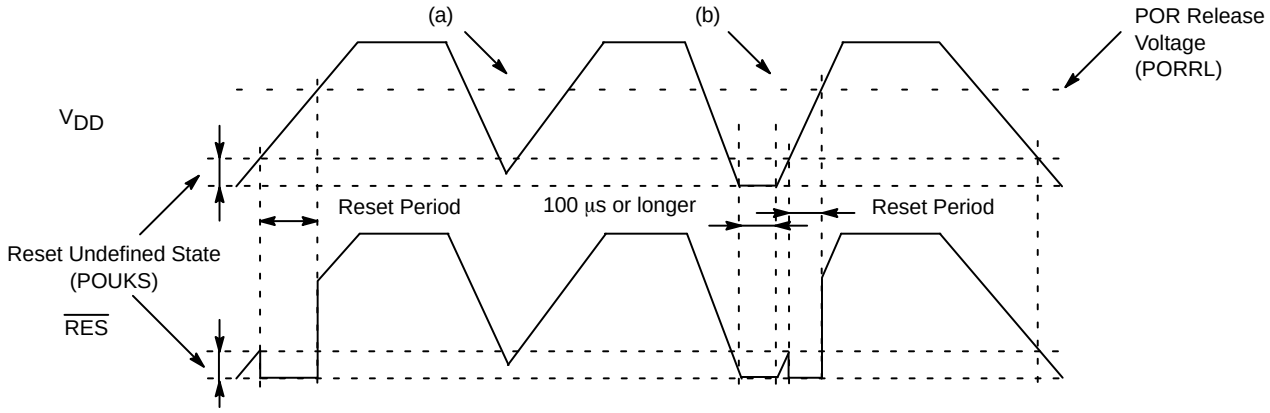


Figure 15. Sample Operating Waveforms When Only POR is Used (LVD not Selected) (at Reset Pin with P_{RES} Pull−up Resistor Only)

- The POR function generates a reset only when power is turned on starting at the V_{SS} level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the V_{SS} level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function or implement an external reset circuit as shown below.
- A reset is generated only when the power level goes down to the V_{SS} level as shown in (b) and power is turned on again after this condition continues for 100 μs or longer.

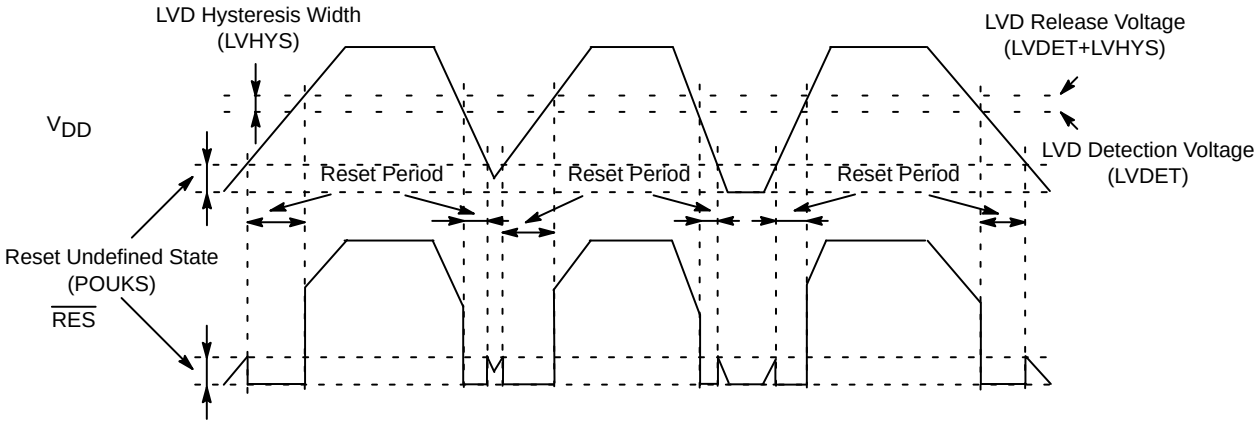


Figure 16. Example of POR + LVD Mode Waveforms (at Reset Pin with P_{RES} Pull−up Resistor Only)

- A reset is generated when power is turned on and when the power voltage falls.
- LVD has a hysteresis width (LVHYS) so that entry into and exit from the reset sequence will not be repeated near the detection level.

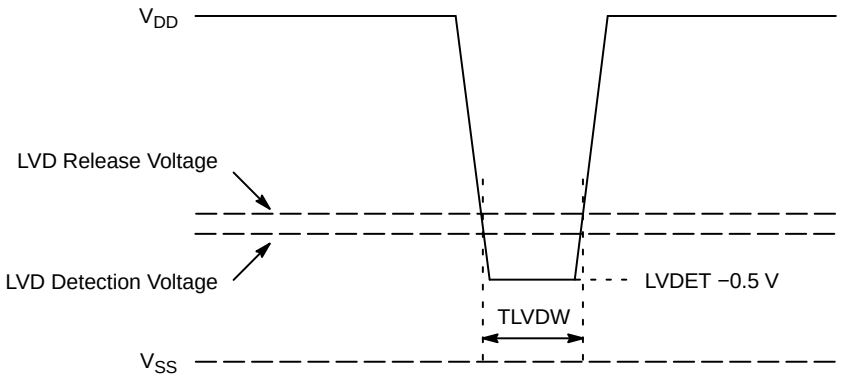


Figure 17. Minimum Low Voltage Detection Width (Momentary Power Loss/Fluctuation Sample Waveform)

The rest of this document describes the specifications for the tablet signal processing circuit.

Functional Block Diagram and Peripheral Circuit Configuration

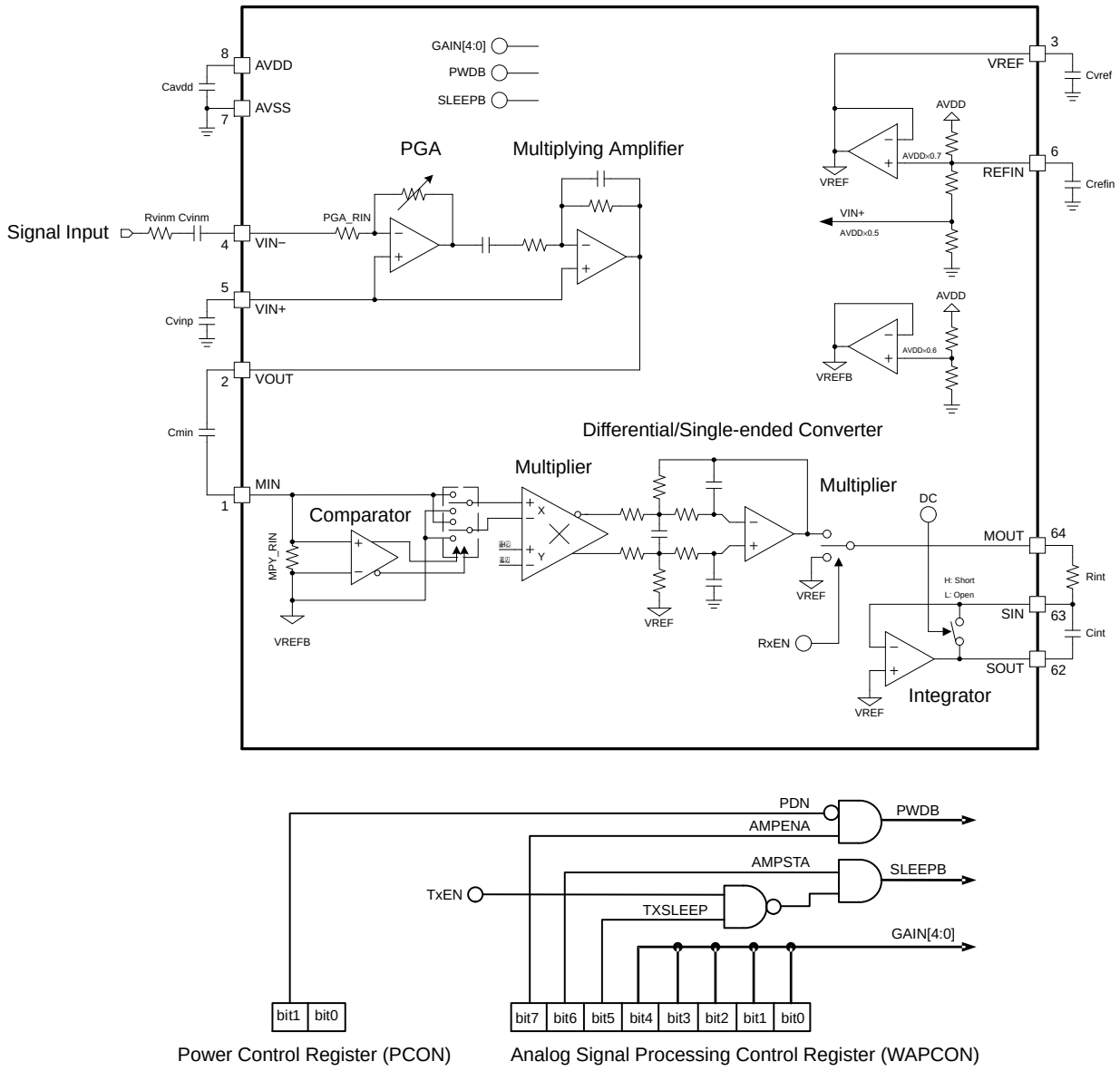


Figure 18. Functional Block Diagram and Peripheral Circuit Configuration

Table 22. PIN DESCRIPTION

Pin Name	I/O	Description	Recommended External Constants
AV_{SS}	−	GND pin	
AV_{DD}	−	Power pin	Cavdd = 0.1 μF+10 μF
REFIN	I	Reference voltage input	Crefin = 0.1 μF
VREF	O	Reference voltage output	Cvref = 0.1 μF or or more is required (Note 23)
VIN−	I	PGA (Programmable Gain Amplifier) signal input	Cvinm = 300 pF, Rvinm = 1.0 kΩ (Note 24)
VIN+	I	PGA (Programmable Gain Amplifier) reference voltage input	Cvinp = 300 pF
VOUT	O	PGA (Programmable Gain Amplifier) output	
MIN	I	Multiplier (full-wave rectifier circuit) input	Cmin = 100 pF AC coupled
MOUT	O	Multiplier (full-wave rectifier circuit) output	
SIN	I	Integrator input	Rint = 1.0 kΩ (Note 25)
SOUT	O	Integrator output/AD converter input port (AN4)	Cint = 1500 pF

23. Cvref also serves as the phase compensation capacitor for the VREF buffer amplifier. An external capacitor of 0.1 μF or more is required throughout the operating temperature range.
24. Cvinm and Rvinm will affect the gain of the programmable gain amplifier.
The attenuation at the VIN-pin as viewed from the signal input is given by the following formula:

$$\text{Attenuation [dB]} = 20 \cdot \log_{10}\left(\frac{2\pi \cdot f \cdot C_{vinm} \cdot PGA\_RIN}{\sqrt{1 + \left[2\pi \cdot f \cdot C_{vinm} \cdot \left(R_{vinm} + PGA\_RIN\right)\right]^2}}\right)$$

25. Rint is subjected to constraints imposed by the output current of the full-wave rectifier circuit and needs to be 700 Ω or more throughout the operating temperature range.

Table 23. INTERNAL PIN DESCRIPTION

Internal Pin Name	I/O	Description	Remarks
PWDB	I	Power down control	H: Normal operation, L: Power down
SLEEPB	I	Sleep control	H: Normal operation, L: Sleep mode
GAIN[4:0]	I	PGA (Programmable Gain Amplifier) gain control	
TxEN	I	Transmission period flag	H: During the transmission period, L: Other than the transmission period
RxEN	I	Integrator input signal switching control	H: Multiplier output, L: VREF
DC	I	Integrator output reset control	H: SIN−SOUT shorted, L: SIN−SOUT open

Table 24. ALLOWABLE OPERATING CONDITIONS

(at T_A = −40°C to +85°C, AV_{SS} = 0 V)

Parameter	Symbol	Pin	Conditions	Specification			
				Min	Typ	Max	Unit
Operating Supply Voltage	V_{DD}	AV_{DD}		2.7	3.3	5.5	V
Maximum Output Load Capacitance	Cp_VOUT	VOUT				20	pF
	Cp_MOUT	MOUT				20	pF
	Cp_SOUT	SOUT				50	pF

Table 25. ELECTRICAL CHARACTERISTICS (DC)
(at T_A = 25°C, V_{DD} = 3.3 V, AV_{SS} = 0 V)

Parameter	Symbol	Pin/Remarks	Conditions	Specification			
				Min	Typ	Max	Unit
REFIN Open Voltage	VREFIN	REFIN			0.7*V_{DD}		V
VREF Output Voltage	VREFOUT	VREF			0.7*V_{DD}		V
PGA Input Open Voltage	PGA_COM	VIN−, VIN+			0.5*V_{DD}		V
PGA Input Resistance	PGA_RIN	VIN−			1.7k		Ω
Multiplier Input Open Voltage	MPY_COM	MIN			0.6*V_{DD}		V
Multiplier Input Resistance	MPY_RIN	MIN			30k		Ω
Multiplier Output Range	MPY_VOUT	MOUT	RxEN = H	0.3		V_{DD}−0.3	V
Multiplier Output Offset	MPY_OFFH	MOUT	RxEN = H, with respect to VREF			±25	mV
	MPY_OFFL	MOUT	RxEN = L, with respect to VREF			±10	mV
Integrator Output Range	ITG_VOUT	SOUT	DC = L	0.3		V_{DD}−0.3	V
Integrator Output Current	ITG_IOUT	SOUT	DC = L	−1		1	mA
Integrator Output Offset	ITG_OFF	SOUT	DC = H, with respect to VREF			±7	mV
Input Pin Capacitance	Cp_IN	REFIN, VIN−, VIN+, MIN, SIN			10		pF
Consumption Current	I_{DD}	AV_{DD}	PWDB = H, SLEEPB = H		4.3		mA
	I_{sleep}	AV_{DD}	PWDB = H, SLEEPB = L		1.0		mA
	I_{pwrdwn}	AV_{DD}	PWDB = L			1.0	μA

Table 26. ELECTRICAL CHARACTERISTICS (AC)
(at T_A = 25°C, V_{DD} = 3.3 V, AV_{SS} = 0 V, VOUT load 20 pF, MOUT load 20 pF, SOUT load 50 pF)

Parameter	Symbol	Pin/Remarks	Conditions	Specification			
				Min	Typ	Max	Unit
PGA Input Amplitude	PGA_VIN	VIN−	667 kHz sine wave		24	200	mVpp
PGA Output Amplitude	PGA_VOUT	VOUT	667 kHz sine wave		350	600	mVpp
PGA Input Frequency Band	PGA_FIN	VIN−	Sine wave	500	667	750	kHz
PGA Gain (Note 26)	PGA_Ga	VOUT	Not including Rvinm and Cvinm	0.0		44.0	dB
PGA Output Noise	PGA_Vn	VOUT	PGA gain = 34.5 dB VIN−/VIN+ input-to-ground capacitance of 0.1 μF			0.66	μV/√Hz
Multiplier Input Amplitude	MPY_VIN	MIN	667 kHz sine wave		350	600	mVpp
Multiplier Frequency Band	MPY_Fc	MOUT	RxEN = H	1.0	1.3	1.6	MHz
Multiplier Gain	MPY_Ga	MOUT	RxEN = H	0.85	1.00	1.15	Times

26. See the next page for details on the relationship between the PGA gain and GAIN[4:0].

Table 27. PGA GAIN CHARACTERISTICS

(at T_A = 25°C, V_{DD} = 3.3 V, AV_{SS} = 0 V, not including Rvinm and Cvinm)

Parameter	Symbol	Pin/Remarks	Conditions	Specification			
				Min	Typ	Max	Unit
PGA Gain	PGA_Ga	VOUT	GAIN[4:0] = 0x00	0.0	1.0	3.0	dB
			GAIN[4:0] = 0x01	1.4	2.4	4.4	
			GAIN[4:0] = 0x02	2.9	3.9	5.9	
			GAIN[4:0] = 0x03	4.3	5.3	6.8	
			GAIN[4:0] = 0x04	5.7	6.7	8.2	
			GAIN[4:0] = 0x05	7.2	8.2	9.7	
			GAIN[4:0] = 0x06	8.6	9.6	11.1	
			GAIN[4:0] = 0x07	10.0	11.0	12.5	
			GAIN[4:0] = 0x08	11.4	12.4	13.9	
			GAIN[4:0] = 0x09	12.9	13.9	15.4	
			GAIN[4:0] = 0x0A	14.3	15.3	16.8	
			GAIN[4:0] = 0x0B	15.7	16.7	18.2	
			GAIN[4:0] = 0x0C	17.2	18.2	19.7	
			GAIN[4:0] = 0x0D	18.6	19.6	21.1	
			GAIN[4:0] = 0x0E	20.0	21.0	22.5	
			GAIN[4:0] = 0x0F	21.5	22.5	24.0	
			GAIN[4:0] = 0x10	22.9	23.9	25.4	
			GAIN[4:0] = 0x11	24.3	25.3	26.8	
			GAIN[4:0] = 0x12	25.8	26.8	28.3	
			GAIN[4:0] = 0x13	27.2	28.2	29.7	
			GAIN[4:0] = 0x14	28.6	29.6	31.1	
			GAIN[4:0] = 0x15	30.1	31.1	32.6	
			GAIN[4:0] = 0x16	31.5	32.5	34.0	
			GAIN[4:0] = 0x17	32.9	33.9	35.4	
			GAIN[4:0] = 0x18	34.3	35.3	36.8	
			GAIN[4:0] = 0x19	35.8	36.8	38.3	
			GAIN[4:0] = 0x1A	37.2	38.2	39.7	
			GAIN[4:0] = 0x1B	38.6	39.6	41.1	
			GAIN[4:0] = 0x1C	40.1	41.1	42.6	
			GAIN[4:0] = 0x1D−0x1F	41.5	42.5	44.0	

Table 28. ELECTRICAL CHARACTERISTICS (TIMING)
(at T_A = 25°C, V_{DD} = 3.3 V, AV_{SS} = 0 V)

Parameter	Symbol	Pin/Remarks	Conditions	Specification			
				Min	Typ	Max	Unit
Integrator Discharge Time	Tdis	SOUT	Rint = 1.0 kΩ, Cint = 1500 pF See Figure 19	3			μs
Mute Recovery Time	Tmute	VOUT, MOUT, SOUT	See Figure 19			5	μs
Sleep Recovery Time	Tslp	VOUT, MOUT, SOUT	See Figure 20			5	μs

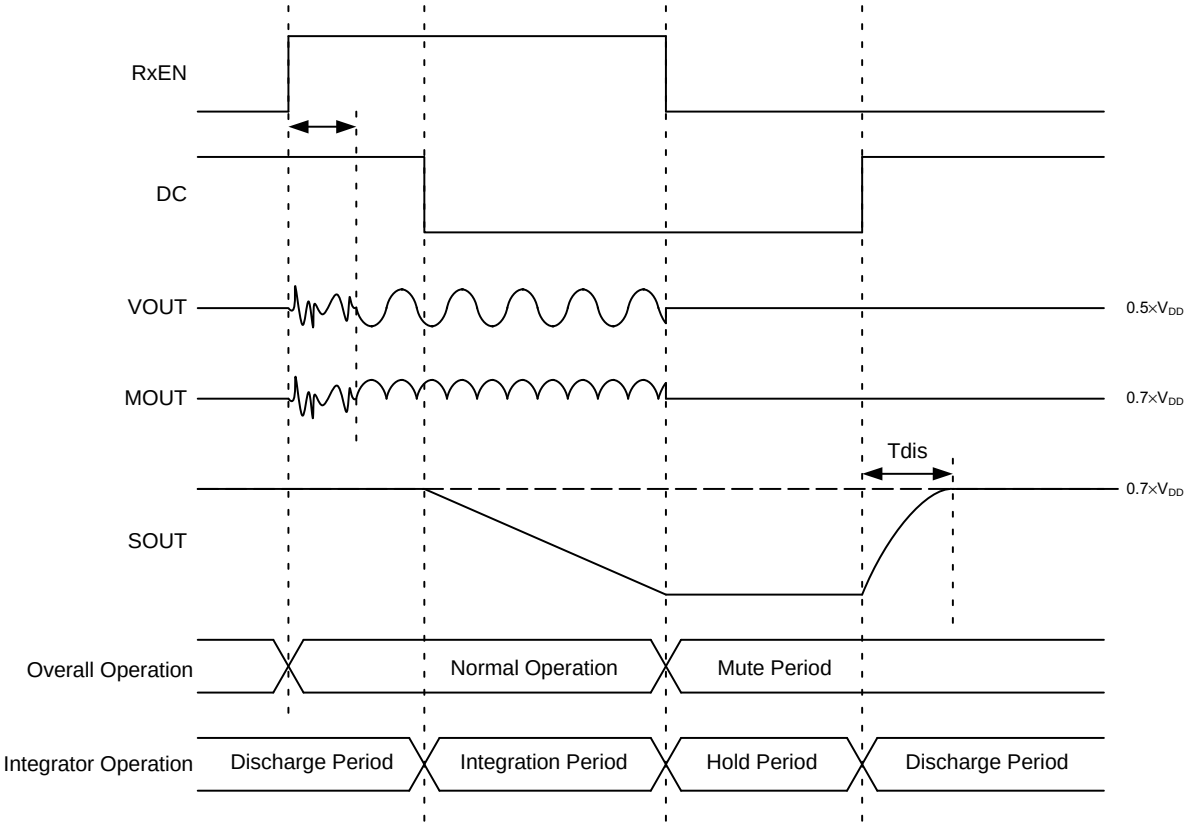


Figure 19. Integrator Discharge Time and Mute Recovery Time

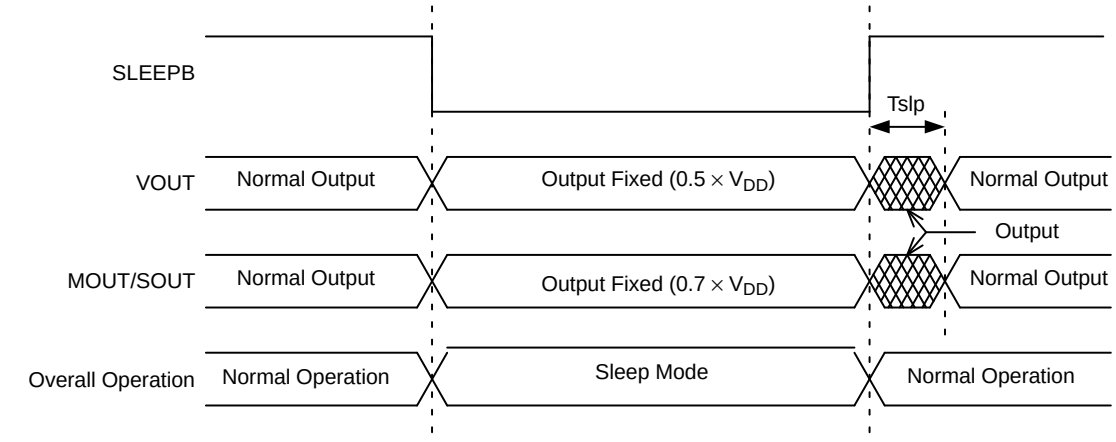
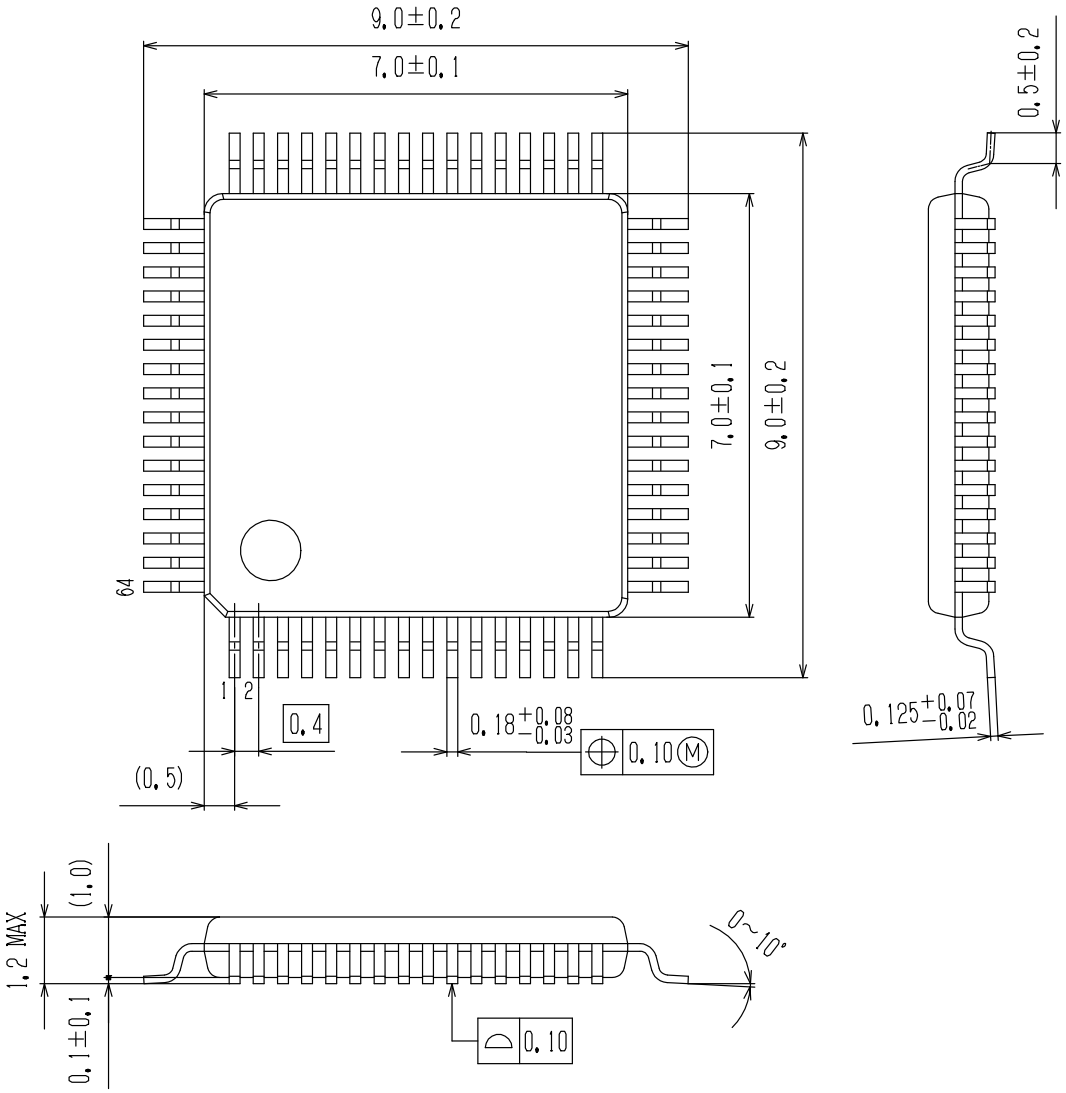


Figure 20. Sleep Recovery Time

PACKAGE DIMENSIONS

TQFP64 7x7 / TQFP64
CASE 932BC
ISSUE O



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