

# LV0222CS



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## Front Monitor OE-IC, for Optical Pickups

### Overview

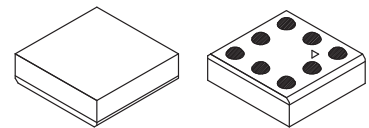
The LV0222CS is a front monitor optoelectronic IC for optical pickups that has a built-in photo diode compatible with three waveforms. LV0222CS is small size and type CSP packages.

### Functions

- PIN photodiode compatible with three wavelengths incorporated.
- Gain adjustment (-6dB to +6dB in 256 steps) through serial communication.
- Amplifier to amplify differential output.

### Applications

- Blu-ray Disk Drive for PC
- Blu-ray recorder
- Blu-ray player



ODCSP8 (1.75×1.75)

### Specifications

#### Maximum Ratings at Ta = 25°C (Note1)

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply	V <sub>CC</sub>		6	V
Allowable power dissipation	Pd1	Glass epoxy one-side substrate 55mm × 45mm × 0.8mm Copper foil area (about 80%), Ta=75°C	136	mW
	Pd2	Glass epoxy one-side substrate 55mm × 45mm × 0.8mm Copper foil area (head: about 85% Tail: about 90%), Ta=75°C	100	mW
Operating temperature	Topr		-20 to +85	°C
Storage temperature	Tstg		-40 to +100	°C

1. Stresses exceeding those listed in the Maximum Rating table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### Recommended Operating Conditions at Ta = 25°C (Note2)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply voltage	V <sub>CC</sub>		4.5	5	5.5	V
Output load capacitance	C <sub>O</sub>		12	20	33	pF
Output load resistance	Z <sub>O</sub>		3			kΩ

2. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

### ORDERING INFORMATION

Ordering Code:  
LV0222CS-TLM-H

Package  
ODCSP8  
(Pb-Free / Halogen Free)

Shipping (Qty / packing)  
4000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.  
[http://www.onsemi.com/pub\\_link/Collateral/BRD8011-D.PDF](http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF)

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**Electrical Characteristics at Ta = 25°C, VCC = 5V, RL=6kΩ, CL=20pF (Note3)**

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current dissipation	I <sub>CC</sub>			18	23.4	mA
Sleep current	I <sub>slp</sub>				1	mA
Output voltage when shielded	V <sub>C</sub>	At shielding	1.85	2.0	2.15	V
Output offset voltage	V <sub>ofs</sub>	At shielding, voltage between VOP-VON	-20	0	20	mV
Temperature dependence of offset voltage (Note4)	V <sub>ofs</sub>	Ta=-10 to +85°C	-30	0	30	μV/°C
Optical output voltage (Note4) Voltage between VOP-VON	V <sub>LC</sub>	Low Gain, λ=780nm, G=0dB	0.21	0.262	0.31	mV/μW
	V <sub>LD</sub>	Low Gain, λ=650nm, G=0dB	0.22	0.275	0.33	mV/μW
	V <sub>LB</sub>	Low Gain, λ=405nm, G=0dB	0.14	0.172	0.21	mV/μW
	V <sub>MC</sub>	Middle Gain, λ=780nm, G=0dB	0.66	0.83	0.99	mV/μW
	V <sub>MD</sub>	Middle Gain, λ=650nm, G=0dB	0.70	0.87	1.05	mV/μW
	V <sub>MB</sub>	Middle Gain, λ=405nm, G=0dB	0.43	0.54	0.65	mV/μW
	V <sub>HC</sub>	High Gain, λ=780nm, G=0dB	1.97	2.46	2.95	mV/μW
	V <sub>HD</sub>	High Gain, λ=650nm, G=0dB	2.07	2.58	3.10	mV/μW
	V <sub>HB</sub>	High Gain, λ=405nm, G=0dB	1.29	1.62	1.94	mV/μW
Light output voltage adjustment range (Note4)	G	G=0dB reference, absolute value of adjustment width	5.5	6.0	6.5	dB
D range (Note4)	V <sub>oD</sub>	Voltage between VOP-VON	1756	2200		mV
Frequency characteristics (Note4), (Note5)	F <sub>cC</sub>	-3dB(1MHz reference), λ=780nm Light input = 40μW(DC) + 20μW(AC)	50	75		MHz
	F <sub>cD</sub>	-3dB(1MHz reference), λ=650nm Light input = 40μW(DC) + 20μW(AC)	60	85		MHz
	F <sub>cB</sub>	-3dB(1MHz reference), λ=405nm Light input = 40μW(DC) + 20μW(AC)	60	85		MHz
Settling time (Note4)	T <sub>set</sub>			15		ns
Response time (Note4)	T <sub>r</sub> , T <sub>f</sub>	V <sub>o</sub> =0.9Vp-p, output level 10 to 90% f <sub>c</sub> =10MHz, duty=50%			10	ns
Overshoot (Note4)	O <sub>vst</sub>	V <sub>o</sub> =0.9Vp-p			15	%
Undershoot (Note4)	U <sub>nst</sub>	V <sub>o</sub> =0.9Vp-p			15	%
Linearity (Note4)	Lin	At output voltage 0.5V and 1.0V (Between VOP-VON)	-1	0	1	%
Light-output voltage temperature dependence Voltage between VOP-VON (Note4), (Note6)	T <sub>C</sub>	λ=780nm, 25°C reference	10	13	16	%
	T <sub>D</sub>	λ=650nm, 25°C reference	0	3	6	%
	T <sub>B</sub>	λ=405nm, 25°C reference	0	3	6	%
Light-output voltage spectral sensitivity Voltage between VOP-VON (Note4)	V <sub>f</sub>	λ=785nm ±5nm	-0.7		0	%/nm
		λ=660nm ±5nm	-0.3		0.3	%/nm
		λ=405nm ±5nm	0.1		1.1	%/nm
Step-step voltage ratio (Note4)	DG	(V <sub>n</sub> -V <sub>n-1</sub> ) / V <sub>n</sub> *100 (Note7) Deviation from the ideal curve of above equation	-3	0	3	%

3. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Indicate the design reference value.

5. Indicate the frequency characteristics when VOP and VON are applied individually.

The frequency characteristics are for the case of High / Middle / Low gain and for the case when the output voltage adjustment range is -6 to +6dB

6. indicates the temperature dependence for the case of High / Middle / Low gain and for the case when the temperature is 25 to 85°C for the output voltage adjustment range of -6 to +6dB

7. V<sub>n</sub> is V<sub>n</sub> = (sensitivity / 2) × 5400 / (5400-16 × GCAstep) × light intensity (μW)

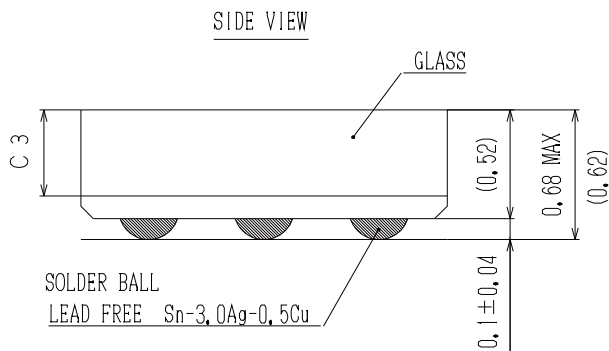
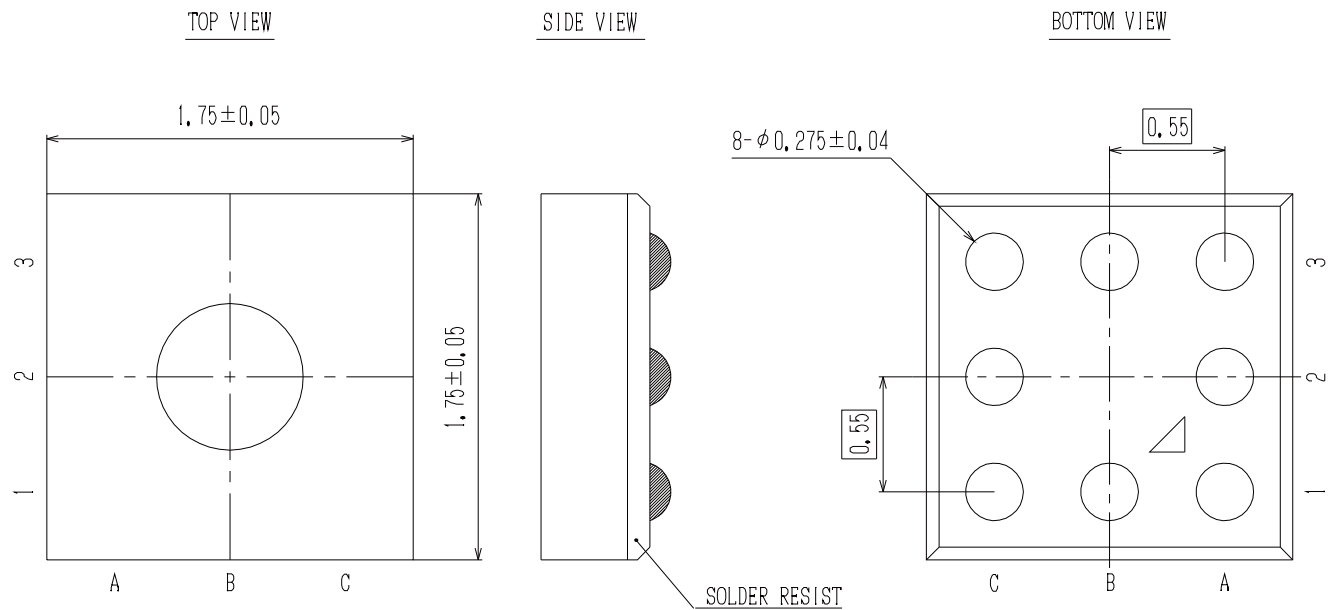
GCA = Gain Control Amplifier

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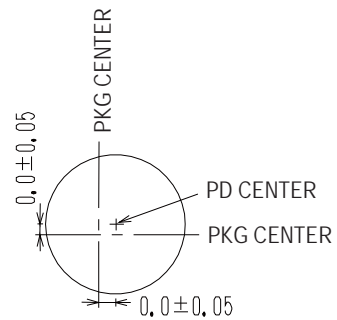
## Package Dimensions

unit : mm

ODCSP8 (1.75 × 1.75)



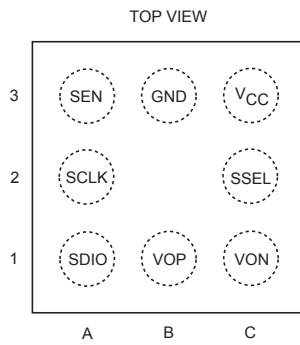
C3 = (Glass surface to PD : 412 ± 27 μm)



It is position clearance of PD CENTER to PKG CENTER

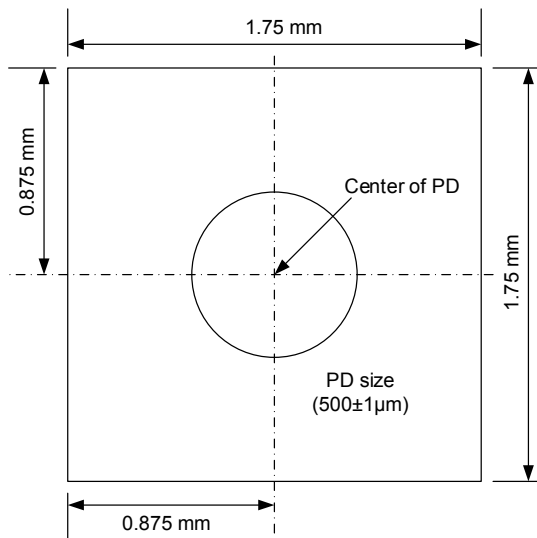
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## Pin Assignment



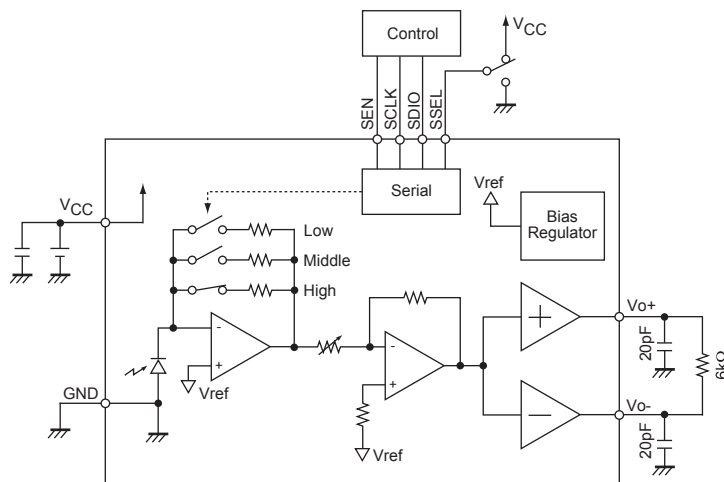
Pin No.	Pin name	Function
1A	SDIO	Serial communication Data pin
1B	VOP	Positive side output pin
1C	VON	Negative side output pin
2A	SCLK	Serial communication Clock pin
2C	SSEL	Register selection pin SSEL = Low, Open : Address 00 to 0Fh used SSEL = High : Address 10 to 1Fh used
3A	SEN	Serial communication Enable pin
3B	GND	GND pin
3C	V <sub>CC</sub>	Power supply voltage pin

## PD assignment



\*PD size for reference to be used for design

## Block diagram and Test circuit diagram



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## Resister table

Enable selection of the register group from the SSEL pin.

SSEL = Low, Open

	Address	7	6	5	4	3	2	1	0
Name	00h	<b>POWER</b>		<b>IV GAIN SEL</b>		<b>GAIN SEL</b>			
Default		00		00		00		x	x
Value		11: Power on 00 01 10: Sleep		00 01: High 10: Middle 11: Low		00 01: BD 10: DVD 11: CD			
Name	01h	<b>BD GAIN</b>							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	02h	<b>DVD GAIN</b>							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	03h	<b>CD GAIN</b>							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	0Eh	<b>TEST1 (*1)</b>							
Name	0Fh	<b>TEST2 (*1)</b>							

SSEL = High

	Address	7	6	5	4	3	2	1	0
Name	10h	<b>POWER</b>		<b>IV GAIN SEL</b>		<b>GAIN SEL</b>			
Default		00		00		00		x	x
Value		11: Power on 00 01 10: Sleep		00 01: High 10: Middle 11: Low		00 01: BD 10: DVD 11: CD			
Name	11h	<b>BD GAIN</b>							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	12h	<b>DVD GAIN</b>							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	13h	<b>CD GAIN</b>							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	1Eh	<b>TEST1 (*1)</b>							
Name	1Fh	<b>TEST2 (*1)</b>							

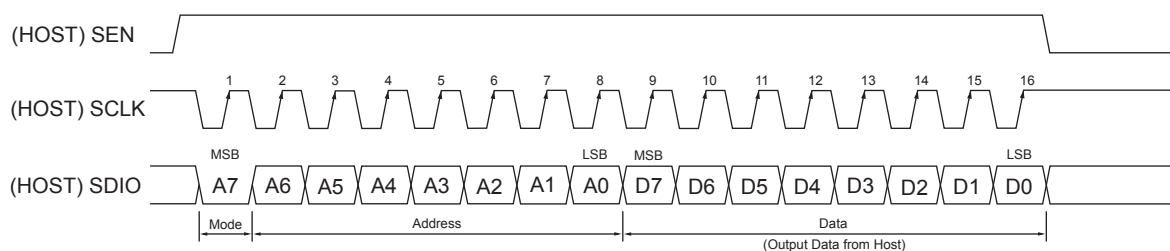
\*1 TEST1 and TEST2 are either the time when power is applied or "00000000" is set. Do not attempt to change "00000000" during operation. "00000000" is returned when reading is made.

\*2 No problem in terms of operation occurs even when writing is made to the address 04h to 0Dh and 14h to 1Dh. "00000000" is returned when this address is read.

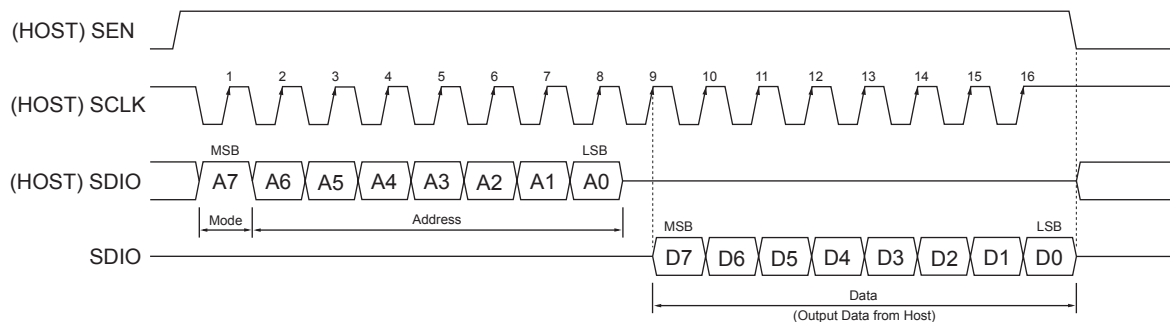
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## Serial protocol

WRITE timing chart



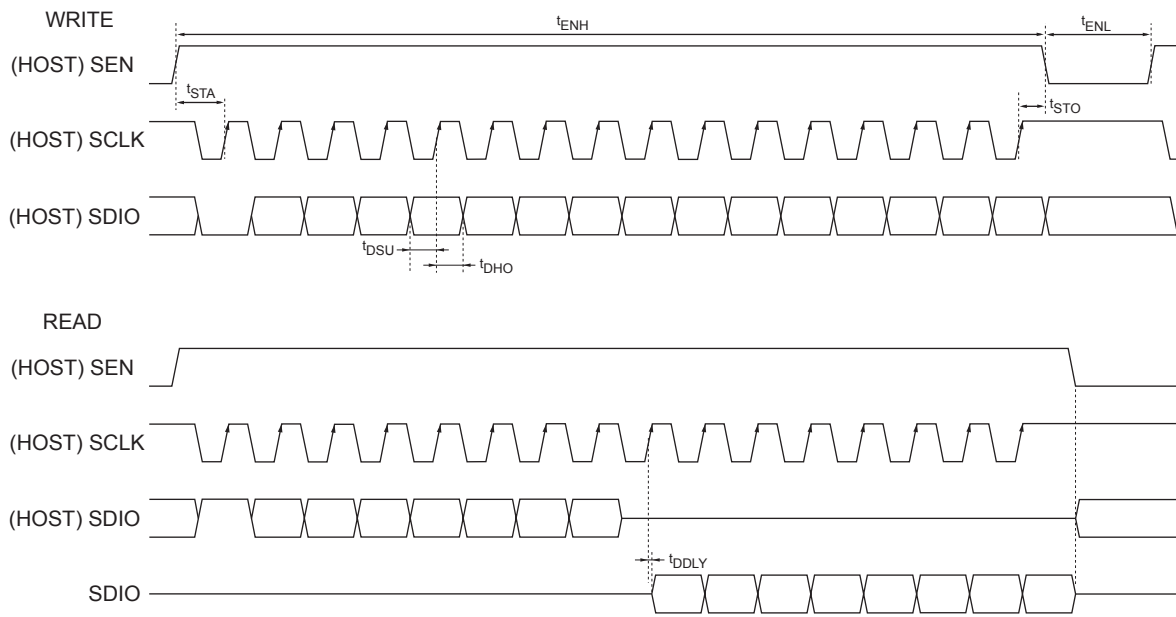
READ timing chart



SDIO pin load / CL=20pF (The table below shows the design reference value.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency Write	f <sub>SCL</sub>	0		10	MHz
SCL clock frequency Read	f <sub>SCL</sub>	0		4	MHz
SDIO data setup time	t <sub>DSU</sub>	50			ns
SDIO data hold time	t <sub>DHO</sub>	50			ns
SDIO output delay	t <sub>DDLY</sub>		10	80	ns
SEN "H" period	t <sub>ENH</sub>	1.6			μs
SEN "L" period	t <sub>ENL</sub>	200			ns
SCL rise time after SEN rise	t <sub>STA</sub>	60			ns
SEN fall time after final SCL rise	t <sub>STO</sub>	100			ns
Serial input "H" voltage	V <sub>IH</sub>	2.4			V
Serial input "L" voltage	V <sub>IL</sub>			0.6	V
SDIO output "H" voltage	V <sub>OH</sub>	2.5	2.9	3.3	V
SDIO output "L" voltage	V <sub>OL</sub>	0	0.3	0.8	V

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## Pin Functions

Pin	Type	Equivalent circuit diagram
SDIO	Input Output	
VOP VON	Output	
SCLK SSEL SEN	Input	

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