Front Monitor OE-IC, for Optical Pickups

Overview

The LV0229XA is a front monitor optoelectronic IC for optical pickups that has a built-in photo diode compatible with three waveforms. LV0229XA is small size and type CSP packages.

Function

- Pin photodiode compatible with three wavelengths incorporated.
- Gain adjustment (-5dB to +5dB in 256 steps) through serial communication.
- Amplifier to amplify differential output.
- Photodiode compatible with three wavelengths incorporated, high-speed process employed.
- Compact, thin CSP package employed.
- Use AR coated glass for three-wavelength (One side).

Typical Applications

- Blu-ray Disk Drive for PC
- Blu-ray recorder
- Blu-ray player

Specifications

Absolute Maximum Ratings at Ta = 25°C (Note1)

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	VCC		6	V
Allowable power dissipation	Pd	substrate (Note2), Ta = 75°C	105	mW
Operating temperature	Topr		-20 to +75	°C
Storage temperature	Tstg		-40 to +100	°C

Stresses exceeding those listed in the Maximum Rating table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Recommended Operating Conditions at Ta = 25°C (Note3

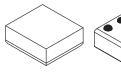
Descriptor	Oh. al	O disi		1.1:4			
Parameter	Symbol	Conditions	min	typ	max	Unit	
Operating supply voltage	Vcc		4.5	5	5.5	V	
Output load capacitance	Co		12	20	33	pF	
Output load resistance	Zo		3			kΩ	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.



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ODCSP8 (1.35 x 1.23)

ORDERING INFORMATION

Ordering Code: LV0229XA-NH

Package ODCSP8 (Pb-Free / Halogen Free)

Shipping (Qty / packing) 5000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D, http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

^{2.} Glass epoxy both-side substrate 55mm × 45mm × 1mm, Copper foil area (head: about 85% tail: about 70%).

$\textbf{Electrical and Optical Characteristics} \ \ \text{at Ta} = 25 ^{\circ}\text{C}, \ \ V_{CC} = 5 \text{V}, \ \ R_{L} = 6 \text{k}\Omega, \ \ C_{L} = 20 \text{pF} \qquad \text{(Note4)}$

Parameter	Symbol	Conditions	IV Gain		Ratings		Unit
Farameter	Symbol	Conditions	IV Gaiii	min	typ	max	Offic
Current dissipation	Icc			9	14	19	mA
Sleep current	Islp				0.2	0.5	mA
Output voltage when shielded	Vc	At shielding		1.85	2	2.15	V
Output offset voltage	Vofs	At shielding, voltage between VOP- VON		-30	0	30	mV
Temperature dependence of offset voltage (Note5)	Vofs	Ta = -10 to +75°C		-60	0	60	μV/°C
Optical output voltage (Note5)	VLC		Low	1.93	2.41	2.90	
Voltage between VOP-VON	VH1C	$\lambda = 780$ nm, G = 0dB	Middle	4.58	5.73	6.87	
	VH2C		High	10.86	13.58	16.29	
	VLD		Low	2.03	2.54	3.05	
	VH1D	$\lambda = 650$ nm, G = 0dB	Middle	4.82	6.02	7.23	mV/μW
	VH2D	, , , , , , , , , , , , , , , , , , , ,	High	11.42	14.28	17.13	.,.
	VLB		Low	1.27	1.59	1.90	
	VH1B	$\lambda = 405$ nm, G = 0dB	Middle	3.01	3.76	4.52	
	VH2B		High	7.14	8.92	10.71	
Light output voltage adjustment range (Note5)	G	G = 0dB reference, absolute value of adjustment width		4.5	5	5.5	dB
Output saturation voltage (Note5)	VoD	Voltage between VOP-VON		2000			mV
Frequency characteristics (Note5,6)	FcC	-3dB (1MHz reference), λ = 780nm Light input = 40 μ W (DC) + 20 μ W (AC)		40	60		
	FcD1	-3dB (1MHz reference), λ = 650nm Light input = 40μW (DC) + 20μW (AC)	Low Middle	60	85		
	FcD2	-3dB (1MHz reference), λ = 650nm Light input = 40μW (DC) + 20μW (AC)	High	50	70		MHz
	FcB1	-3dB (1MHz reference), λ = 405nm Light input = 40μW (DC) + 20μW (AC)	Low Middle	60	85		
	FcB2	-3dB (1MHz reference), λ = 405nm Light input = 40 μ W (DC) + 20 μ W (AC)	High	50	70		
Settling time (Note5)	Tset				10	15	ns
Response time (Note5)	Tr, Tf	Vo = 0.9Vp-p, output level 10 to 90% fc = 10MHz, duty = 50%			4	10	ns
Linearity (Note5)	Lin	At output voltage 0.5V and 1.0V (Between VOP-VON)		-1	0	1	%
Light-output voltage temperature dependence	TC	λ = 780nm, 25°C reference		6	9	12	%
Voltage between VOP-VON (Note5,7)	TD	λ = 650nm, 25°C reference		-3	0	3	%
	ТВ	λ = 405nm, 25°C reference		-2	1	4	%
Product parametric performance is indicated in	the Fleetries	I Characteristics for the listed test conditi		- 41 1	D		

^{4.} Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

[Expression of output voltage]

Vn = (sensitivity / 1.78) \times 5221 / (5221 - 14 \times GCAstep) \times light intensity (µW)

^{5.} The design reference value.

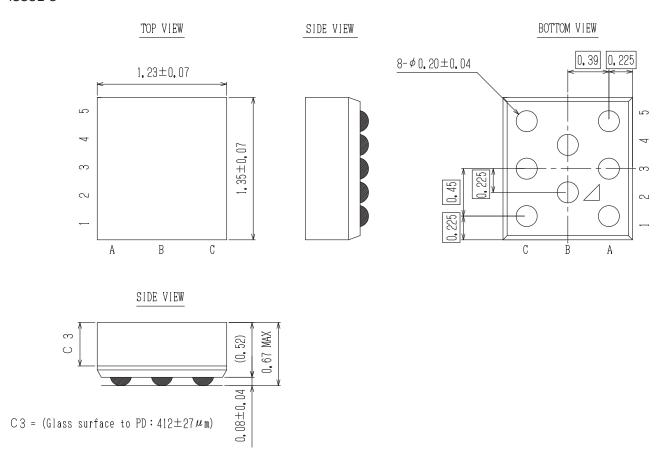
^{6.} The frequency characteristics when VOP and VON are applied individually.
The frequency characteristics are for the output voltage adjustment range is -5 to +5dB.

7. The temperature dependence for the case of High / Middle / Low gain and for the case when the temperature is 25 to 75°C for the output voltage adjustment range of -5 to +5dB.

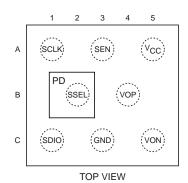
Package Dimensions

unit: mm

ODCSP8 1.35x1.23 CASE 570AR ISSUE O

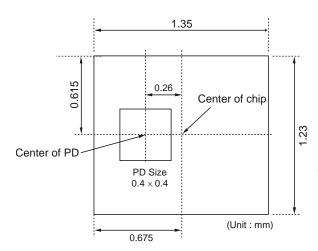


Pin Assignment



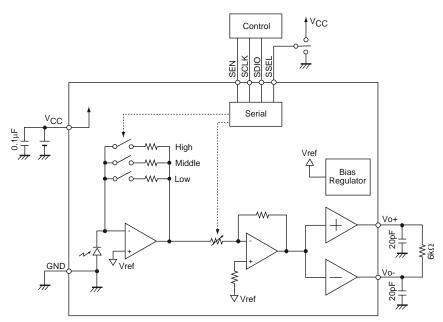
Pin No.	Pin name	Function
A1	SCLK	Serial communication Clock pin
А3	SEN	Serial communication Enable pin
A5	V _{CC}	Power supply voltage pin
B2	SSEL	Register selection pin
		SSEL = Low : Address 00 to 0Fh used
		SSEL = High : Address 10 to 1Fh used
		SSEL = Open : Address 70 to 7Fh used
B4	VOP	Positive side output pin
C1	SDIO	Serial communication Data pin
C3	GND	GND pin
C5	VON	Negative side output pin

PD assignment



*PD size for reference to be used for design

Block diagram and Test circuit diagram



* Please place decoupling capacitors within 3mm from pin

Resister table

Enable selection of the register group from the SSEL pin.

SSEL = Low

	Address	7	6	5	4	3	2	1	0	
Name		POV	POWER		IV GAIN SEL					
Default		0	00		0	0	0	0	0	
Value	00h	11: Power on 00/01/10: Sleep		00/01: High 10: Middle 11: Low						
Name			GAIN							
Default	01h	1	1	1	1	1	1	1	1	
Value		00000000 to 11111111								
Name	0Eh		TEST1 (*1)							

SSEL = High

DOLL - II				1	1	1	1		
	Address	7	6	5	4	3	2	1	0
Name		POWER		IV GAIN SEL					
Default		0	00		00	0	0	0	0
	10h	11: Power on		11: Power on 00/01: High					
Value		00/01/10: Sleep		10: Middle					
				11: Low					
Name			GAIN						
Default	11h	1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	1Eh		TEST1 (*1)						

SSEL = Open

	Address	7	6	5	4	3	2	1	0	
Name		POV	POWER		IV GAIN SEL					
Default		0	00		0	0	0	0	0	
Value	70h	11: Power on 00/01/10: Sleep		00/01: High 10: Middle 11: Low						
Name			GAIN							
Default	71h	1	1	1	1	1	1	1	1	
Value		00000000 to 11111111								
Name	7Eh		TEST1 (*1)							

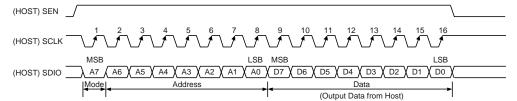
^{*1} TEST1 are either the time when power is applied or "00000000" is set. Do not attempt to change "00000000" during operation. "00000000" is returned when reading is made.

^{*2} No problem in terms of operation occurs even when writing is made to the address 02h to 0Dh & 0Fh, 12h to 1Dh & 1Fh and 72h to 7Dh & 7Fh. "00000000" is returned when this address is read.

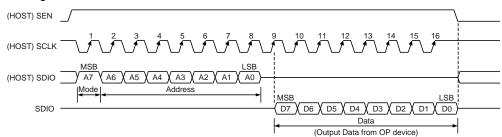
^{*3} When I performed address reading except the register group set by an SSEL terminal, I keep Hi-Z without paying a value.

Serial protocol

WRITE timing chart

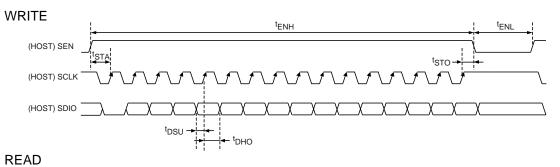


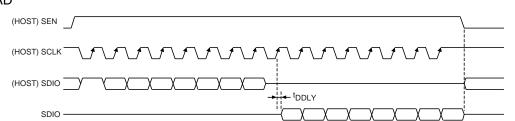
READ timing chart



SDIO pin load / $C_L = 20 pF$. The table below shows the design reference value.

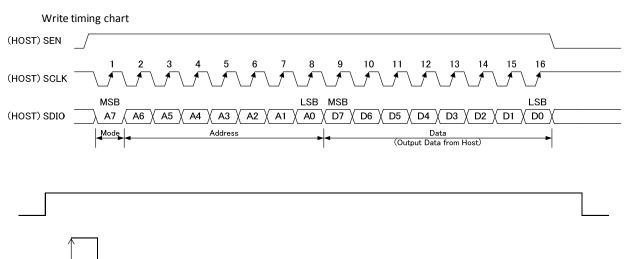
Parameter	Symbol	Min.	Тур.	Max.	Unit
SCL clock frequency Write	fSCL	0		10	MHz
SCL clock frequency Read	fSCL	0		4	MHz
SDIO data setup time	t _{DSU}	50			ns
SDIO data hold time	^t DHO	50			ns
SDIO output delay	^t DDLY		10	80	ns
SEN "H" period	t _{ENH}	1.6			μS
SEN "L" period	t _{ENL}	200			ns
SCL rise time after SEN rise	^t STA	60			ns
SEN fall time after final SCL rise	^t STO	100			ns
Serial input "H" voltage	V _I H	2.4		Vcc	V
Serial input "L" voltage	V _I L			0.6	V
SDIO output "H" voltage	V _O H	2.5	2.9	3.3	V
SDIO output "L" voltage	V _O L	0	0.3	0.8	V





Pin Description

Pin	Type	Equivalent circuit diagram
SDIO		
3510	Input Output	3V 3V 125 Ω 100kΩ 100kΩ
VOP VON	Output	$\frac{20\Omega}{m}$
SCLK SEN	Input	3V 100kΩ ———————————————————————————————————
SSEL	Input	$\begin{array}{c c} & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & \\ & & & \\ & & & \\ & & \\ & & & \\ & & \\ & & & \\ & &$



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